

Instruction Set

Hexadecimal	Load and Store Instructions
<u>Load Accumulator (LD)</u>	
C0XX	Contents of CSL at EA (I+DISP) are loaded into A
C1XX	Contents of CSL at EA (XR1+DISP) are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP) are loaded into A
C400XXXX	Contents of CSL at EA (Addr) are loaded into A
C500XXXX	Contents of CSL at EA (Addr+XR1) are loaded into A
C600XXXX	Contents of CSL at EA (Addr+XR2) are loaded into A
C700XXXX	Contents of CSL at EA (Addr+XR3) are loaded into A
C800XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A
C580XXXX	Contents of CSL at EA (V in CSL at "Addr+XR1") are loaded into A
C680XXXX	Contents of CSL at EA (V in CSL at "Addr+XR2") are loaded into A
C780XXXX	Contents of CSL at EA (V in CSL at "Addr+XR3") are loaded into A
<u>Double Load (LDD)</u>	
C8XX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q
C9XX	Contents of CSL at EA (XR1 + DISP) and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q
CC00XXXX	Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q
CD00XXXX	Contents of CSL at EA (Addr+XR1) and EA+1 are loaded into A and Q
CE00XXXX	Contents of CSL at EA (Addr+XR2) and EA+1 are loaded into A and Q
CF00XXXX	Contents of CSL at EA (Addr+XR3) and EA+1 are loaded into A and Q
CC80XXXX	Contents of CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q
CD80XXXX	Contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 are loaded into A and Q
CE80XXXX	Contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 are loaded into A and Q
CF80XXXX	Contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 are loaded into A and Q
<u>Store Accumulator (STO)</u>	
D0XX	Contents of A are stored in CSL at EA (I+DISP)
D1XX	Contents of A are stored in CSL at EA (XR1+DISP)
D2XX	Contents of A are stored in CSL at EA (XR2+DISP)
D3XX	Contents of A are stored in CSL at EA (XR3+DISP)
D400XXXX	Contents of A are stored in CSL at EA (Addr)
D500XXXX	Contents of A are stored in CSL at EA (Addr+XR1)
D600XXXX	Contents of A are stored in CSL at EA (Addr+XR2)
D700XXXX	Contents of A are stored in CSL at EA (Addr+XR3)
D800XXXX	Contents of A are stored in CSL at EA (V in CSL at Addr)
D580XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr+XR1")
D680XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr+XR2")
D780XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr+XR3")
<u>Double Store (STD)</u>	
D8XX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in CSL at EA (XR1+DISP) and EA+1
DAXX	Contents of A and Q are stored in CSL at EA (XR2+DISP) and EA+1
DBXX	Contents of A and Q are stored in CSL at EA (XR3+DISP) and EA+1
DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr+XR1) and EA+1
DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr+XR2) and EA+1
DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr+XR3) and EA+1
DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1
DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr+XR1") and EA+1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr+XR2") and EA+1
DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr+XR3") and EA+1
<u>Load Index (LDX)</u>	
60XX	Load DISP into the Instruction Register
61XX	Load DISP into Index Register 1
62XX	Load DISP into Index Register 2
63XX	Load DISP into Index Register 3
6400XXXX	Load Addr into the Instruction Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2
6700XXXX	Load Addr into Index Register 3
6480XXXX	Load contents of CSL at Addr into the Instruction Register
6580XXXX	Load contents of CSL at Addr into Index Register 1
6680XXXX	Load contents of CSL at Addr into Index Register 2
6780XXXX	Load contents of CSL at Addr into Index Register 3
<u>Store Index (STX)</u>	
68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX	Store XR3 in CSL at EA (I+DISP)
6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)
6C80XXXX	Store I in CSL at EA (V in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (V in CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (V in CSL at Addr)
<u>Store Status (STS)</u>	
28XX	Store status of indicators in CSL at EA (I+DISP)
29XX	Store status of indicators in CSL at EA (XR1+DISP)
2AXX	Store status of indicators in CSL at EA (XR2+DISP)
2BXX	Store status of indicators in CSL at EA (XR3+DISP)
2C00XXXX	Store status of indicators in CSL at EA (Addr)

Hexadecimal	Load and Store Instructions
2D00XXXX	Store status of indicators in CSL at EA (Addr+XR1)
2E00XXXX	Store status of indicators in CSL at EA (Addr+XR2)
2F00XXXX	Store status of indicators in CSL at EA (Addr+XR3)
2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)
2D80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr+XR1")
2E80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr+XR2")
2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr+XR3")
2C40XXXX	Clear storage protect bit in CSL at EA (Addr)
2C41XXXX	Write storage protect bit in CSL at EA (Addr)
2D40XXXX	Clear storage protect bit in CSL at EA (Addr+XR1)
2D41XXXX	Write storage protect bit in CSL at EA (Addr+XR1)
2E40XXXX	Clear storage protect bit in CSL at EA (Addr+XR2)
2E41XXXX	Write storage protect bit in CSL at EA (Addr+XR2)
2F40XXXX	Clear storage protect bit in CSL at EA (Addr+XR3)
2F41XXXX	Write storage protect bit in CSL at EA (Addr+XR3)
2CC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at Addr)
2CC1XXXX	Write storage protect bit in CSL at EA (V in CSL at Addr)
2DC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR1")
2DC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR1")
2EC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR2")
2EC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR2")
2FC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR3")
2FC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR3")
<u>Load Status (LDS)</u>	
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF
2002	Set OVERFLOW OFF and CARRY ON
2003	Set CARRY and OVERFLOW indicator ON
<u>Arithmetic Instructions</u>	
<u>Add (A)</u>	
80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX	Add contents of CSL at EA (XR2+DISP) to A
83XX	Add contents of CSL at EA (XR3+DISP) to A
8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX	Add contents of CSL at EA (Addr+XR1) to A
8600XXXX	Add contents of CSL at EA (Addr+XR2) to A
8700XXXX	Add contents of CSL at EA (Addr+XR3) to A
8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
<u>Double Add (AD)</u>	
88XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q
8C00XXXX	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8F00XXXX	Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 to A and Q
8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q
8F80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 to A and Q
<u>Subtract (S)</u>	
90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX	Subtract contents of CSL at EA (XR1+DISP) from A
92XX	Subtract contents of CSL at EA (XR2+DISP) from A
93XX	Subtract contents of CSL at EA (XR3+DISP) from A
9400XXXX	Subtract contents of CSL at EA (Addr) from A
9500XXXX	Subtract contents of CSL at EA (Addr+XR1) from A
9600XXXX	Subtract contents of CSL at EA (Addr+XR2) from A
9700XXXX	Subtract contents of CSL at EA (Addr+XR3) from A
9480XXXX	Subtract contents of CSL at EA (V in CSL at Addr) from A
9580XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A
9780XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") from A
<u>Double Subtract (SD)</u>	
98XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
99XX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q
9AXX	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9D00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q
9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q
9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q
9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
<u>Multiply (M)</u>	
A0XX	Multiply contents of CSL at EA (I+DISP) by A
A1XX	Multiply contents of CSL at EA (XR1+DISP) by A
A2XX	Multiply contents of CSL at EA (XR2+DISP) by A
A3XX	Multiply contents of CSL at EA (XR3+DISP) by A
A400XXXX	Multiply contents of CSL at EA (Addr) by A

Instruction Set

Hexadecimal	Arithmetic Instructions
A500XXXX A600XXXX A700XXXX A480XXXX A580XXXX A680XXXX A780XXXX	Multiply contents of CSL at EA (Addr+XR1) by A Multiply contents of CSL at EA (Addr+XR2) by A Multiply contents of CSL at EA (Addr+XR3) by A Multiply contents of CSL at EA (V in CSL at Addr) by A Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	<u>Divide (D)</u>
A8XX A9XX AAXX ABXX AC00XXXX AD00XXXX AE00XXXX AF00XXXX AC80XXXX AD80XXXX AE80XXXX AF80XXXX	Divide A and Q by contents of CSL at EA (I+DISP) Divide A and Q by contents of CSL at EA (XR1+DISP) Divide A and Q by contents of CSL at EA (XR2+DISP) Divide A and Q by contents of CSL at EA (XR3+DISP) Divide A and Q by contents of CSL at EA (Addr) Divide A and Q by contents of CSL at EA (Addr+XR1) Divide A and Q by contents of CSL at EA (Addr+XR2) Divide A and Q by contents of CSL at EA (Addr+XR3) Divide A and Q by contents of CSL at EA (V in CSL at Addr) Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1") Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2") Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")
	<u>Logical And (AND)</u>
E0XX E1XX E2XX E3XX E400XXXX E500XXXX E600XXXX E700XXXX E480XXXX E580XXXX E680XXXX E780XXXX	AND contents of CSL at EA (I+DISP) with A AND contents of CSL at EA (XR1+DISP) with A AND contents of CSL at EA (XR2+DISP) with A AND contents of CSL at EA (XR3+DISP) with A AND contents of CSL at EA (Addr) with A AND contents of CSL at EA (Addr+XR1) with A AND contents of CSL at EA (Addr+XR2) with A AND contents of CSL at EA (Addr+XR3) with A AND contents of CSL at EA (V in CSL at Addr) with A AND contents of CSL at EA (V in CSL at "Addr+XR1") with A AND contents of CSL at EA (V in CSL at "Addr+XR2") with A AND contents of CSL at EA (V in CSL at "Addr+XR3") with A
	<u>Logical Or (OR)</u>
E8XX E9XX EAXX EBXX EC00XXXX ED00XXXX EE00XXXX EF00XXXX EC80XXXX ED80XXXX EE80XXXX EF80XXXX	OR contents of CSL at EA (I+DISP) with A OR contents of CSL at EA (XR1+DISP) with A OR contents of CSL at EA (XR2+DISP) with A OR contents of CSL at EA (XR3+DISP) with A OR contents of CSL at EA (Addr) with A OR contents of CSL at EA (Addr+XR1) with A OR contents of CSL at EA (Addr+XR2) with A OR contents of CSL at EA (Addr+XR3) with A OR contents of CSL at EA (V in CSL at Addr) with A OR contents of CSL at EA (V in CSL at "Addr+XR1") with A OR contents of CSL at EA (V in CSL at "Addr+XR2") with A OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	<u>Logical Exclusive Or (EOR)</u>
F0XX F1XX F2XX F3XX F400XXXX F500XXXX F600XXXX F700XXXX F480XXXX F580XXXX F680XXXX F780XXXX	EOR contents of CSL at EA (I+DISP) with A EOR contents of CSL at EA (XR1+DISP) with A EOR contents of CSL at EA (XR2+DISP) with A EOR contents of CSL at EA (XR3+DISP) with A EOR contents of CSL at EA (Addr) with A EOR contents of CSL at EA (Addr+XR1) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (Addr+XR3) with A EOR contents of CSL at EA (V in CSL at Addr) with A EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
Hexadecimal	Shift Instructions
	<u>Shift Left Logical A (SLA)</u>
10*X 1100 1200 1300	Contents of A shift left the number of shift counts in DISP Contents of A shift left the number of shift counts in XR1 Contents of A shift left the number of shift counts in XR2 Contents of A shift left the number of shift counts in XR3
	<u>Shift Left Logical A & Q (SLT)</u>
10*X 1180 1280 1380	Contents of A and Q shift left the number of shift counts in DISP Contents of A and Q shift left the number of shift counts in XR1 Contents of A and Q shift left the number of shift counts in XR2 Contents of A and Q shift left the number of shift counts in XR3
	<u>Shift Left And Count A (SLCA)</u>
10*X 1140 1240 1340	Contents of A shift left the number of shift counts in DISP Contents of A shift left the number of shift counts in XR1 Contents of A shift left the number of shift counts in XR2 Contents of A shift left the number of shift counts in XR3
	<u>Shift Left And Count A & Q (SLC)</u>
10*X 11C0 12C0 13C0	Contents of A and Q shift left the number of shift counts in DISP Contents of A and Q shift left the number of shift counts in XR1 Contents of A and Q shift left the number of shift counts in XR2 Contents of A and Q shift left the number of shift counts in XR3
	<u>Shift Right Logical A (SRA)</u>
18*X 1900 1A00 1B00	Contents of A shift right the number of shift counts in DISP Contents of A shift right the number of shift counts in XR1 Contents of A shift right the number of shift counts in XR2 Contents of A shift right the number of shift counts in XR3

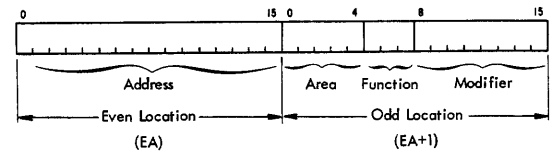
Hexadecimal	Shift Instructions
	<u>Shift Right A & Q (SRT)</u>
18*X 1900 1A80 1B80	Contents of A and Q shift right the number of shift counts in DISP Contents of A and Q shift right the number of shift counts in XR1 Contents of A and Q shift right the number of shift counts in XR2 Contents of A and Q shift right the number of shift counts in XR3
	<u>Rotate Right A & Q (RTE)</u>
18*X 19C0 1AC0 1BC0	Contents of A and Q rotate right the number of counts in DISP Contents of A and Q rotate right the number of counts in XR1 Contents of A and Q rotate right the number of counts in XR2 Contents of A and Q rotate right the number of counts in XR3
Hexadecimal	Branch Instructions
	<u>Branch Or Skip On Condition (BSC or BOSQ)</u>
48*X 4C*XXXXXX 4D*XXXXXX 4E*XXXXXX 4F*XXXXXX 4C*XXXXXX 4D*XXXXXX 4E*XXXXXX 4F*XXXXXX	Skip the next one-word instruction if ANY condition is sensed Branch to CSL at EA (Addr) on NO condition Branch to CSL at EA (Addr+XR1) on NO condition Branch to CSL at EA (Addr+XR2) on NO condition Branch to CSL at EA (Addr+XR3) on NO condition Branch to CSL at EA (V in CSL at Addr) on NO condition Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	<u>Branch And Store Instruction Register (BSI)</u>
40XX 41XX 42XX 43XX 44*XXXXXX 45*XXXXXX 46*XXXXXX 47*XXXXXX 44*XXXXXX 45*XXXXXX 46*XXXXXX 47*XXXXXX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1 Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1 Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1 Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr+XR3) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1
	<u>Modify Index and Skip (MDX)</u>
70XX 71XX 72XX 73XX 74XXXXXX 7500XXXX 7600XXXX 7700XXXX 74XXXXXX 7580XXXX 7680XXXX 7780XXXX	ADD expanded DISP to I (no skip can occur) ADD expanded DISP to XR1 ADD expanded DISP to XR2 ADD expanded DISP to XR3 Add expanded positive DISP to CSL at Addr (Add to memory) Add Addr to XR1 Add Addr to XR2 Add Addr to XR3 Add expanded negative DISP to CSL at Addr (Add to Memory) Add V in CSL at Addr to XR1 Add V in CSL at Addr to XR2 Add V in CSL at Addr to XR3
	<u>Wait (WAIT)</u>
3000	WAIT until manual start or until completion of an interrupt subroutine
	<u>Compare (CMP)</u>
80XX 81XX 82XX 83XX 8400XXXX 8500XXXX 8600XXXX 8700XXXX 8480XXXX 8580XXXX 8680XXXX 8780XXXX	Compare A with contents of CSL at EA (I+DISP) Compare A with contents of CSL at EA (XR1+DISP) Compare A with contents of CSL at EA (XR2+DISP) Compare A with contents of CSL at EA (XR3+DISP) Compare A with contents of CSL at EA (Addr) Compare A with contents of CSL at EA (Addr+XR1) Compare A with contents of CSL at EA (Addr+XR2) Compare A with contents of CSL at EA (Addr+XR3) Compare A with contents of CSL at EA (V in CSL at Addr) Compare A with contents of CSL at EA (V in CSL at "Addr+XR1") Compare A with contents of CSL at EA (V in CSL at "Addr+XR2") Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")
	<u>Double Compare (DCM)</u>
88XX 89XX 8AXX 8BXX 8C00XXXX 8D00XXXX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1 Compare A and Q with contents of CSL at EA (Addr) and EA+1 Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1

Input/Output Control Commands

Device/Function	IOCC		
	Address Word	Area, Function, and Modifier Word	
		Hex.	Hex.
Console (Area 0000) Continued			
Interrupt (Console) Sense	0000	Load Indicator Status to A-register	07C0 1 -Reset Indicator
Operations Monitor Control	0000	Reset Timer	04E1
Interval Timers Sense	0000	Load Indicator Status to A-register	0720 1 -Reset Indicator
Control	X000 	Start or Stop Timer	0420
Interrupt Mask Register Control	XXXX (Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9) 1-bit = mask 0-bit = unmask	Levels 0-13- Levels 14-23-	0480 0481
Program Interrupt Control	XXXX (Generate Interrupt with 1-bit. Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9.)	Levels 0-13- Levels 14-23-	04A0 04A1
Digital Input			
Direct Program Control Read	XXXX (Addr to Store Digit Input Group)	DI or PI Group to Core Storage	5A XX -DI Addr 40 thru 7F or PI Addr 02 thru 19
Sense Device	0000	DSW, DI, or PISW A-register	5F 00 -DSW 01 -DSW, Reset Indicators XX -DI Addr 40 thru 7F or PISW Addr 02 thru 19
Control	0000	Generate Reset to DI Controls	5C20
Data Channel Control			
Initialize Read	XXXX (Addr of Data Table)	Set up DC Controls for Transfer of Data	5E X0
Analog Input			
Direct Program Control Write	XXXX (Mpx Addr Location)	AI- AIE- 51 81 XX 	Analog Input to ADC
Read	XXXX (Addr to Store ADC Reading)	AI- AIE- 52 82 00 80	ADC to Core -Sequential Programmed Operation
Control	0000	AI- AIE- 5400 8400	Reset Controls and Registers
Sense Device	0000	AI- AIE- 57 87 0 8 1	-AI -Comparator -Reset Indicators

Device/Function	IOCC		
	Address Word	Area, Function, and Modifier Word	
		Hex.	Hex.
Analog Input Continued			
Data Channel Control			
Initialize Write	XXXX (First Mpx Addr Table Location)	AI- AIE- 5500 8500	(Set up DC for Transfer of Mpx Addr and Limit Words)
Initialize Read	XXXX (First Data Table Addr)	AI- AIE- 56 86 XX 	00=11-bit res. 01=14-bit res. 10=8-bit res. 0=1 DC Operation 1=2 DC Operation 1=Ex. Sync.
Digital and Analog Output			
Direct Program Control			
Write	XXXX (Addr of Output Data)	Core Storage to DAO Device	61 XX -DAO Register Addr 00 thru 7F
Control	0000		64 20 -Reset DAO Controls 40 -Inflate Simultaneous Transfer from Registers 80 -Start Pulse Output Timer
Sense Device	0000	DSW to A A-register	6700 01 -Reset Indicators
Data Channel Control			
Initialize Write	XXXX (Addr of Data Table)	Set up DC Controls to Transfer Data	65 X0

IOCC Format



Interrupts

Interrupt	Priority Level	Core Storage Location		ILSW
		Decimal	Hex.	
Internal	1	8	8	Yes
Trace	26	9	9	No
** CE	27	10	A	No
*External 0	2	11	B	Yes
1	3	12	C	Yes
2	4	13	D	Yes
3	5	14	E	Yes
4	6	15	F	Yes
5	7	16	10	Yes
6	8	17	11	Yes
7	9	18	12	Yes
8	10	19	13	Yes
9	11	20	14	Yes
10	12	21	15	Yes
11	13	22	16	Yes
12	14	23	17	Yes
13	15	24	18	Yes
14	16	25	19	Yes
15	17	26	1A	Yes
16	18	27	1B	Yes
17	19	28	1C	Yes
18	20	29	1D	Yes
19	21	30	1E	Yes
20	22	31	1F	Yes
21	23	32	20	Yes
22	24	33	21	Yes
23	25	34	22	Yes

* External interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE Interrupt Stores the return link in core location 10 (decimal) and starts execution at core location 0001. Interrupts are prevented in the same manner as for the standard forced BSI.

Instruction Set

Hexadecimal	Arithmetic Instructions
A500XXXX A600XXXX A700XXXX A480XXXX A580XXXX A680XXXX A780XXXX	Multiply contents of CSL at EA (Addr+XR1) by A Multiply contents of CSL at EA (Addr+XR2) by A Multiply contents of CSL at EA (Addr+XR3) by A Multiply contents of CSL at EA (V in CSL at Addr) by A Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	<u>Divide (D)</u>
A8XX A9XX AAXX ABXX AC00XXXX AD00XXXX AE00XXXX AF00XXXX AC80XXXX AD80XXXX AE80XXXX AF80XXXX	Divide A and Q by contents of CSL at EA (I+DISP) Divide A and Q by contents of CSL at EA (XR1+DISP) Divide A and Q by contents of CSL at EA (XR2+DISP) Divide A and Q by contents of CSL at EA (XR3+DISP) Divide A and Q by contents of CSL at EA (Addr) Divide A and Q by contents of CSL at EA (Addr+XR1) Divide A and Q by contents of CSL at EA (Addr+XR2) Divide A and Q by contents of CSL at EA (Addr+XR3) Divide A and Q by contents of CSL at EA (V in CSL at Addr) Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1") Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2") Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")
	<u>Logical And (AND)</u>
E0XX E1XX E2XX E3XX E400XXXX E500XXXX E600XXXX E700XXXX E480XXXX E580XXXX E680XXXX E780XXXX	AND contents of CSL at EA (I+DISP) with A AND contents of CSL at EA (XR1+DISP) with A AND contents of CSL at EA (XR2+DISP) with A AND contents of CSL at EA (XR3+DISP) with A AND contents of CSL at EA (Addr) with A AND contents of CSL at EA (Addr+XR1) with A AND contents of CSL at EA (Addr+XR2) with A AND contents of CSL at EA (Addr+XR3) with A AND contents of CSL at EA (V in CSL at Addr) with A AND contents of CSL at EA (V in CSL at "Addr+XR1") with A AND contents of CSL at EA (V in CSL at "Addr+XR2") with A AND contents of CSL at EA (V in CSL at "Addr+XR3") with A
	<u>Logical Or (OR)</u>
E8XX E9XX EAXX EBXX EC00XXXX ED00XXXX EE00XXXX EF00XXXX EC80XXXX ED80XXXX EE80XXXX EF80XXXX	OR contents of CSL at EA (I+DISP) with A OR contents of CSL at EA (XR1+DISP) with A OR contents of CSL at EA (XR2+DISP) with A OR contents of CSL at EA (XR3+DISP) with A OR contents of CSL at EA (Addr) with A OR contents of CSL at EA (Addr+XR1) with A OR contents of CSL at EA (Addr+XR2) with A OR contents of CSL at EA (Addr+XR3) with A OR contents of CSL at EA (V in CSL at Addr) with A OR contents of CSL at EA (V in CSL at "Addr+XR1") with A OR contents of CSL at EA (V in CSL at "Addr+XR2") with A OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	<u>Logical Exclusive Or (EOR)</u>
F0XX F1XX F2XX F3XX F400XXXX F500XXXX F600XXXX F700XXXX F480XXXX F580XXXX F680XXXX F780XXXX	EOR contents of CSL at EA (I+DISP) with A EOR contents of CSL at EA (XR1+DISP) with A EOR contents of CSL at EA (XR2+DISP) with A EOR contents of CSL at EA (XR3+DISP) with A EOR contents of CSL at EA (Addr) with A EOR contents of CSL at EA (Addr+XR1) with A EOR contents of CSL at EA (Addr+XR2) with A EOR contents of CSL at EA (Addr+XR3) with A EOR contents of CSL at EA (V in CSL at Addr) with A EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	<u>Shift Instructions</u>
	<u>Shift Left Logical A (SLA)</u>
10*X 1100 1200 1300	Contents of A shift left the number of shift counts in DISP Contents of A shift left the number of shift counts in XR1 Contents of A shift left the number of shift counts in XR2 Contents of A shift left the number of shift counts in XR3
	<u>Shift Left Logical A & Q (SLT)</u>
10*X 1180 1280 1380	Contents of A and Q shift left the number of shift counts in DISP Contents of A and Q shift left the number of shift counts in XR1 Contents of A and Q shift left the number of shift counts in XR2 Contents of A and Q shift left the number of shift counts in XR3
	<u>Shift Left And Count A (SLCA)</u>
10*X 1140 1240 1340	Contents of A shift left the number of shift counts in DISP Contents of A shift left the number of shift counts in XR1 Contents of A shift left the number of shift counts in XR2 Contents of A shift left the number of shift counts in XR3
	<u>Shift Left And Count A & Q (SLCQ)</u>
10*X 11C0 12C0 13C0	Contents of A and Q shift left the number of shift counts in DISP Contents of A and Q shift left the number of shift counts in XR1 Contents of A and Q shift left the number of shift counts in XR2 Contents of A and Q shift left the number of shift counts in XR3
	<u>Shift Right Logical A (SRA)</u>
18*X 1900 1A00 1B00	Contents of A shift right the number of shift counts in DISP Contents of A shift right the number of shift counts in XR1 Contents of A shift right the number of shift counts in XR2 Contents of A shift right the number of shift counts in XR3

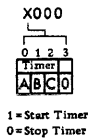
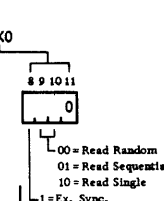
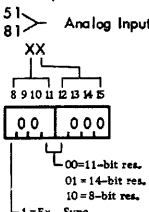
Hexadecimal	Shift Instructions
	<u>Shift Right A & Q (SRT)</u>
18*X 1980 1A80 1B80	Contents of A and Q shift right the number of shift counts in DISP Contents of A and Q shift right the number of shift counts in XR1 Contents of A and Q shift right the number of shift counts in XR2 Contents of A and Q shift right the number of shift counts in XR3
	<u>Rotate Right A & Q (RTE)</u>
18*X 19C0 1AC0 1BC0	Contents of A and Q rotate right the number of counts in DISP Contents of A and Q rotate right the number of counts in XR1 Contents of A and Q rotate right the number of counts in XR2 Contents of A and Q rotate right the number of counts in XR3
	<u>Branch Instructions</u>
	<u>Branch Or Skip On Condition (BSC or BOSC)</u>
48*X 4C*XXXXXX 4D*XXXXXX 4E*XXXXXX 4F*XXXXXX 4C*XXXXXX 4D*XXXXXX 4E*XXXXXX 4F*XXXXXX	Skip the next one-word instruction if ANY condition is sensed Branch to CSL at EA (Addr) on NO condition Branch to CSL at EA (Addr+XR1) on NO condition Branch to CSL at EA (Addr+XR2) on NO condition Branch to CSL at EA (Addr+XR3) on NO condition Branch to CSL at EA (V in CSL at Addr) on NO condition Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	<u>Branch And Store Instruction Register (BSI)</u>
40XX 41XX 42XX 43XX 44*XXXXXX 45*XXXXXX 46*XXXXXX 47*XXXXXX 44*XXXXXX 45*XXXXXX 46*XXXXXX 47*XXXXXX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1 Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1 Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1 Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (Addr+XR3) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1 If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1
	<u>Modify Index and Skip (MDX)</u>
70XX 71XX 72XX 73XX 74XXXXXXX 7500XXXX 7600XXXX 7700XXXX 74XXXXXXX 7580XXXX 7680XXXX 7780XXXX	ADD expanded DISP to I (no skip can occur) ADD expanded DISP to XR1 ADD expanded DISP to XR2 ADD expanded DISP to XR3 Add expanded positive DISP to CSL at Addr (Add to memory) Add Addr to XR1 Add Addr to XR2 Add Addr to XR3 Add expanded negative DISP to CSL at Addr (Add to Memory) Add V in CSL at Addr to XR1 Add V in CSL at Addr to XR2 Add V in CSL at Addr to XR3
	<u>Wait (WAIT)</u>
3000	WAIT until manual start or until completion of an Interrupt subroutine
	<u>Compare (CMP)</u>
80XX 81XX 82XX 83XX 8400XXXX 8500XXXX 8600XXXX 8700XXXX 8480XXXX 8580XXXX 8680XXXX 8780XXXX	Compare A with contents of CSL at EA (I+DISP) Compare A with contents of CSL at EA (XR1+DISP) Compare A with contents of CSL at EA (XR2+DISP) Compare A with contents of CSL at EA (XR3+DISP) Compare A with contents of CSL at EA (Addr) Compare A with contents of CSL at EA (Addr+XR1) Compare A with contents of CSL at EA (Addr+XR2) Compare A with contents of CSL at EA (Addr+XR3) Compare A with contents of CSL at EA (V in CSL at Addr) Compare A with contents of CSL at EA (V in CSL at "Addr+XR1") Compare A with contents of CSL at EA (V in CSL at "Addr+XR2") Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")
	<u>Double Compare (DCM)</u>
88XX 89XX 8AXX 8BXX 8C00XXXX 8D00XXXX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1 Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1 Compare A and Q with contents of CSL at EA (Addr) and EA+1 Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1

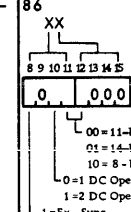
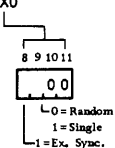
Input/Output Control Commands

Device/Function	IOCC			
	Address Word		Area, Function, and Modifier Word	
	Hex.		Hex.	
1816/1053				
Write	XXXX (Core Storage Addr)	1st-4th Printers- 5th-8th Printers-	09 79 02 04 08 10	-1st or 5th Printer -2nd or 6th Printer -3rd or 7th Printer -4th or 8th Printer
Sense Device	0000	1st-4th Printers- 5th-8th Printers-	0F 7F 02 04 08 10	-1st or 5th (03 if reset) -2nd or 6th (05 if reset) -3rd or 7th (09 if reset) -4th or 8th (11 if reset)
1816				
Read	XXXX (Core Storage Addr)	1st 1816- 2nd 1816-	0B02 7A02	Enter Input Character from Keyboard
Control	0000	1st 1816- 2nd 1816-	0C02 7C02	Place Keyboard in Proceed Status
1054/1055				
Read	XXXX (Core Storage Addr)	Read to Core-	1A00	
Write	XXXX (Core Storage Addr)	Punch from Core-	1900	
Control	0000	Read to Buffer-	1C10	-Initiate Reader Service Response Interrupt
Sense Device	0000	1054/1055-	1E00 01	-Reset Indicators
1442				
Initialize Read	XXXX (Table Addr)	1st 1442- 2nd 1442-	16 8D 00 01	-Card Image -Packed Mode
Initialize Write	XXXX (Table Addr)	1st 1442- 2nd 1442-	1500 8D00	Punch Core Image to Card Columns
Control	0000	1st 1442- 2nd 1442-	14 8C 02 80 82	-Feed Cycle -Stacker Select -Feed Cycle & Stacker Select
Sense Device	0000	1st 1442- 2nd 1442-	1700 8F00 01	-Reset Indicators
1443				
Initialize Write	XXXX (Table Addr)		3500 01	-Suppress Space After Print
Control	XX00 (Carriage Control Character)	Carriage Control-	3400	
Sense Device	0000	1443-	3700 01	-Reset Indicators
1627				
Write	XXXX (Core Storage Addr)	1627-	2900	
Sense Device	0000	1627-	2F00 01	-Reset Indicators
1810				
Control "A" Models	00XX (Number of Cylinder Movements)	1st drive- 2nd drive- 3rd drive-	24 44 4C 00 04	-Carriage Forward -Carriage Backward
Control "B" Models	00XX (Cylinder Addr)	1st drive- 2nd drive- 3rd drive-	24 44 4C 00 01	-Seek Specified Addr -Restore to Home Position
Initialize Read (A or B Model)	XXXX (Table Addr)	1st drive- 2nd drive- 3rd drive-	26 46 4E 0 8 X	-Read into Core -Read Check -Disk Sector

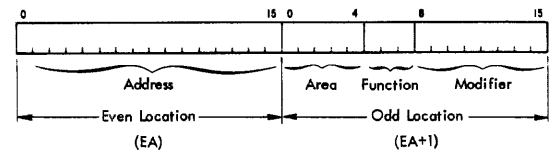
Device/Function	IOCC			
	Address Word		Area, Function, and Modifier Word	
	Hex.		Hex.	
1810 (Continued)				
Initialize Write (A or B Model)	XXXX (Table Addr)	1st drive- 2nd drive- 3rd drive-	25 45 4D 0X	-Disk Sector
Sense Device (A or B Model)	0000	1st drive- 2nd drive- 3rd drive-	2700 4700 4F00 01	-Reset Indicators
2401/2402				
Initialize Read	XXXX (Table Addr)	Tape to Core-	76XX 8 9 10 11 12 13 14 15 0 0	<ul style="list-style-type: none"> Parity* 0 = Odd 1 = Even 1 = Rd-while-correcting 1 = Packed Format* Density* 00 = 800 bpi 01 = 200 bpi 10 = 556 bpi 0 = Tape Unit 0, 1 = Tape Unit 1 *Ignored on 9-Track
Initialize Write	XXXX (Table Addr)	Core to Tape-	75XX	See Initialize Read (Bit 14 is not used)
Control	0000	Control-	74XX 8 9 10 11 12 13 14 15 0 0	<ul style="list-style-type: none"> 000 = Rewind Unload 001 = Write Tape Mark 010 = Erase 011 = Backspace 100 = Rewind Density 00 = 800 bpi 01 = 200 bpi 10 = 556 bpi 0 = Tape Unit 0, 1 = Tape Unit 1
Sense Device	0000		77XX 8 9 10 11 12 13 14 15 0 0, 0 0	<ul style="list-style-type: none"> 1 = Reset Indicators 1 = Operation Stop 0 = Sense DSW 1 = Channel Word Count 0 = Select Tape Unit 0 1 = Select Tape Unit 1
System/360 Adapter				
Initialize Write	XXXX (Table Addr)	Load Control Word to Adapter Buffer	6D00	
Initialize Read	XXXX (Table Addr)	Load Control Word to Adapter Buffer	6E00	
Sense Status	0000	Sense DSW-	6F00 1	-Reset Indicators
Word Count	0000	Present Word Count of Data Channel	6F80	
Control (Reset)	0000	Generate Reset to Adapter Controls	6C00	
Console (Area 00000)				
Data Entry Switches Sense	0000	Load Content of Switches to A-register	0740	
Read	XXXX (Core Storage Addr)	A-register to Core Storage	0240	
Program Switches Sense	0000	Load Content of Switches to A-register	0760	
Read	XXXX (Core Storage Addr)	A-register to Core Storage	0260	

Input/Output Control Commands

Device/Function	IOCC			
	Address Word		Area, Function, and Modifier Word	
	Hex.		Hex.	
Console (Area 0000) Continued				
Interrupt (Console) Sense	0000	Load Indicator Status to A-register	07C0 1	-Reset Indicator
Operations Monitor Control	0000	Reset Timer	04E1	
Interval Timers Sense	0000	Load Indicator Status to A-register	0720 1	-Reset Indicator
Control	X000 	Start or Stop Timer	0420	
Interrupt Mask Register Control	XXXX (Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9) 1-bit = mask 0-bit = unmask	Levels 0-13- Levels 14-23-	0480 0481	
Program Interrupt Control	XXXX (Generate Interrupt with 1-bit. Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9.)	Levels 0-13- Levels 14-23-	04A0 04A1	
Digital Input				
Direct Program Control Read	XXXX (Addr to Store Digit Input Group)	DI or PI Group to Core Storage	5A XX	-DI Addr 40 thru 7F or PI Addr 02 thru 19
Sense Device	0000	DSW, DI, or PISW A-register	5F 00 01 XX	-DSW -DSW, Reset Indicators -DI Addr 40 thru 7F or PISW Addr 02 thru 19
Control	0000	Generate Reset to DI Controls	5C20	
Data Channel Control Initialize Read	XXXX (Addr of Data Table)	Set up DC Controls for Transfer of Data	5E X0 	
Analog Input				
Direct Program Control Write	XXXX (Mpx Addr Location)	AI- AIE-	51 81	Analog Input to ADC 
Read	XXXX (Addr to Store ADC Reading)	AI- AIE-	52 82	ADC to Core 00 80 -Sequential Programmed Operation
Control	0000	AI- AIE-	5400 8400	Reset Controls and Registers
Sense Device	0000	AI- AIE-	57 87	0 8 -AI 1 -Comparator -Reset Indicators

Device/Function	IOCC			
	Address Word		Area, Function, and Modifier Word	
	Hex.		Hex.	
Analog Input Continued				
Data Channel Control Initialize Write	XXXX (First Mpx Addr Table Location)	AI- AIE-	5500 8500	(Set up DC for Transfer of Mpx Addr and Limit Words)
Initialize Read	XXXX (First Data Table Addr)	AI- AIE-	56 86	
Digital and Analog Output				
Direct Program Control Write	XXXX (Addr of Output Data)	Core Storage to DAO Device	61 XX	-DAO Register Addr 00 thru 7F
Control	0000		64 20 40 80	-Reset DAO Controls -Initiate Simultaneous Transfer from Registers -Start Pulse Output Timer
Sense Device	0000	DSW to A A-register	6700 01	-Reset Indicators
Data Channel Control Initialize Write	XXXX (Addr of Data Table)	Set up DC Controls to Transfer Data	65 X0 	

IOCC Format



Interrupts

Interrupt	Priority Level	Core Storage Location		ILSW	
		Decimal	Hex.		
Internal	1	8	8	Basic	
Trace	26	9	9		
** CE	27	10	A		
*External 0	2	11	B		
1	3	12	C		
2	4	13	D		
3	5	14	E		
4	6	15	F		
5	7	16	10		
6	8	17	11		
7	9	18	12		
8	10	19	13		
9	11	20	14		
10	12	21	15		
11	13	22	16		
12	14	23	17		
13	15	24	18		
14	16	25	19		Special Feature Group 1
15	17	26	1A		
16	18	27	1B		
17	19	28	1C		
18	20	29	1D		
19	21	30	1E		Special Feature Group 2
20	22	31	1F		
21	23	32	20		
22	24	33	21		
23	25	34	22		

* External Interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE Interrupt Stores the return link in core location 10 (decimal) and starts execution at core location 0001. Interrupts are prevented in the same manner as for the standard forced BSI.

Instruction Set

Hexadecimal	Branch Instructions	Symbol	Meaning
BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1	A	Accumulator
BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1	Q	Accumulator Extension
BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA+1	Addr	Contents of the address portion of a two-word instruction
BD80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1	CSL	Core storage location
BE80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1	DISP	Contents of the displacement portion of a one-word instruction
BF80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1	EA	Effective address (See Figure 1-)
		EA + 1	Next higher address from the effective address
		I	Contents of the Instruction Register
		V	Value
		XR1	Contents of Index Register 1
		XR2	Contents of Index Register 2
		XR3	Contents of Index Register 3
		X	Hexadecimal value can be 0-F
		*	Used for hexadecimal values that have limits
----- I/O Instructions -----			
Execute I/O (XIO)			
08XX	Execute IOCC in CSL at EA (H+DISP) and EA+1		
09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA+1		
0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA+1		
0BXX	Execute IOCC in CSL at EA (XR3+DISP) and EA+1		
0C00XXXX	Execute IOCC in CSL at EA (Addr) and EA+1		
0D00XXXX	Execute IOCC in CSL at EA (Addr+XR1) and EA+1		
0E00XXXX	Execute IOCC in CSL at EA (Addr+XR2) and EA+1		
0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA+1		
0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1		
0D80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1		
0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1		
0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1		

Effective Address Computation

Tag Bits	F = 0 (Direct Addressing)	F = 1, IA = 0 (Direct Addressing)	F = 1, IA = 1 (Indirect Addressing)
T = 00	EA = I + Disp	EA = Address	EA = C (Address)
T = 01	EA = XR1 + Disp	EA = Address + XR1	EA = C (Address + XR1)
T = 10	EA = XR2 + Disp	EA = Address + XR2	EA = C (Address + XR2)
T = 11	EA = XR3 + Disp	EA = Address + XR3	EA = C (Address + XR3)

Disp = Contents of Displacement field of instruction
C = Contents of location specified by Address or Address + XR1, 2 or 3

Device Status Words

Internal Interrupt ILSW

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15														
		<table border="1" style="width:100%; text-align:center;"> <tr> <td>0</td><td>1</td><td>2</td><td>3</td><td>3</td> </tr> <tr> <td>Invalid Op Code</td><td>Parity Error</td><td>Storage Protect Violation</td><td>CAR Check Error</td><td>(No others used.)</td> </tr> </table>					0	1	2	3	3	Invalid Op Code	Parity Error	Storage Protect Violation	CAR Check Error	(No others used.)															
0	1	2	3	3																											
Invalid Op Code	Parity Error	Storage Protect Violation	CAR Check Error	(No others used.)																											
0	Console Interrupt	Interrupt Request																													
	Interval Timers	Timer A	Timer B	Timer C																											
	Data Entry Switches	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15														
	Sense Switches	Sense			Program			CE Sense																							
1-15	1816 Printer-KeyBoard 1053 Printer -In First Group -In Second Group	* Printer Service Response	* Keyboard Service Response (1816)	* Keyboard Request (1816)	Printer Busy	Printer Not Ready	Keyboard Not Ready	Storage Protect Violation (1816)	Feed Check Read Station	Keyboard Parity Error (1816)	Printer Parity Error			†CE Busy	†CE Not Ready																
2-17	1442 Card Read Punch -First -Second		Error	Last Card	* Operation Complete	Parity Error	Storage Protect Violation	Feed Check Read Station						†CE Busy	†CE Not Ready	Busy	Not Ready														
3	1054/1055 Paper Tape Reader/Punch	PT Reader Any Error	* PT Reader Service Request	PT Punch Parity Error	* PT Punch Service Request	PT Reader Busy	PT Reader Not Ready	PT Punch Busy	PT Punch Not Ready	PT Reader Parity Error	PT Reader Storage Protect	†CE PT Reader Busy	†CE PT Reader Not Rdy	†CE PT Punch Busy	†CE PT Punch Not Rdy																
4-8-9	1810 Disk Storage "A" First Drive Second Drive Third Drive	Any Error	* Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun	†CE Not Ready	†CE Busy			Sector Count High	Sector Count Low														
4-8-9	1810 Disk Storage "B" First Drive Second Drive Third Drive	Any Error	* Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun	Seek Error	†CE Not Ready	†CE Busy	"C" Model Access	Sector Count High	Sector Count Low														
5	1627 Plotter	* Service Response	Parity Error											†CE Busy	†CE Not Ready	Busy	Not Ready														
6	1443 Printer	* Transfer Complete	Error	* Printer Complete	Channel 9	Channel 12	Channel 1	Parity				†CE Carriage Busy	†CE Printer Busy	†CE Printer Not Ready	Carriage Busy	Printer Busy	Printer Not Ready														
10-16	Analog Input -Basic -Expander	* End of Table	DPC SS Conv Complete	DPC Rly Conv Complete	Storage Protect Violation	Parity Control Error	Parity Data Error	* Overload	* Overlap Conflict	Cyc Steal SS, AMAR Busy	DPC Relay Busy						Any Error														
10-16	Comparator -AI Basic -AI Expander	* High Out of Limit	* Low Out of Limit	* Overload	AMAR SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR 1														
11	Digital Input	* Parity Error	* Storage Protect Violation	* DI Scan Complete	* Command Reject												DI Busy														
	PISW	Process Interrupt Points (Customer Assigned Groups)																													
12	Digital and Analog Output	* Parity Error	Pulse Output Timer	* D & A Out Scan Complete	* Command Reject	Data Channel Active											D/AO Busy														
13	S/360 Adapter	* Command Reject	1800 Command Stored	360 Command Stored	* Halt	* Data Check	* Storage Protect Violation	* Transfer End	* End of Table								360 Command Byte														
	Adapter Word Counter	Word Count (1's Complement)																													
14	Tape Control Unit		Tape Unit 1 Select	* Command Reject	* End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Data Bus Out or P-C Parity Error	Data Overrun Error	* Operation Complete	CE Diagnostic Indicator	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Busy or Rewind	Tape Busy or Not Ready														
	TCU Word Counter	Word Count																													

* Interrupt Conditions
† Active Only in CE Mode

