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IBM 1130 Typesetting System (RPQ)

This publication describes the IBM 1130 Typesetting System. The 1130 Typesetting System automates the hyphenation and justification functions of the printing and publishing industry. The IBM 1130 Computing System is described briefly, and the features and operations that comprise the 1130 Typesetting System are described in more detail.

PREFACE

This publication deals primarily with the special functions of the IBM 1130 Computing System that make it possible to automatically hyphenate and justify lines of text and to automatically provide the control codes required for the operation of linecaster machines.

This publication includes sufficient information about the standard IBM 1130 Computing System to provide a foundation for the special devices and operations included with the typesetting feature. For more detailed information about the IBM 1130 Computing System refer to the Systems Reference Library publication "IBM 1130 Functional Characteristics" (Form A26-5881).

First Edition

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CONTENTS

The IBM 1130 Typesetting System features an IBM 1130 Computing System, incorporating special circuitry into the 1130 system to provide the typesetting features. The IBM 1130 Typesetting System provides 8,192 sixteen-bit words of core storage and an additional 512,000 words of on-line disk storage capacity. Disk storage permits random or sequential access to data or programs.

The basic system includes an IBM 1131 Central Processing Unit with the special circuitry, and either an IBM 1442 Card Read Punch (Model 6 or 7) or an IBM 1134 Paper Tape Reader and an IBM 1055 Paper Tape Punch. Attached to the system, for the typesetting operations, will be at least one Teletype* High Speed Reader Set CX (CX) and at least one Teletype* High Speed Punch Set BRPE (BRPE). The IBM 1130 Typesetting System can accommodate up to 16 CX readers and up to 16 BRPE punches. The input tapes read by the CX readers and the output tapes punched by the BRPE punches are the advanced feed hole paper tape used exclusively by the printing industry.

Other applications are possible with the IBM 1130 Typesetting System.

Application

The IBM 1130 Typesetting System includes special circuitry added to the basic 1131 Central Processing Unit. With this circuitry, the system can prepare the paper tape that causes tape-controlled linecasting machines to set type for printing. Preparing the paper tape by means of a computer differs in several ways from preparing the tape manually. The following descriptions point out these differences.

Manual Preparation

Figure 1 shows the flow of work when the paper tape is prepared manually. At the left is the source document. An operator reads the manuscript and, using a keyboard-operated tape perforator, transcribes the text into punched holes in the paper tape. While doing so the operator examines each line and decides where to add extra spaces or hyphenate words to make all lines equal in length. This equalization, called justification, can add several seconds to the time required to punch the text of each line. The operator must also add the codes required to control the linecasting machines.

A complete story, or a desired portion of a story, is called a "take". When a take is complete, the tape is fed into the linecasting machine. The linecaster reads the tape and converts the punched hole information into type slugs (lines of type). The type slugs are combined into galleys for the printing process.

Computer Assisted Preparation

Figure 2 shows the work flow when text is processed by the 1130 computer. As in the manual method, an operator must transcribe the information from the manuscript into punched tape. However, the operator does not perform any hyphenation or justification for line length. Nor does the operator enter any control codes for the linecaster. The operator enters only the text and formatting control codes.

When the take is complete, the tape is fed into a tape reader, and the computer is signaled that a take is ready. The reader, under control of the computer, reads the tape information into the computer. The computer program divides the take into correct line length segments, hyphenating and justifying each line as required. As each line is processed, the computer adds the codes for control of

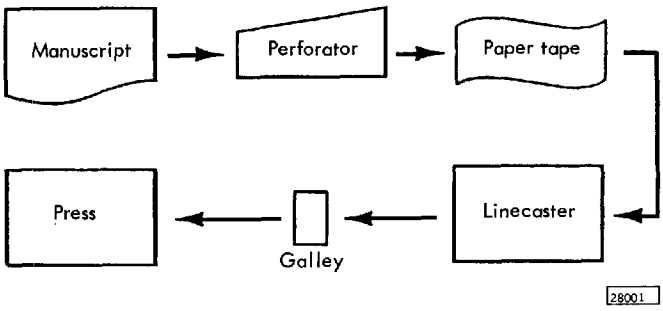

Figure 1. Manual Preparation

*Trademark of the Teletype Corporation

NOTE: The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

the linecaster. The resulting copy of the take is punched into a second paper tape by the paper tape punch. When the take is complete, the tape is fed into the linecaster. The linecaster reads the tape and converts the punched holes into type slugs.

Advantages

Using the 1130 Typesetting System provides advantages over the manual method of preparing paper tapes for linecasting machines because the computer performs the hyphenation, justification, and the entry of control codes automatically.

Because the computer performs the detail work of hyphenation and justification, a competent typist with relatively little additional training can operate the perforator. The manual operation, however, requires a skilled operator.

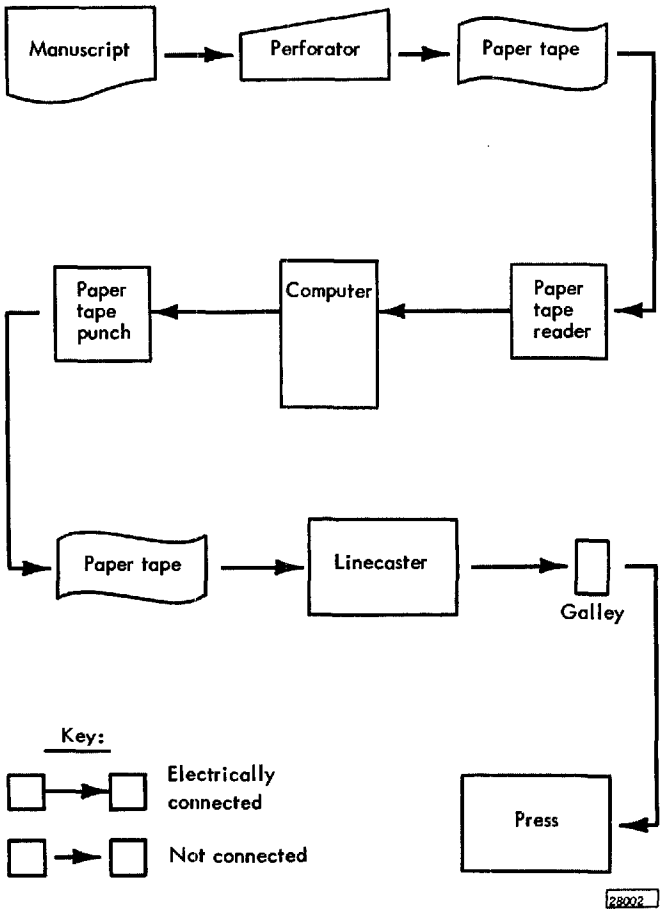

Figure 2. Computer Assisted Preparation

Because the computer relieves the operator of all decision making relative to hyphenation, justification, and linecaster control code entry, the time required to enter a take onto tape is significantly reduced.

In most cases the appearance of the final copy is improved by computer handling of the text.

Computer-assisted processing of a take can be subdivided into two general methods of tape handling: torn tape or allotting. The methods are similar. Only the transfer of tape between machines differs.

Torn Tape Method

The torn tape method (Figure 3) requires a manual distribution of tape takes. Each completed take is literally torn off at the output of each tape perforator. A take is manually fed into the tape reader and the computer is signaled that a take is ready. The IBM 1131 Central Processing Unit (CPU) processes the take. This procedure must be repeated for each take that is fed into the system. More than one reader could be used, but each reader would require manual loading of each take.

On the output side, the paper-tape punch output is torn off at the end of each take. These tape segments are distributed and manually loaded into the linecaster reading mechanisms. More than one punch could be used, but each take output would require manual handling.

Only one reader and one punch may be operated at any one time. However, they are completely overlapped so a maximum throughput of 12,000 lines per hour can be achieved (ignoring manual tape loading time).

Allotting Method

The allotting method (Figure 4) eliminates practically all of the manual tape handling. Multiple readers and punches are used. Each reader is placed beside its associated tape perforator with the tape from the perforator being loop fed into the reader. The only manual loading of tape is at the beginning of the operation.

The operator transcribes the text into punched tape, with the tape accumulating in the loop between the perforator and the reader. The computer is signaled when the take is complete and processes the entire take. The reader reads tape as required until the end-of-take code character is detected.

On the output side, the punch is mounted directly on or near the linecaster and the tape loop is fed directly into the linecaster reading mechanism.

Again, the only manual loading of tape required is at the beginning of the operation.

The computer processes and punches out the take. The linecaster reads the output tape as long as tape is available, stopping when the tight tape contact is operated.

Each input and output station has a similar arrangement. Although the computer will read from only one reader at a time, requests for service from other reader stations will be "remembered" by the computer and will be serviced in the order determined by the operating program. Similarly only one punch will be operated at a time. Normal program routines will operate one reader and one punch simultaneously at their rated speeds of 110 characters per second with ample time for the operating program.

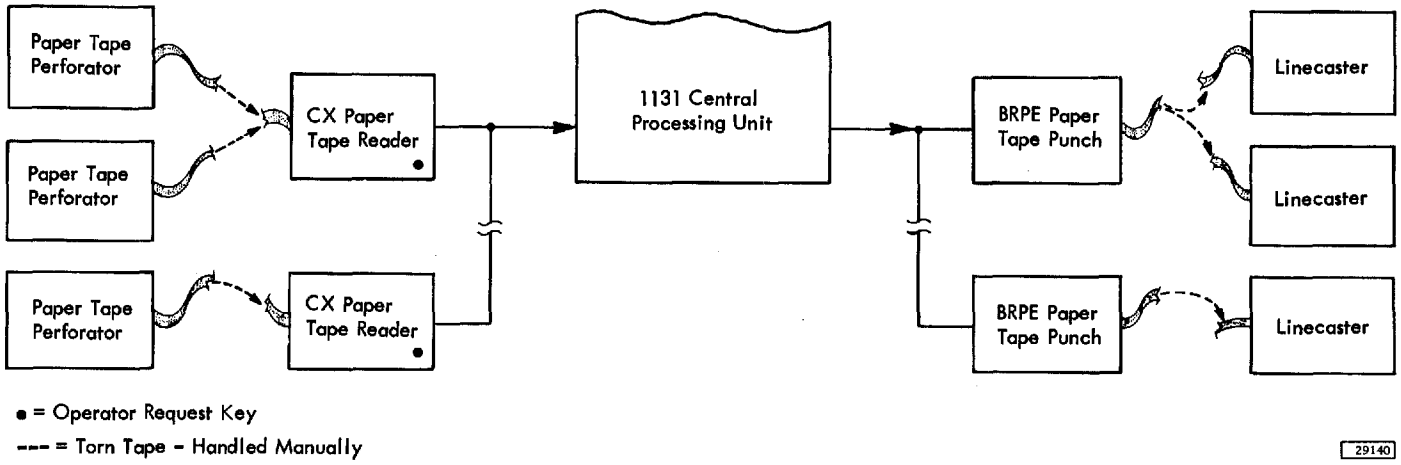

Figure 3. Torn Tape Method

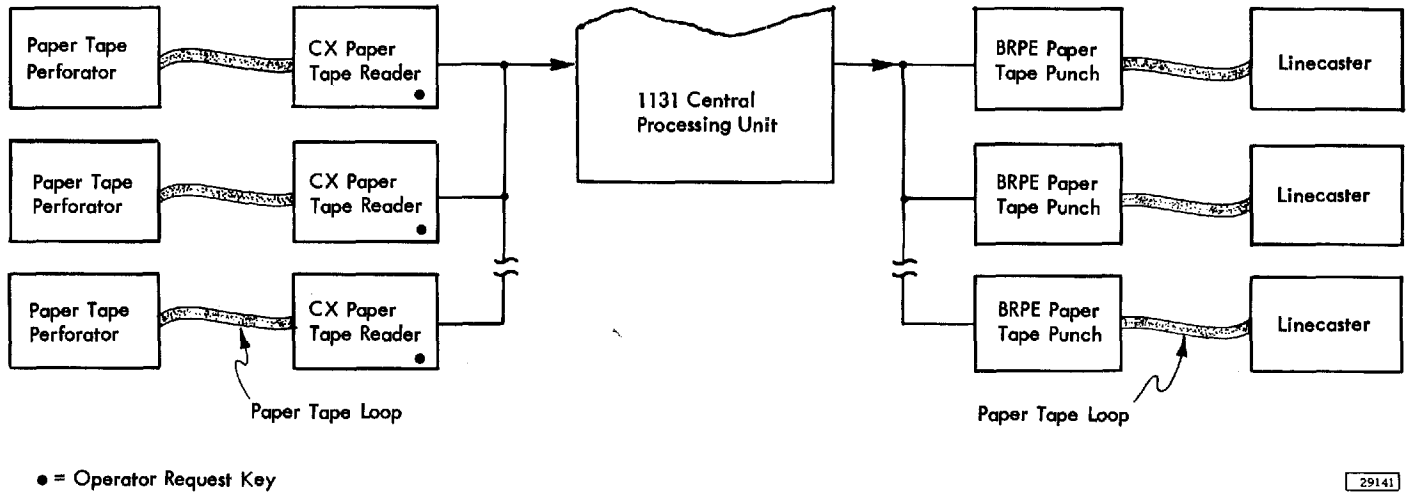

Figure 4. Allotting Method

SYSTEM UNITS

The IBM 1130 Typesetting System consists of an IBM 1131 Model 2B Central Processing Unit (Figure 5) and either an IBM 1442 Card Read Punch or an IBM 1134 Paper Tape Reader and an IBM 1055 Paper Tape Punch. Attached to the Central Processing Unit (CPU) will be one or more (up to 16) Teletype High Speed Tape Reader Sets CX and one or more (up to 16) Teletype High Speed Punch Sets BRPE.

CENTRAL PROCESSING UNIT (CPU)

The 1130 Typesetting System (Figure 6) can perform the typesetting function because of the programming capability of the 1131 CPU and the special circuitry provided. The CPU is the center of the system, containing the paths for all data passing through the system. The CPU controls all input and output (I/O) units attached to the system and contains the logic circuits required to process the data. Main storage and the disk storage device with the CPU provide ample storage capacity for programs and data.

Special circuits required by the typesetting function are provided. Included are the controls for the CX readers and the BRPE punches as well as circuits for handling the data between these units and the CPU.

Core Storage

The CPU main storage uses magnetic cores for data and program instruction storage. Core storage capacity is 8,192 sixteen-bit words. Each word is individually addressable. Words may be coupled and operated on as double (32-bit) words when required. Data is recorded and processed in fixed-point binary form. The largest possible positive number is $2^{31}-1$; the largest negative number is -2^{31}.

The cycle time to access and replace a word in core storage is 3.6 microseconds (μsec).

Disk Storage

Disk storage is housed within the CPU and consists of a single disk drive and a removable disk cartridge. The disk drive provides random or sequential access to data storage. Because one disk cartridge is easily replaced with another, virtually unlimited storage capacity is available. Data and program routines can be put on-line as needed.

The capacity of a disk is 512,000 sixteen-bit words. The data transfer rate is 36,000 words per second, or 27.8 μsec per word.

Console

The Console is an integral part of the IBM 1131 Central Processing Unit and consists of the input keyboard, console printer, display panel, function switches and lights, and Console Entry switches.

IBM 1442 CARD READ PUNCH

The IBM 1442 Card Read Punch, Model 6 or Model 7, (Figure 7) provides card input and output for the IBM 1130 Typesetting System.

The 1442 is a single unit that processes cards serially, column-by-column, from a single supply hopper. Each card passes a read station and then a punch station. This arrangement of stations permits cards to be read, punched, or read and punched.

Maximum machines speeds are:

Model 6
- Read - 300 cards per minute
- Punch - 80 columns per second

Model 7
- Read - 400 cards per minute
- Punch - 160 columns per second

Card reading and card punching are controlled by the operating program stored in the CPU.

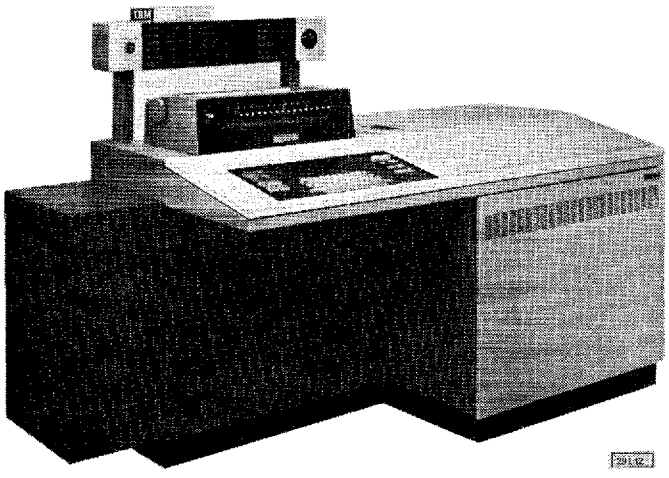

Figure 5. IBM 1131 Central Processing Unit (Typesetting)

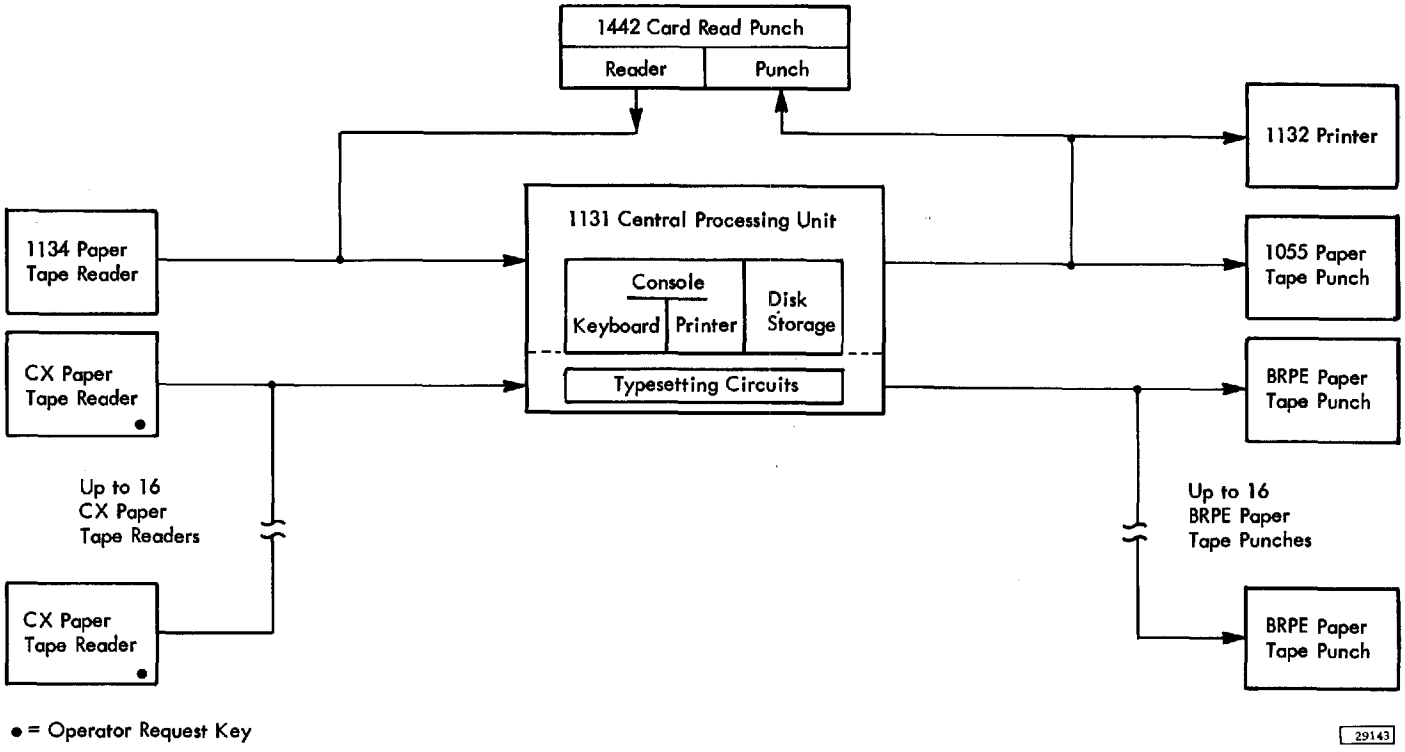

Figure 6. 1130 Typesetting Configuration

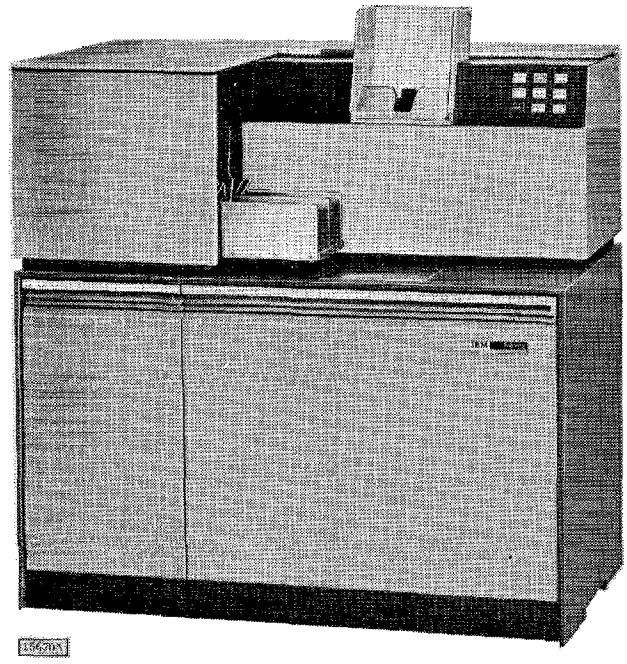

Figure 7. IBM 1442 Card Read Punch

IBM 1134 PAPER TAPE READER

The IBM 1134 Paper Tape Reader (Figure 8) provides paper tape input to the IBM 1130 Typesetting System. The 1134 is capable of reading perforated tape at speeds up to 60 characters per second. The reader dynamically senses the presence and absence of holes in the tape, thus ensuring positive identification of a hole or space. Tape motion and tape reading are controlled by the operating program in the CPU. Each character read from tape is stored in one addressed core storage location. The character placed in storage is an image of the holes in the tape. Any translation of characters must be accomplished through programming.

IBM 1055 PAPER TAPE PUNCH

The IBM 1055 Paper Tape Punch (Figure 9) provides paper tape output from the IBM 1130 Typesetting System. The 1055 is capable of punching paper tape at speeds up to 14.8 characters per second. Tape

punching is controlled by the operating program in the CPU. Each character punched represents one addressed core storage location. The character code punched into tape is an image of the core storage word. Any translation of characters must be accomplished through programming.

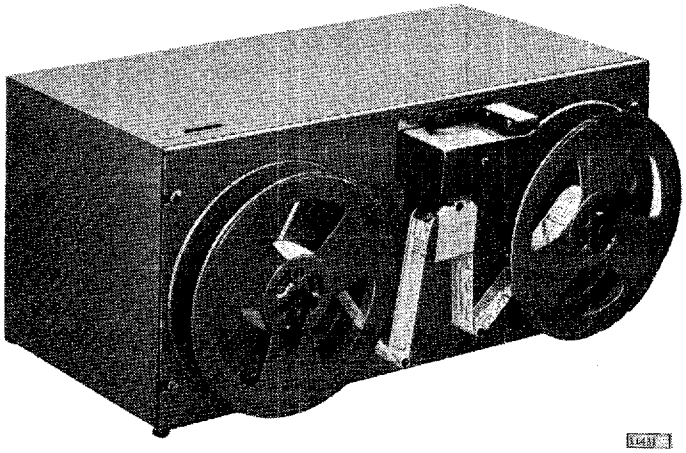

Figure 8. IBM 1134 Paper Tape Reader

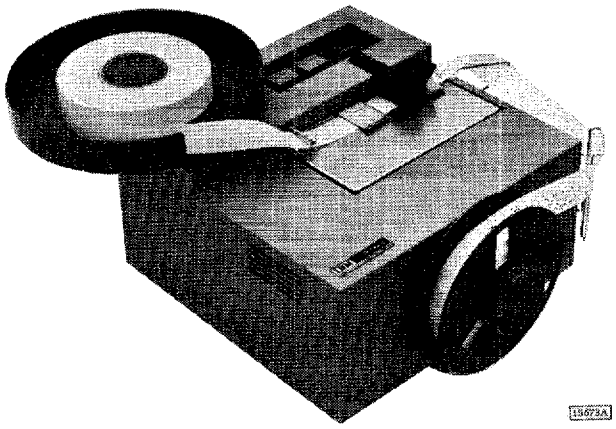

Figure 9. IBM 1055 Paper Tape Punch

IBM 1132 PRINTER

The 1132 Printer (Figure 10) provides printed output for the 1130 Typesetting System at maximum rates of 82 lines per minute (lpm) for alphameric printing and 110 lpm for numeric printing. The print line is 120 print positions long; horizontal spacing is ten characters per inch. Vertical spacing of six or eight lines per inch can be selected by the operator.

The 1132 contains a printwheel with 48 alphabetic, numeric, and special characters for each of the 120 printing positions. Special (FORTRAN) characters are as follows:

& - / . $, * ( ) ' + =

Each wheel rotates continuously and moves forward to print when the data in the output record specifies that the character to be printed is in the print position. Thus, all similar characters for the entire line are printed on the same cycle. Forty-eight cycles are required to print the complete line.

Forms control is provided through a tape-controlled carriage that uses the standard IBM carriage tape. Channels 1 through 6, 9, and 12 are available to the stored program.

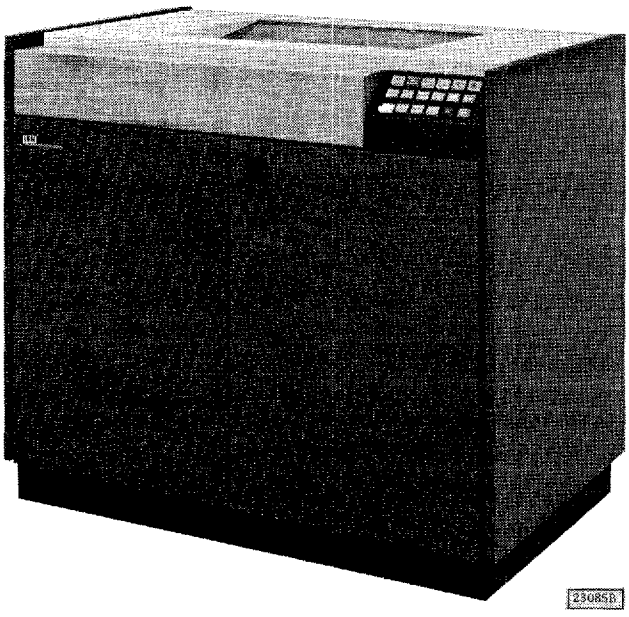

Figure 10. IBM 1132 Printer

TELETYPE EQUIPMENT

Teletype High Speed Reader Sets CX and Teletype High Speed Punch Sets BRPE are used as input and output processing devices for the 1130 Typesetting System. The readers and punches normally process the six-channel advanced feed hole paper tape used exclusively in the printing industry. The system can be modified to allow the readers and punches to process six- or eight-channel data interchangeably (See Additional Features). The 1131 CPU provides the interface to match the signals between the Teletype equipment and the CPU.

The customer is responsible for providing, modifying, and maintaining the Teletype equipment. The customer must supply the cables connecting the Teletype equipment with the 1131 CPU. The cables can be purchased locally, or they can be purchased from IBM.

Teletype High Speed Reader Set CX

The Teletype High Speed Reader Set CX is used to read a story or take from perforated paper tape and thus provides the input data to the 1130 Typesetting System. Up to 16 readers can be attached to the 1131 CPU. A CX can read tape at speeds up to 107 characters per second. Tape motion and tape reading are controlled by the operating program in the CPU. Each character read from tape is stored in one addressed core storage location. The character placed in storage is an image of the holes in the tape.

Each CX reader must be modified by the addition of a normally open operator request switch. This switch is used to signal the CPU that a take is ready to be read in from the associated reader.

Teletype High Speed Punch Set BRPE

The Teletype High Speed Punch Set BRPE (BRPE) is used to punch the computer-processed take into paper tape and thus provides the output data from the 1130 Typesetting System. Up to 16 punches can be attached to the 1131 CPU. A BRPE can punch tape at speeds up to 110 characters per second. Tape punching is controlled by the operating program in the CPU. Each character punched into tape is from one addressed core storage location. The character punched into tape is an image of the character in storage.

ADDITIONAL FEATURES

The following additional special features can be added to the 1130 Typesetting System.

Linecaster Contact Sense (LCCS)

This feature provides the 1130 Typesetting System with the ability to monitor the typecasting workload on each linecaster.

A contact is added to each linecaster to signal the CPU each time that a linecaster casts a line of type. By CPU programming, an active record can be maintained for each linecaster. The number of lines sent to a particular linecaster can be recorded and decremented for each line cast. Thus, a linecaster that is not operating can be detected by the computer program, and takes can be directed to another linecaster.

This positive control of linecaster activity provides automatic, efficient, and economical production.

Six- or Eight-Channel Paper Tape

The addition of this special feature expands the interface channels from six to eight. Effectively this allows the CX readers and BRPE punches to process six- or eight-channel data interchangeably. Data can be read in any code. Parity checking is not provided. Detection of either a six- or eight-channel device being connected to the interface is not provided.

If both six- and eight-channel readers are connected to the system simultaneously, six-channel CX readers must have the seventh and eighth channel contacts disconnected.

This desired model of readers and punches must be furnished by the customer.

Remote Power Control

The addition of this feature allows operation of a BRPE punch motor only when the punch is selected.

FEATURE SUMMARY

The IBM 1130 Typesetting System consists of special features added to the IBM 1131 Central Processing Unit. The Typesetting System is available on a Request for Price Quotation (RPQ) basis. Figure 11 provides information about each RPQ device that is used in the 1130 Typesetting System.

RPQ Number	Name	Description	Prerequisites
834398	Basic Interface	Provides basic I/O circuits for various I/O attachment RPQ's. Useful only as a prerequisite; does not provide any I/O capabilities by itself.	None
834399	Paper Tape Attachment	Permits attachment of one Teletype CX 6-channel paper tape reader and/or one Teletype BRPE 6-channel paper tape punch.	1. 834398 2. Customer must supply a single-pole, normally open, momentarily closed switch connected to positions 35 and 36 in the reader to indicate that data is ready to be transferred to the CPU.
834400	Multiple Capability	Permits attachment of more than one reader (if this RPQ is accompanied by 834401) and/or more than one punch (if this RPQ is accompanied by 834402).	834399
834401	Additional Paper Tape Reader Interface	Permits attachment of more than one reader. One 834401 is required for each reader after the first.	For up to 8 readers: 834400 For up to 16 readers: 834400 and E36610
834402	Additional Paper Tape Punch Interface	Permits attachment of more than one punch. One 834402 is required for each punch after the first.	For up to 8 punches: 834400 For up to 16 punches: 834400 and E36610
E36610	Second Expansion	Permits attachment of more than 8 readers and/or more than 8 punches.	834401 (for readers) and/or 834402 (for punches)
M29025	8-channel Tape	Permits attachment of 8-channel readers and/or punches.	1. 834399 2. If 6- and 8-channel readers are both used, disconnect the wires of the unused contacts of the 6-channel readers.
834491	Linecaster Contact Sense	Causes an interrupt request to occur each time a line of type is cast.	1. 834399 and E36610 2. Customer must provide normally open contacts that close each time a line of type is cast.
833150	Cables	Provides cables for any of the above RPQ's if customer chooses not to supply cables.	None
W22929	Remote Power Control	Causes BRPE punch motor to operate only when the punch is selected	1. 834398 2. 834399 3. 834402

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Figure 11. RPQ Summary

The ability of the 1130 Typesetting System to perform the processing of data for typesetting is due to the 1131 Central Processing Unit and the special circuits provided. The CPU is the center of the system. It provides the control for all input and output units and performs the processing of the data being passed through the system. The descriptions that follow concern the storage of data and program instructions; the formats in which data and instructions are stored and used; functions of CPU registers; and the aspects of addressing core storage, disk storage, and attached input/output (I/O) units. For additional information about 1131 operations, other than those specifically provided for typesetting, see the Systems Reference Library publication "IBM 1131 Functional Characteristics" (Form A26-5881).

CORE STORAGE

The 1131 main storage uses magnetic cores for data and program instruction storage. Core storage capacity is 8,192 sixteen-bit words. Each 16-bit word has two additional bits, called parity bits, which are used for internal data checking only.

The main storage memory cycle (the time required to place a word in core storage or retrieve it from core storage) is 3.6 μsec.

Addressing

Each 16-bit word in core storage is locatable through an address that specifies the position of the word. Addresses range from 0000 to 8191. The high-order address is contiguous with the low-order address, which provides for "wrap-around" addressing. "Wrap-around" means that in sequential processing of addresses, 8191 is followed by 0000 without further specification by the CPU.

Reserved Storage Locations

The following are core storage decimal addresses reserved for specific purposes and not available for general data storage.

Tag Bits	Core Storage Address	Description
00	--	Displacement
01	0001	Index Register 1
10	0002	Index Register 2
11	0003	Index Register 3
--	0008 - 0013	Interrupt Addresses
--	0032 - 0039	Printer Scan Field

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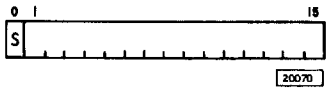
DATA FORMAT

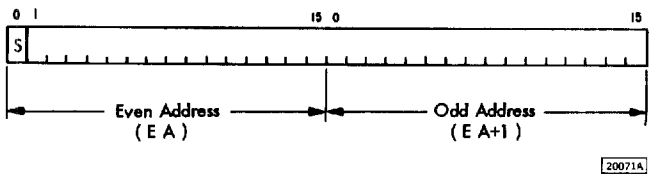
Data in the 1131 CPU is in fixed-point binary form. Each number is treated as a signed integer; positive numbers are in true binary with a sign of 0, and negative numbers must be stored and operated upon in 2's complement form with a sign bit of 1. Complementing is done by inverting each bit of the number (including the sign bit) and adding 1 to the low-order bit. The following example illustrates this.

Positive number	0001101001001100
Inverted	1110010110110011
Add 1	1
Resulting negative number	1110010110110100

Data is stored as either a single precision word or a double precision word. A single precision data word comprises 16 bits; bit positions are numbered 0 to 15 from left to right. The high-order bit (0) is the sign position.



The largest base-10 (decimal) values of single precision words are +32,767 and -32,768. A double precision data word contains 32 bits and is composed of two sequential single precision words. The high-order bit (0) is the sign position.



A double precision data word is addressed by the leftmost word, which must have an even address.

The highest base-10 values of double precision data words are +2,147,483,647 and -2,147,483,648. The largest positive number ($2^{31}-1$) is one less than the largest negative number (2^{31}) because the sign (0 for plus, 1 for minus) is, arithmetically, part of the number.

All CPU storage is in binary form, and internal addressing is in 16-bit binary notation. Because of the ease of operation with 16-bit words in the hexadecimal number system (base 16), all programming systems for the IBM 1130 Computing System use this notation.

DISK STORAGE

Disk storage provides the IBM 1130 Computing System with low-cost random or sequential access data storage. On-line data capacity is 512,000 words; off-line capacity is virtually unlimited because the interchangeable disk cartridge is easily removed and replaced with another. Thus, the large storage capacity, comparable to that of magnetic tape, coupled with the unique advantage of random access, affords the 1130 Typesetting System great flexibility in handling typesetting, accounting, and commercial applications.

Disk storage for the 1130 System is contained in the CPU frame and is connected to the CPU by the attachment circuitry. It is composed of two components: the disk and drive assembly and the access mechanism.

Disk Assembly

The disk assembly (Figure 12) is a single disk drive, completely enclosed in a protective housing, or cartridge. The recording medium is an oxide-coated disk that provides two surfaces for the magnetic recording of data. The disk drive rotates at the rate of 1500 revolutions per minute.

Access Mechanism

The disk storage access mechanism has two horizontal arms. Each arm has a magnetic read/write head, and each head is positioned to read or write on the corresponding disk surface as the access arms straddle the disk in the manner of a large tuning fork. The entire assembly moves horizontally forward and backward, so that the heads have access to the entire recording area.

The access mechanism is positioned automatically, at the home position (outside cylinder) when the disk cartridge is inserted.

Disk Organization and Capacity

The access mechanism is moved back and forth by program instructions and can be placed in any one of 200 positions, from a point near the periphery of the disk to a point near the center of the disk. The heads can read or write in a circular pattern on both surfaces of the disk, as it revolves. These circular patterns of data are called tracks. The track on the upper surface of the disk and the corresponding track on the lower surface, either of which can be read or written while the access mechanism is in the same position, are called a cylinder. The total number of cylinders is 203. However, three of the cylinders are used as spares to ensure that 200 cylinders are available for customer use. Figure 13 shows the innermost and outermost cylinders of two tracks each. To complete the picture, the intermediate cylinders, or pairs of tracks, should be visualized; they were omitted for the sake of clarity of the diagram.

For convenience in transferring data between the CPU core storage and disk storage, each track is divided into four equal segments called sectors. Sectors are numbered by the cylinder, from 0 through 7, as shown in Figure 14. Sectors 0 - 3 divide the upper surface track, and sectors 4 - 7, the lower. A sector contains 321 data words and is the largest segment of data that can be read or written with a single instruction.

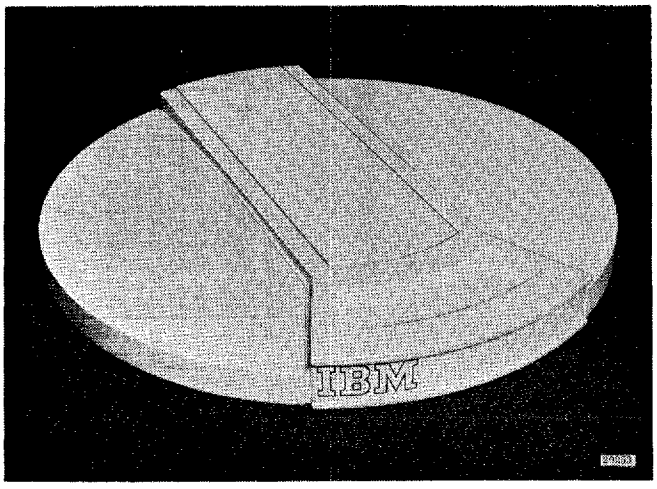
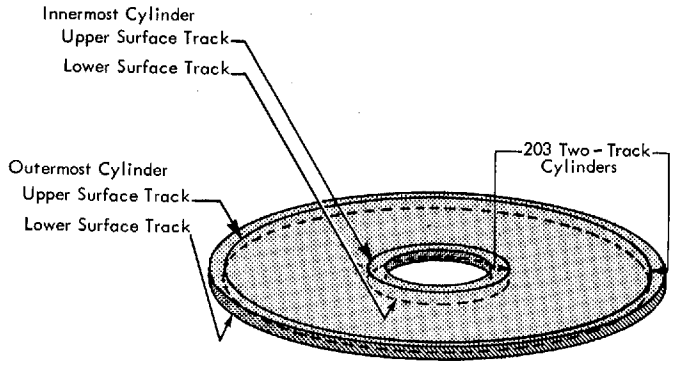


Figure 12. Disk Assembly Cartridge



NOTE: The thickness of the disk has been greatly exaggerated in order to show the relative positions of the upper and lower surface tracks.

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Figure 13. Disk Storage Cylinder Schematic

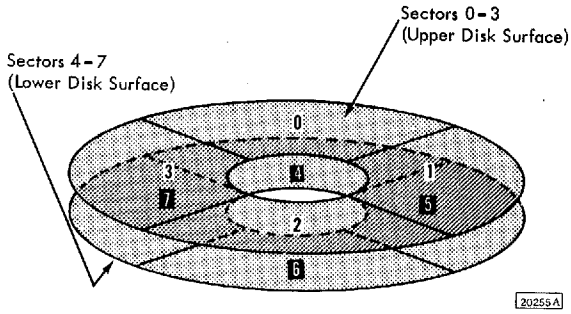

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Figure 14. Disk Storage Sector Numbers

In the programs and programming systems provided by IBM, e.g., the monitor system and its programs, the first word of a 321-word sector is used for cylinder sector number.

Therefore, the first word of the sector cannot be used by the programmer if the assembler program or other components of the monitor system are to be used.

A disk storage word comprises 16 data bits and four check and space bits.

The following illustration shows the organizational components of disk storage. Note that capacities are based upon the 320-word sector.

No of / Per	Word	Sector	Track	Cylinder	Disk
Bits	16	5,120	20,480	40,960	8,192,000
Data Words		320	1,280	2,560	512,000
Sectors			4	8	1,600
Tracks				2	400
Cylinders					200

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Timing

Timing considerations of disk storage operation involve three elements: access time, reading and writing data, and the time during which the CPU is tied up.

Access: The access mechanism moves in increments of two cylinders at the rate of 15 ms per increment. Thus, in the formula that follows, the number of cylinders (N) must be even. (The next higher even number is used if an odd number of cylinders is specified.) During the 20 ms stabilization period that follows the last incremental movement, a Read or Write instruction can be given and will be started at the end of the stabilization period.

$$\text{Access time (ms)} = 7.5(N) + 20$$

Read/Write: Reading or writing of data in disk storage is at the rate of 27.8 μsec per word. Average rotational delay time is 20 ms, based on 1500 rpm, or 40 ms per revolution. Thus, a sector can be read or written in an average of 30 ms. Although there are no timing considerations for head switching there are programming considerations in consecutive sector operations because there is an interval of over 420 μsec between sectors; the interval is increased by 27.8 μsec for each word less than 321 read or written.

A full cylinder of eight 321-word sectors can be read or written in 100 ms because the rotational delay is required for only the first sector.

CPU Time: An interrupt in a disk storage operation occurs only at the end of the seek or read/write operation. This means that once the instruction is initiated, disk storage operation is virtually independent of the CPU. As data is being read or written a cycle is literally "stolen" from the CPU operation in progress every 27.8 μsec for the transmission of the next word. Thus, except for the normal instruction times, the CPU is busy only 14 ms of the 100 ms required to read or write a full cylinder. The remaining 86 ms are available for other program operations.

Data Checking

Data is checked on each transmission between core storage and disk storage. The number of bits of each word is divided by four as the word leaves core storage, and the number of bits necessary to make the division even (modulo 4) is added to the end of the word. The modulo 4 test is performed again each time a word is written in disk storage or read from it. A word that is not modulo 4 causes the data check bit to be set in the disk storage device status word (DSW). (See Device Status Word.)

CONSOLE

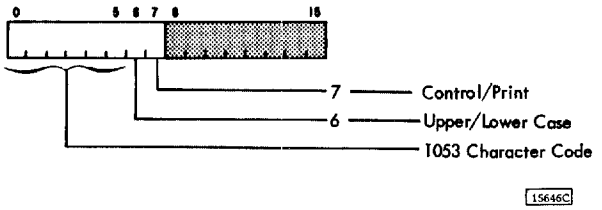
While the keyboard and console printer are usually considered as one unit, control of each of them by the operator and by the stored program is discrete. For this reason, the functional description and programmed operation of each unit is considered separately in the sections that follow.

Console Printer Functional Description

The console printer provides output at a maximum rate of 15.5 characters per second. Data to be printed is transferred from core storage to the console printer by direct program control.

Data characters and control characters (space, tabulate, etc.) are sent to the console printer by means of the Write command. Because control characters and data characters are sent in the same manner, the message to be printed contains a mixture of data characters and control characters in the sequence necessary to give the desired formatted output.

The character format within a core storage word to be transmitted to the console printer is:



Each word transmitted to the console printer contains one data character or one control character.

Data Coding

Data to be printed is coded by the program into the console printer code. Figure 15 shows the characters which can be printed by the standard print element.

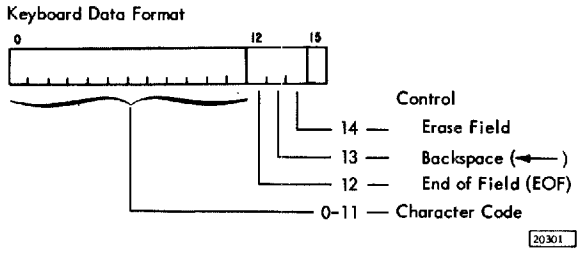
The data-character code also contains (in B6) the information as to whether the character is an upper-case (UC) shift or lower-case (LC) shift character. The printer shifts automatically as required for each data character.

A printer Write command is modified by the B7 position of the output character word. If B7 equals one, the Write command to the printer is interpreted as a control function. If B7 equals zero, the Write command is interpreted as a print function.

The codes for console printer control functions are shown in Figure 16.

Keyboard Functional Description

The input speed of the keyboard (Figure 17) is limited only by the speed of the operator. Keyboard entries are not automatically printed unless the CPU is programmed to provide an output of the entry on the printer. The keyboard emits a coded character for each key struck by the operator. These characters are related to IBM card coding. Striking the A character key places bits in positions 0 and 3 of the CPU word; striking the I character key places bits in positions 0 and 11 of the word; striking a 9 character places a bit in position 11 of the word; etc.



The two-position Console/Keyboard switch indicates to the program the desired source of the console input data, either the keyboard or the console entry switches.

Console Entry Switches

These 16 toggle switches are used to set up data or instructions to be entered into core storage. Each switch represents a bit position in a 16-bit word.

Character Code Bits						U/L Case		Ctrl
B0	B1	B2	B3	B4	B5	B6=0 LC	B6=1 UC	B7
0	0	1	1	1	1	A	A	0
0	0	0	1	1	0	B	B	0
0	0	0	1	1	1	C	C	0
0	0	1	1	0	0	D	D	0
0	0	1	1	0	1	E	E	0
0	0	0	1	0	0	F	F	0
0	0	0	1	0	1	G	G	0
0	0	1	0	0	1	H	H	0
0	0	1	0	0	0	I	I	0
0	1	1	1	1	1	J	J	0
0	1	0	1	1	0	K	K	0
0	1	0	1	1	1	L	L	0
0	1	1	1	0	0	M	M	0
0	1	1	1	0	1	N	N	0
0	1	0	1	0	0	O	O	0
0	1	0	1	0	1	P	P	0
0	1	1	0	0	1	Q	Q	0
0	1	1	0	0	0	R	R	0
1	0	0	1	1	0	S	S	0
1	0	0	1	1	1	T	T	0
1	0	1	1	0	0	U	U	0
1	0	1	1	0	1	V	V	0
1	0	0	1	0	0	W	W	0
1	0	0	1	0	1	X	X	0
1	0	1	0	0	1	Y	Y	0
1	0	1	0	0	0	Z	Z	0
1	1	1	1	1	1	1	(	0
1	1	0	1	1	0	2	+	0
1	1	0	1	1	1	3	<	0
1	1	1	1	0	0	4	¬	0
1	1	1	1	0	1	5	)	0
1	1	0	1	0	0	6	;	0
1	1	0	1	0	1	7	*	0
1	1	1	0	0	1	8	'	0
1	1	1	0	0	0	9	"	0
1	1	0	0	0	1	0	|	0
1	1	0	0	0	0	#	=	0
1	0	1	1	1	1	/	-	0
1	0	0	0	0	1	-	?	0
1	0	0	0	0	0	,	:	0
0	1	0	0	0	1	&	>	0
0	1	0	0	0	0	$	.	0
0	0	0	0	0	1	@	%	0
0	0	0	0	0	0	.	¢	0

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Figure 15. Console Printer Character Coding

Function	0 1 2 3 4 5 6 7 8 15
Carrier Return	1 0 0 0 0 0 0 1
Tabulate	0 1 0 0 0 0 0 1
Space	0 0 1 0 0 0 0 1
Backspace	0 0 0 1 0 0 0 1
Shift to Red*	0 0 0 0 1 0 0 1
Shift to Black*	0 0 0 0 0 1 0 1
Line Feed	0 0 0 0 0 0 1 1

*May be done concurrently with any other function.

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Figure 16. Console Printer Control Functions

Console Display Panel

The contents of the registers within the computer are displayed on the console panel (Figure 18) by means of small incandescent lights. Each bit in each register position is represented by a light. The light is on when the bit which it represents is present in the word displayed.

REGISTERS

The CPU has auxiliary storage areas, called registers, that are used to store data during the performance of operations directed by the stored program. Each register has a distinct purpose and is concerned with a specific type of data. Closely interrelated, they provide the CPU with the necessary functions to provide the results required.

Index Registers

Index registers are located in core storage and are used to contain data added to an instruction to provide an effective address.

The three index registers, located in core storage, are used to contain data that is added to an instruction to provide an effective address. Their instruction coding and storage locations are:

Register Number	Instruction Code in Bits 6 and 7	Core Storage Location
1	01	0001
2	10	0002
3	11	0003

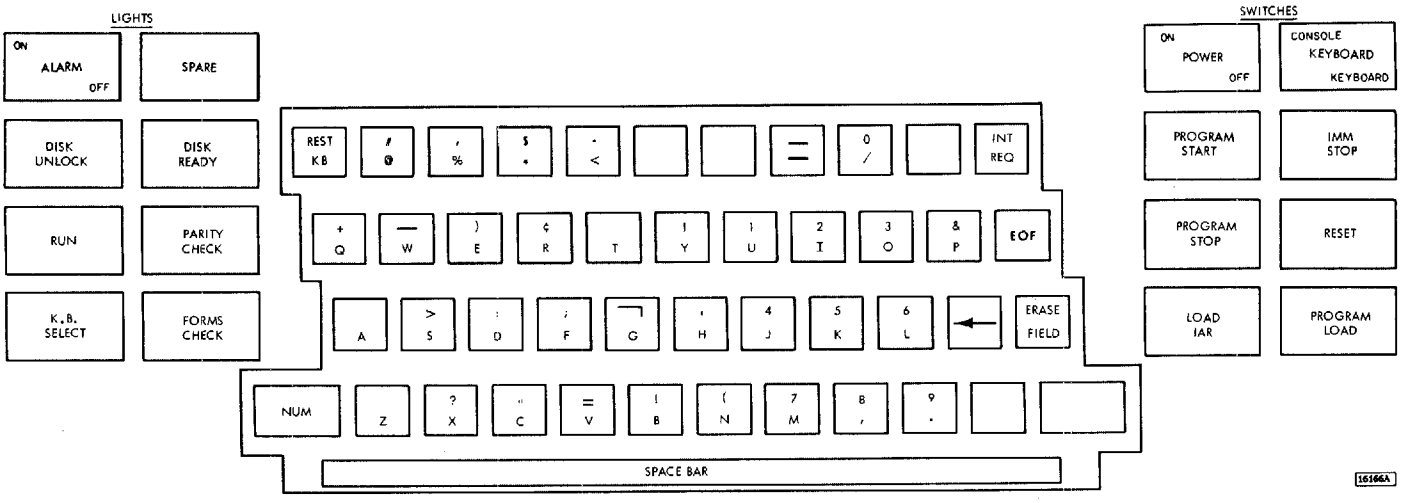


Figure 17. 1131 Console Keyboard

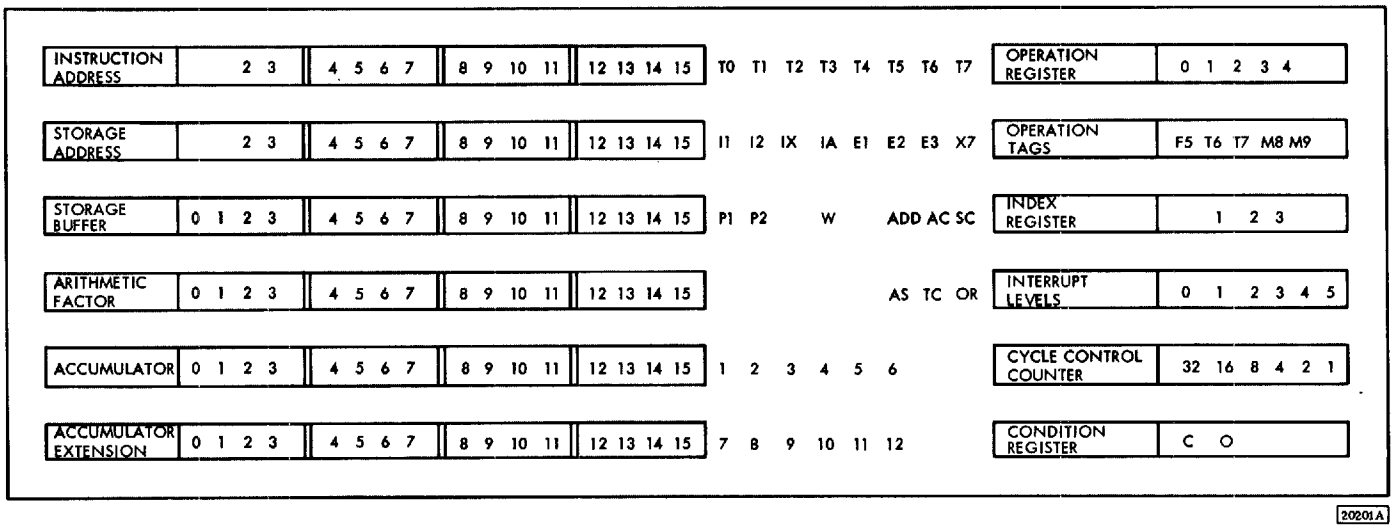


Figure 18. Console Display Panel

Machine Registers

The ten registers in the CPU are basic to the system and are functional elements of the CPU. Each register operates as necessary to enable the CPU to provide the results specified by the program. The abbreviation for each register name is the designation by which it is usually identified.

Accumulator (ACC): This 16-bit register contains the result of an arithmetic operation. It can be loaded from or stored in core storage, shifted right or left, and otherwise manipulated by specific arithmetic and logical instructions.

Accumulator Extension (EXT): This 16-bit register is the low-order extension of the ACC. It is used during multiply and divide operations, shifting of the ACC and EXT, and double-word arithmetic.

Temporary Accumulator (TAR): This 16-bit register is the image of the ACC and is used to store the contents of the ACC during effective address computation.

Arithmetic Factor Register (AFR): This 16-bit register holds one operand during arithmetic and logical operations. (The other operand is provided by the ACC.)

Storage Buffer Register (SBR): This 16-bit register is the buffer between the CPU and core storage, and every word of data transferred into or out of core storage passes through the SBR.

Storage Address Register (SAR): This 14-bit register contains the address pertaining to each reference to a core storage word.

Instruction Address Register (IAR): This 14-bit register holds the address of the next sequential instruction.

Operation Register (OP): This five-bit register holds the operation code of the instruction being performed.

Operation Tag Register (TAG): This three-bit register contains the F and T bits of the instruction. It controls the instruction length and selects the index register.

Cycle Control Counter (CCC): This 16-bit register is used primarily to count CPU cycles and control shift operations.

Typesetting Feature Registers

The IBM 1130 Typesetting System provides additional controls and registers to process data into, through, and out of the system. Additional registers for the selection of input and output devices and for the transfer of data are:

Reader Select Register (RSR): This 16-bit register contains the identification of the CX reader being used in the current operation. Each bit of the register represents an individual CX reader.

Punch Select Register (PSR): This four-bit register contains bit(s) that identify the BRPE punch being used in the current operation.

Read Data Register (RDR): This six-bit register is a buffer between the CX readers and the CPU. Each data character transmitted from a CX reader to the CPU is temporarily stored in the RDR.

The RDR (Figure 19) is modified to an eight-bit register if the six or eight channel data interchangeability (special feature) is installed.

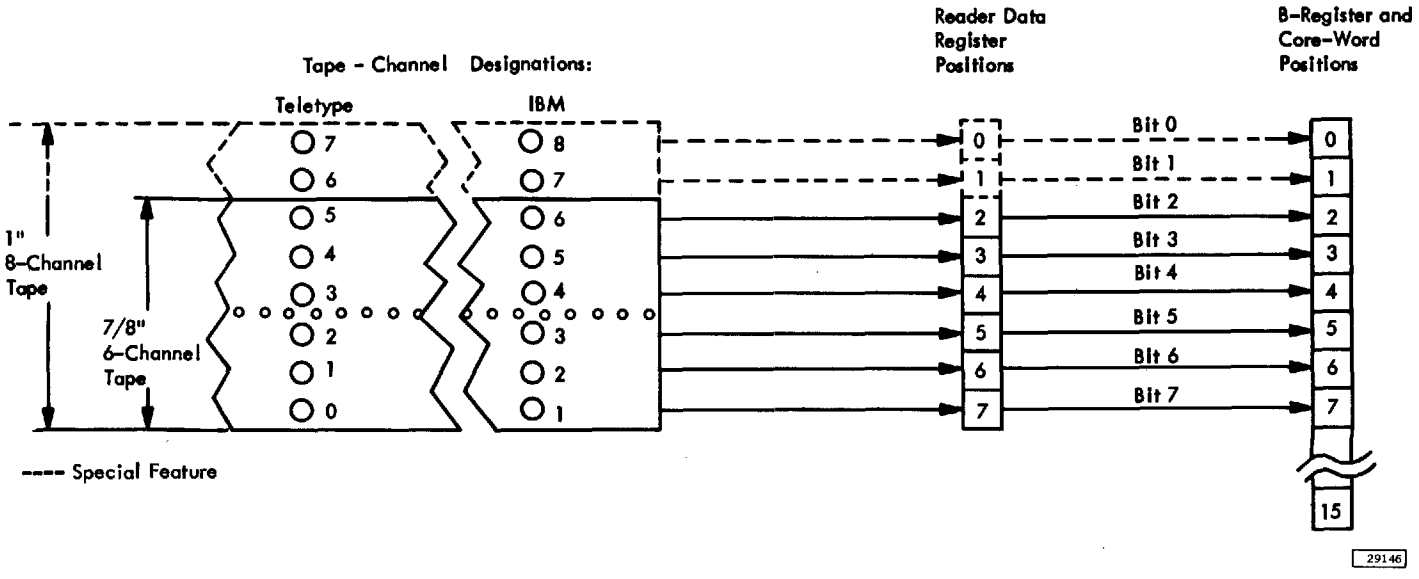


Figure 19. Input Data Format

Punch Data Register (PDR): This six-bit register is a buffer between the CPU and the BRPE punches. Each data character transferred from the CPU to a BRPE punch is temporarily stored in the PDR (Figure 20).

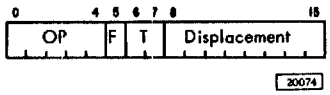
The PDR is modified to an eight-bit register if the six- or eight-channel data interchangeability (special feature) is installed.

Device Status Word—Operator Request (DSW-OR): This 16-bit register contains the identification of the CX readers requesting service from the CPU; i.e., those readers where the operator has finished transcribing a take into punched paper tape and has pressed the operator request key. Each bit of the register represents an individual CX reader.

INSTRUCTION FORMATS

Program instructions in the 1130 System are in either short or long format.

Short Instruction Format



Operation Code (OP): These five bits specify the operation performed.

Format (F): The F bit controls the instruction format. A zero (0) indicates a short instruction format, a one (1) designates a long instruction format.

Tag (T): These two bits specify the instruction counter or index register (XR) to be used for effective address generation.

Displacement: The data contained in these eight bits is added to the data in the instruction counter or index register specified by the tag bits to form the effective address (EA). See Figure 21.

Tag Bits	F = 0 (Direct Addressing)	F = 1, IA = 0 (Direct Addressing)	F = 1, IA = 1 (Indirect Addressing)
T = 00	EA = Disp + IAR	EA = Add	EA = C/Add
T = 01	EA = Disp + XR1	EA = Add + XR1	EA = C/(Add + XR1)
T = 10	EA = Disp + XR2	EA = Add + XR2	EA = C/(Add + XR2)
T = 11	EA = Disp + XR3	EA = Add + XR3	EA = C/(Add + XR3)

Disp = Contents of Displacement field of instuction.
Add = Contents of Address field of instruction.
C = Contents of Location specified by Add or Add + XR.

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Figure 21. Determination of Effective Address

Tag bits of 00 indicate that the displacement is added to the instruction address register (IAR) to form the effective address. The IAR contains the address of the next or immediately following instruction.

The three index registers can also be used to modify the displacement to form the effective address. Tag bits of 01, 10, or 11 designate registers 1, 2, or 3. Again, the contents of the specified register, added to the displacement, form the effective address.

NOTE: Displacement bits have other uses; for example, bits 8 and 9 are used as shift modifiers.

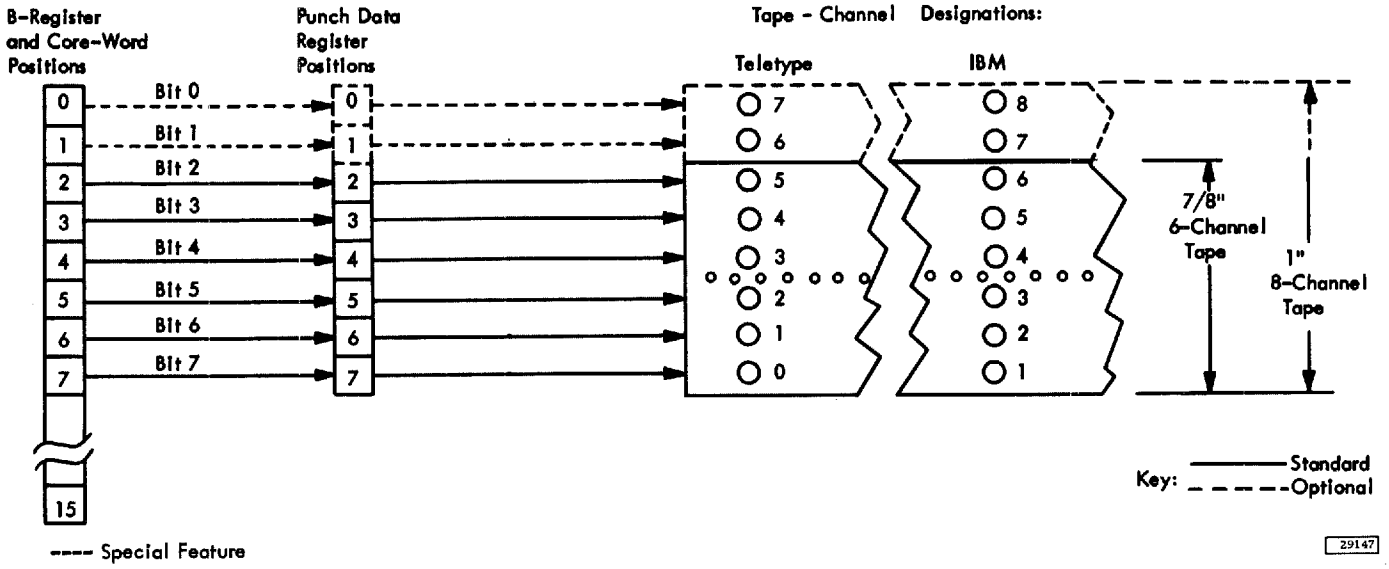
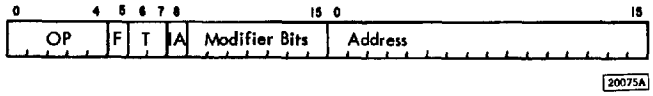


Figure 20. Output Data Format

Long Instruction Format



The first eight bit positions of the long instruction are the same as the short format. The remaining bit positions of this double precision word are used as follows.

Indirect Address (IA): A 0 indicates a direct address (contained in the second word). The effective address is governed by the contents of the tag field. Tag bits of 00 indicate that the address field of the instruction contains the effective address, which requires no modification. Tag bits of 01, 10, or 11 specify that the contents of the address field are added to index register 1, 2, or 3, respectively, to form the EA.

A 1-bit in the IA field of the instruction signifies that addressing is indirect, i.e., the address field of the instruction contains the address of the location in memory that contains the EA significant to the accomplishment of the instruction. The indirect address can be the contents of the address field of the instruction (T = 00), or it can be modified by being added to an index register (T = 01, 10, or 11). As an example (Figure 22), the indirect address is 0914. The CPU goes to that address and finds the contents of the location to be 2719. The EA, then, is 2719. This method of addressing provides one more level of modification of a given address and provides more versatility in programming for variations to the main line program.

Modifier Bits: Bit positions 9 through 15 have various uses as modifiers.

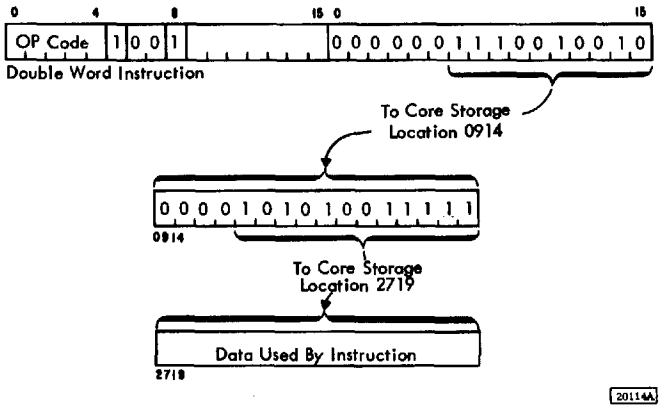


Figure 22. Indirect Addressing

Address: These 16 bits contain the address which may be used in its current form or modified by indirect addressing and/or EA modification.

INPUT/OUTPUT OPERATIONS

The IBM 1130 Typesetting System offers a variety of I/O devices. The keyboard for input and the console printer for output are standard on the IBM 1131 Central Processing Unit (CPU), Model 2. In addition, the 1131 model 2 provides the large capacity and random-access availability of data inherent in disk storage. The following attached units offer a wide diversity of I/O media:

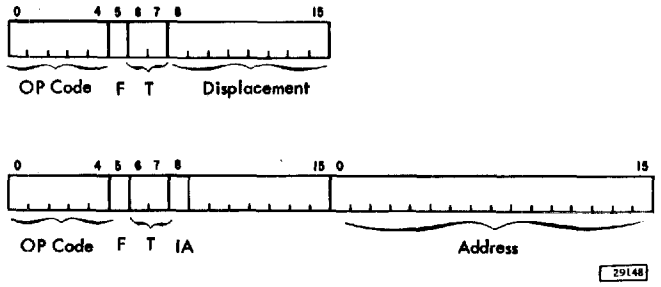
IBM 1134 Paper Tape Reader
IBM 1055 Paper Tape Punch
IBM 1132 Printer
IBM 1442 Card Read Punch
Teletype CX Paper Tape Reader (1 to 16)
Teletype BRPE Paper Tape Punch (1 to 16)

The programmed operation of each of the IBM devices is described in the Systems Reference Library publication "IBM 1130 Functional Characteristics" (Form A26-5881). The programmed operation of the Typesetting System, including the operation of the Teletype equipment, is described in succeeding sections of this manual. Programming operations common to all I/O devices are included to facilitate understanding the Typesetting feature instructions.

The IBM 1130 Typesetting System uses only one I/O instruction: Execute I/O.

Execute I/O (XIO)

This instruction can be in either the short or long format, and operation is the same, except for the inherent differences in the manner in which the EA is generated, and the fact that the long format can have either a direct or indirect address.



The effective address is the core storage location of the first word of the I/O control command (IOCC) and must be even. EA+1 is the location of the second word of the IOCC.

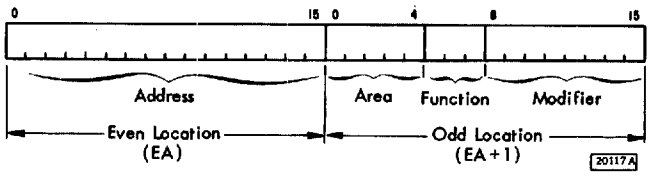
Programming Note: The contents of the accumulator, if significant, must be stored prior to the execution of the XIO instruction. The contents are destroyed during the instruction execution.

Input/Output Control Command

Seven I/O control command functions are provided for the IBM 1130:

Read
Write
Initiate Read
Initiate Write
Control
Sense Device
Sense Interrupt

All I/O control commands have four parts:



Address

The use of this field depends on the function and the device specified.

1. If the function is Write (001) or Read (010), the address specifies the core storage location of the data word.
2. If the function is Sense Device (111) or Sense Interrupt (011), the address field is ignored. Instead, an increment of time, equivalent to a core storage cycle, is taken, during which the selected I/O device or interrupt level places its status code into the accumulator.
3. If the function is Initiate Write (101) or Initiate Read (110), the address specifies the starting address of a table in storage (an I/O block). This table contains data words and control information. Initiate write and initiate read functions are used only with disk storage.
4. If the function is control (100), and the device specifies the disk storage device, the address indicates the number of tracks the access must be moved.

   If the function is control (100), and the device specifies the typesetting feature, the use of the address is further defined by the modifier field.

Device

This 5-bit field (area) identifies the I/O device.

00010	1442 Card Read Punch
00110	1132 Printer
00100	Disk Storage
00011	1134 Paper Tape Reader, 1055 Paper Tape Punch
00001	Console Keyboard, Console Printer
00111	Console Entry Switches
11000	Typesetting Feature

Function

The seven primary I/O functions are specified by the 3-bit function code:

000--Not used

001--Write
This code is used to transfer a single word from core storage to an I/O unit. The address of the core storage location is provided by the address field of the I/O control command.

010--Read
This code is used to transfer a single word from an I/O unit to core storage. The address of the core storage location is provided by the address field of the I/O control command.

011--Sense Interrupt
This code directs the I/O devices requesting interrupt recognition on the interrupt level specified by the modifier field of the I/O control command to make their interrupt status available.

100--Control
This code causes the selected device to interpret the modifier or address field as a specific control action.

101--Initiate Write
This code initiates a write operation on the disk storage unit which will subsequently make data transfers from core storage under disk storage control.

110--Initiate Read

This code initiates a read operation from the disk storage unit which will subsequently make data transfers to core storage under disk storage control.

111--Sense Device

This code loads the accumulator (ACC) with the device status word (DSW) for the device specified in the IOCC. The status indicators are reset by specifying modifier bits as follows: bit 15 for the highest level to which the device is connected, bit 14 for the next highest, and so on.

Modifier

The 8-bit modifier field provides additional definition of either the function or device. For example, if the device field specifies the 1132 Printer (00110) and the function specifies control (100), a particular modifier bit specifies the operation the printer is to perform.

If the IOCC specifies the typesetting device (11000), the modifier bits expand the function field to indicate the operation to be performed. In addition, for certain typesetting system instructions, the modifier bits require that the address field of the IOCC be used to further identify the individual typesetting unit that is to perform the operation.

INTERRUPT

The interrupt facility provides an automatic branch from the normal program sequence based upon an external condition. The following interrupt levels are available with the 1130 Typesetting System.

Level	Device
0	1442 Card Read Punch (column read, punch)
1	1132 Printer
2	Disk Storage
4	1442 (operation complete); Keyboard/Console Printer; 1134 Paper Tape Reader; 1055 Paper Tape Punch; Typesetting Feature
5	Console (Program Stop switch)

Interrupt Philosophy

Because of the number of types of interrupt requests, it is not always possible to cause a branch to a unique address for each interrupt condition. For the same reason, it is frequently not desirable to cause one branch for all interrupt requests and require the program to determine the individual request(s) requiring service. Therefore, it is expedient to group the many individual request lines into a lesser number of priority levels. This grouping accomplishes two very important functions: First, it allows all interrupt requests common to a specific device to have the privilege of interrupting immediately if the only requests waiting or being serviced are of a lower priority level. Service is returned to the initial request only after all higher level requests have been serviced. Second, since a unique branch can be defined for each interrupt priority level, it is possible to combine many interrupt requests on a common priority level and therefore use a common interrupt subroutine to service many requests.

There are two important operating characteristics of the 1130 interrupt system: (1) when more than one request line is connected to any priority level, it is necessary, by programming means, to identify the individual request(s) causing the priority level to be energized; (2) the first request that causes an interrupt prevents future requests on the same or lower priority levels from interrupting until the completion of servicing the first interrupt is signaled by a branch out operation. (See Branch or Skip on Condition-BSC.)

Interrupts that occur on the same level for which an interrupt is being serviced can be detected and acknowledged before the branch out operation is executed.

Program Operation

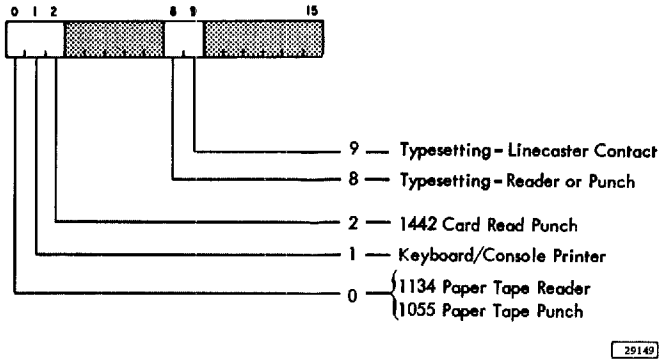
An interrupt may be recognized by the CPU at the completion of any program instruction. It is initiated by the basic interrupt control, which forces execution of a CPU-generated Branch and Store IAR (BSI) instruction. The indirect address of the generated BSI instruction is in location 8-13, corresponding to the level of interrupt. This location should contain the address of the location in the interrupt routine where the IAR is to be stored.

As defined by the BSI instruction description, the IAR is stored at the EA (effective address) and program execution is resumed with the branch to the EA + 1. It is the responsibility of the interrupt subroutine to store all data and/or index registers that are used by the routine, and to restore the same registers prior to departing from the subroutine.

Several devices can request an interrupt on level 4. It thus becomes necessary for the program to determine the requesting device. Identification of the requesting device is accomplished by issuing an XIO instruction with a function of Sense Interrupt.

The Sense Interrupt function is decoded and sent to all I/O devices, along with the current interrupt level being serviced. Each device that is requesting service on level 4 will have a bit appear in an interrupt level status word (ILSW) that is loaded into the accumulator, provided that level 4 is being serviced. The Sense Interrupt command will therefore produce meaningful results only if executed in a program sequence that is a result of interrupt level 4, and before a Branch Out command is executed in this routine.

Interrupt Level Status Word



Although a 16-bit ILSW could exist for each priority level, only level 4 uses the ILSW in the 1130 System. Each device with an interrupt request signal assigned to priority level 4 is given a particular bit position in its ILSW to indicate its interrupt request status, a 1-bit if on and 0 if off. The status indicator(s) in the device(s) is not affected by the sensing of the ILSW. It is possible for a device to contain several conditions which may cause an interrupt on the same interrupt level. When this condition exists, the interrupt conditions are logically ORed to become a single interrupt. The identification of the interrupting condition within the device is accomplished by sensing the device status word (DSW) as described in subsequent paragraphs.

Interrupt Identification

Following loading of ILSW 4 in the ACC (accomplished by an XIO-Sense Interrupt instruction), the Shift Left and Count instruction is used to facilitate examination of the ILSW. First, an index register is loaded with a quantity which corresponds to the number of request signals connected to interrupt priority level 4, followed by the Shift Left and Count instruction (SLC). The resulting count in the index register is unique and corresponds to the first non-zero bit of the ILSW in the accumulator. (It is also possible to execute a Shift Left and Count of both the ACC and EXT.) The SLC is followed by a Branch or Skip on Condition instruction (BSC) utilizing the F = 1 format with IA = 1, indexed with the result of the SLC. This provides, in conjunction with a branch table, a unique branch for each non-zero bit of the ILSW.

After the device causing an interrupt has been identified from data in the ILSW, it is necessary to determine the indicator(s) within the particular device causing the interrupt. The indicator is determined by issuing a subsequent XIO Sense Device instruction with an area assignment corresponding to that of the device being interrogated. The status indicators are reset after the information has been loaded in the ACC, if a bit is present in position 15 of the modifier. If a device can initiate interrupts on more than one interrupt level, the indicators are reset by specifying modifier bits as follows: bit 15 for the highest level to which the device is connected, bit 14 for the next highest level, and so on.

The data in the ACC is now referred to as the device status word (DSW).

Device Status Word

The DSW contains one bit of information for each indicator within the device. These usually fall into three categories, (1) error or exception interrupt conditions, (2) normal data or service-required interrupts, and (3) routine status conditions.

Programming Note: When an interrupt request has been detected by a priority level, the program is directed to service the request by interrupting. During the servicing, all interrupt requests of equal or lower status are effectively constrained from interrupting while the servicing of the higher priority is in progress. However, if a request is detected for a higher priority level than is presently in progress, the program is immediately interrupted again. This procedure is frequently called nesting of interrupts.

At the completion of servicing any level of interrupt, it is necessary to signal the priority hardware to reset the priority-status of the highest level that is on. This reset permits lower priority requests (including those that may have been temporarily constrained, but recorded) to be accepted once again by the CPU. The reset is accomplished by a BSC instruction with bit 9 = 1. This programmed recognition of waiting interrupts should not be confused with a normal subroutine linkage back to a mainline program in which case bit 9 should be set to 0.

The BSC is a conditional instruction, and when bit 9 = 1, the interrupt level is reset only when the branch or skip occurs.

TYPESETTING SYSTEM OPERATIONS

The IBM 1130 Typesetting System provides special circuitry in the IBM 1131 CPU for the attached CX readers and BRPE punches. The functional use of these devices is similar to standard IBM paper tape devices; operational similarity permits programming instructions for control and interrupt to be similar. The basic instruction is Execute I/O (XIO) which fetches the associated input/output control command (IOCC) word from storage. The format of the IOCC is the same as for IBM paper tape devices, but the device code and the modifiers are changed to accommodate the requirements of the typesetting system.

The following descriptions of the typesetting operations point out the similarities, modifications, and additions to the standard operations. Knowledge of the basic input/output operations of the 1130 system is assumed. Refer to Systems Reference Library publication "IBM 1130 Functional Characteristics", (Form A26-5881), for details.

As with the standard IBM paper tape devices, the CX readers and BRPE punches are incremental devices and must be issued a command for each read and punch operation. A read or punch operation is always associated with the transfer of a single character. Each operation has an associated interrupt that allows the computer to overlap I/O operation with other programming functions.

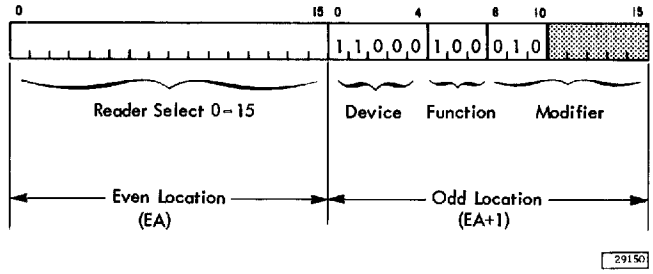
The typesetting feature operates under direct program control of the 1131 CPU. When an IOCC is fetched from storage as a result of an Execute I/O instruction, the IOCC defines and addresses the command to the typesetting logic by the 5-bit device code 11000. The 12 specific typesetting commands are divided between Control, Read/Write, and Sense commands.

Control Commands

Control commands are defined by the 3-bit function code 100 in the IOCC. The control commands are further identified by the first three modifier bits (positions 8, 9, and 10) of the EA + 1 portion of the IOCC.

Select Reader

From 1 to 16 CX readers can be attached to an 1130 Typesetting System. Because only one reader can be operated at a time, this command allows selection of one reader to be operational with the system.



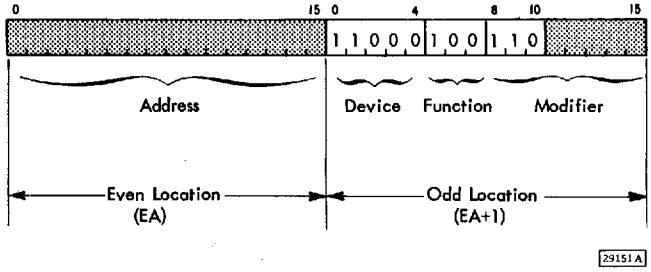
The reader selected is specified by 1 in the bit position of the EA that represents the desired reader. The command transfers this bit to the corresponding bit position of the reader select register. The reader select register directs all subsequent reader IOCC's to that reader until a Deselect Reader command is executed.

The Select Reader command also places the CPU in reader select mode. Reader select mode causes the CPU to mask all operator request interrupts until the reader is deselected. When the reader is deselected the next waiting operator interrupt request is serviced.

Programming Note: The reader select register is not reset by this command. Erroneous reader selection will result from issuing this command without a prior Deselect Reader command.

Deselect Reader

The Deselect Reader command detaches the selected reader from the system.

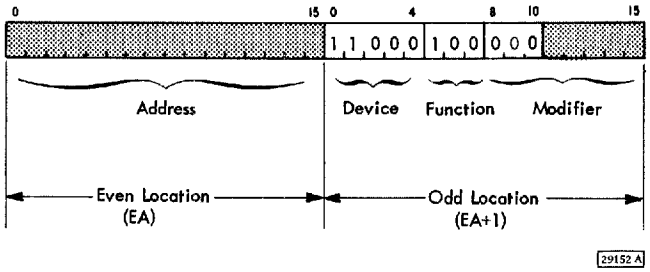


The command resets the entire 16 position reader select register and places CPU in the reader deselect mode. In reader deselect mode, the CPU will recognize operator request interrupts from CX readers.

Programming Note: The Deselect Reader command should always be used prior to a Select Reader command to prevent erroneous reader selection.

Start Read

The start read command causes the selected CX reader to go through a feed cycle. One character is read and placed in the read data register.

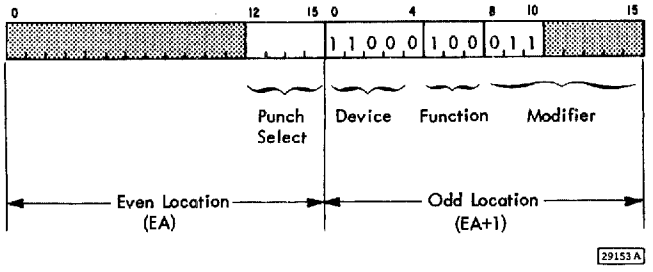


If the selected CX reader is ready and not busy, this command causes a signal to be issued to the reader to initiate a mechanical feed cycle. One character is read during the cycle, the CX reader returns a signal that causes the read data register to be reset and then set with data bits corresponding to the holes in the tape read during the cycle. The signal returned by the reader also causes a reader response to be stored in the CPU to indicate that a character has been read. Reader response subsequently causes an interrupt.

No hardware checking or translation of the character is performed. Any checking or translation must be performed by the computer program.

Select Punch

From 1 to 16 BRPE punches can be attached to an 1130 Typesetting System. Because only one punch can be operated at a time, this command allows selection of one punch to be operational with the system.



The punch selected is specified by a 1 in the bit position(s) of the EA that represents the desired punch. The command transfers this bit(s) to the corresponding bit position(s) of the punch select register. The punch select register selects the punch and directs all subsequent punch IOCC's to that punch until another select punch command is executed. The following illustration shows the bit combinations that select each of the 16 punches.

Punch Select	Bit Position 12	13	14	15
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

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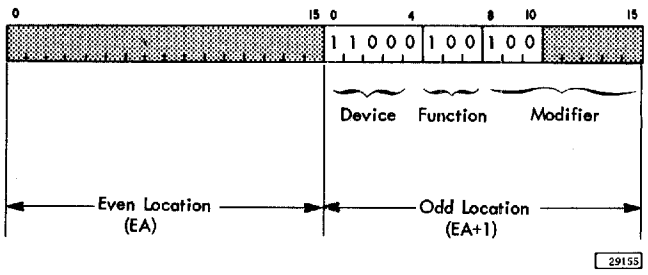
Mask

The Mask command places the CPU in mask mode. In mask mode, the CPU inhibits all typesetting interrupts.



This command prevents the CPU from recognizing the following typesetting interrupts: operator request, reader response, punch response, or linecaster contact sense. Mask mode is active until an Unmask command is executed.

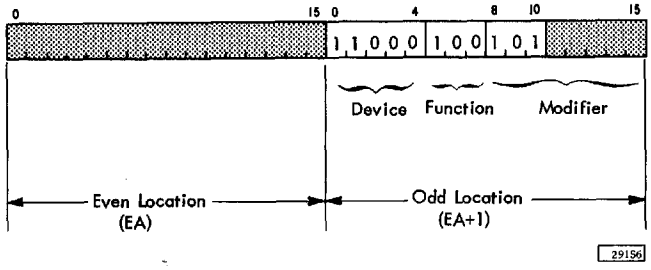
Masking is a convenient means of preventing undesired interrupts. For example, if the 1130 System is being used for a non-typesetting application, such as payroll, the programmer may wish to ensure that accidental or unauthorized operation of the typesetting equipment cannot interfere with the operation. The programmer can precede the payroll operation with a Mask command.

Interrupt requests occurring while the CPU is in masked mode are not necessarily lost. Most interrupt requests are stored until an Unmask command is executed, at which time waiting interrupts are honored.

Pressing the reset key places the CPU in mask mode.

Unmask

The Unmask command places the CPU in unmask mode. In unmask mode all typesetting interrupts can be honored.



This command allows the CPU to recognize the following typesetting interrupts: operator request, reader response, punch response, and linecaster contact sense. Unmask mode is active until either a Mask command is executed or the reset key is pressed.

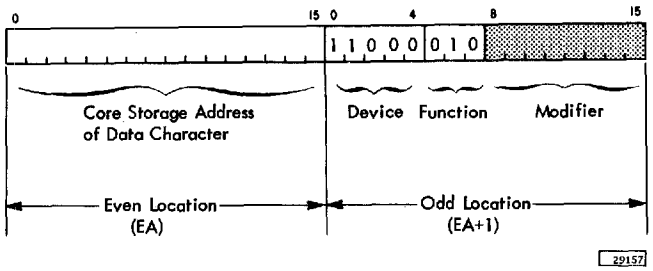
Reader response, punch response, and linecaster contact sense interrupts are honored by the CPU as soon as interrupt priorities will permit. Operator request interrupts will also be honored if the CPU is in the deselect reader mode.

Read/Write Commands

The Read/Write commands transfer one character between the corresponding data register and a core storage location. These commands are defined by the 3-bit function code.

Read

The Read command transfers the data character from the read register to core storage.

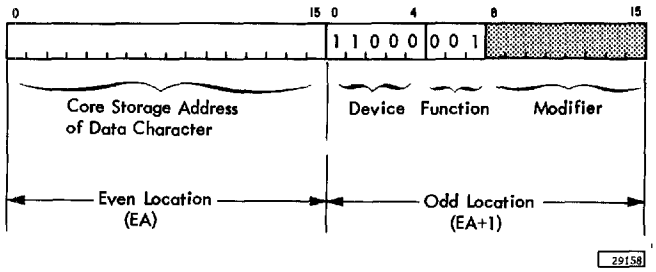


This command transfers the bits in the read register to the core storage location specified by the address field (EA) of the IOCC. After this command is executed, the storage location contains a bit-for-hole image of the character read from paper tape by the preceding Start Read command.

No translation or parity checking of the read data is performed. Checking or translating is a programming function.

Write

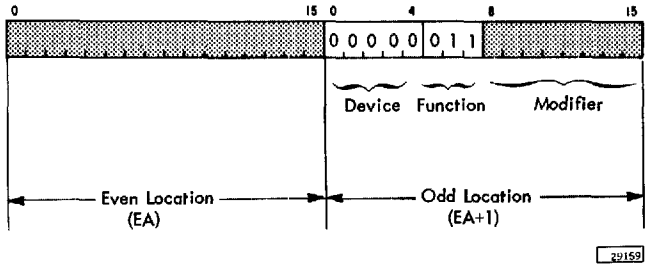
The Write command transfers one data character from core storage to the punch data register and initiates a punch cycle to punch the character into tape.



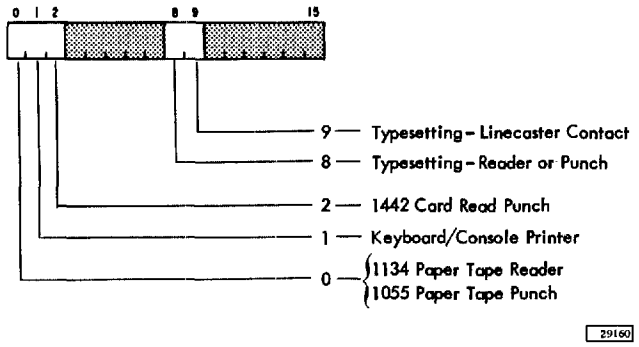
This command causes the bits in the core storage location specified by the address field (EA) of the IOCC to be transferred to the punch data register and signals the punch to start a cycle. To the CPU, the punch is considered busy while punching the hole-for-bit image into tape. The signal returned from the punch resets punch busy, clears the punch data register, and is stored in the CPU as punch response. Punch response indicates the character has been punched and subsequently causes an interrupt.

Sense ILSW-4

The Sense ILSW-4 command is used to determine the device or group of devices that caused the interrupt.



This command loads the ILSW-4 into the accumulator to be analyzed by 1130 interrupt programming. A bit in the ILSW-4 identifies the device or group that caused the interrupt. Further identification as to cause and device is determined by sensing the DSW associated with the interrupt.



Bits 8 and 9 of the ILSW-4 have been added for the Typesetting feature. The 1130 system must be in unmasked mode to recognize these typesetting interrupts.

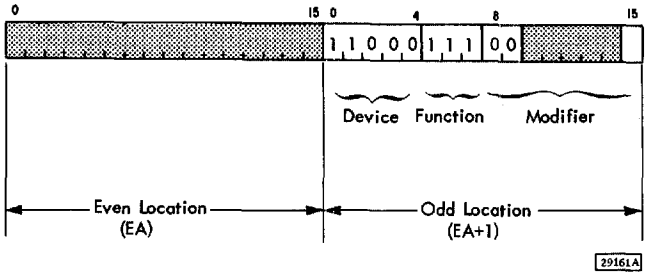
Bit 8 of the ILSW-4 identifies an interrupt due to either a CX reader, operator request, or a BRPE punch. If this bit is on, further 1130 program analysis of the interrupt is required. Sensing the device status word-status and interrupt (DSW–SI) determines the specific device and cause of the interrupt.

Bit 9 of the ILSW-4 identifies an interrupt due to a linecaster contact sense, if this feature is installed on the system. If this bit is on, further 1130 program analysis of the interrupt is required. Sensing the device status word–linecaster contact sense (DSW–LCCS) determines the specific linecaster that causes the interrupt.

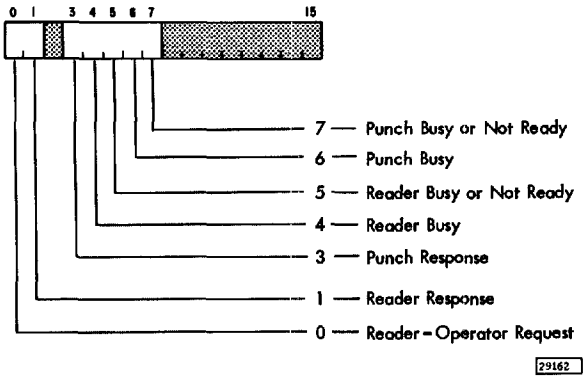
Sense DSW-SI

The Device Status Word-Sense Interrupt (DSW-SI) command is used to determine either the source of the interrupt or the status of the device.

Bit position 15 of the odd location (EA+1) is used in conjunction with a reader or punch response. If bit position 15 contains a 1, the corresponding response bit is turned off.



This command loads the DSW-SI of the typesetting feature into the accumulator to be analyzed by 1130 interrupt programming. A bit in a particular position of the DSW-SI identifies the interrupt cause or the device status.



Bit 0: A 1 in position 0 indicates an operator request and signifies that an operator pressed the operator request key on a CX reader to request the read-in of a take from that particular reader. Because any of the readers attached to the system (up to 16) can request read-in service, the specific reader is subsequently determined by sensing the device status word – Operator Request (DSW-OR). See Sense DSW-OR.

The system must be in reader deselect mode (no reader selected) and unmasked mode to recognise an operator request in the DSW-SI.

An operator request indicator is turned off by selecting the reader that requests the service.

Bit 1: A 1 in position 1 indicates a reader response and signifies that the selected CX reader has completed a feed cycle as directed by the preceding Start Read control command. A character has been placed in the read data register. Read response is turned off by the execution of this command (a 1 in position 15), by deselection of the reader, or by pressing the reset key.

Bit 3: A 1 in position 3 indicates a punch response and signifies that the selected BRPE punch has completed a punch cycle as directed by the preceding Write control command. The punch data register has been cleared, and the punch can accept another Write command. Punch response is turned off by this command (a 1 in position 15), by deselection of the punch, or by pressing the reset key.

Bit 4: A 1 in position 4 indicates the selected CX reader is busy. The reader is busy from the beginning of the Start Read control command until reader response is received, the reader is deselected, or the reset key is pressed.

Bit 5: A 1 in position 5 indicates the selected CX reader is busy or not ready. Not ready indicates either no paper tape in the reader or the tape is not feeding properly. Manual intervention is required. See Bit 4 for busy conditions.

The 1130 program should determine that this indicator is off before issuing a Start Read control command; otherwise, erroneous data may be placed in storage.

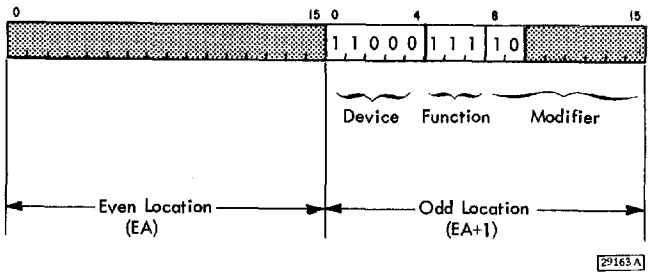
Bit 6: A 1 in position 6 indicates the selected BRPE punch is busy. The punch is busy from the start of the Write control command until the punch response is received, the punch is deselected, or the reset key is pressed.

Bit 7: A 1 in position 7 indicates the selected BRPE punch is busy or not ready. Not ready indicates that the tape supply is low or depleted. Manual intervention is required. See Bit 6 for busy conditions.

The 1130 program should determine that this indicator is off before issuing a Write control command, or loss of data may occur.

Sense DSW-OR

The Device Status Word—Operator Request (DSW-OR) command is used to determine which CX reader has requested read-in service.



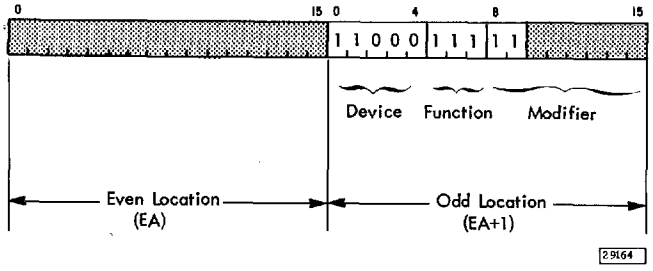
This command is used after program analysis of the DSW-SI indicates that an operator request has caused the interrupt. The DSW-OR command loads the contents of the operator request register into the accumulator. Analysis of the DSW-OR by 1130 programming determines which CX reader is requesting read-in service.

The operator request register is a 16-position register, each position representing the operator request key on a corresponding CX reader. When an operator presses the request key on a reader to signal that a take is ready to be read into the system for processing, the associated register position is set to 1. As soon as the 1130 system is in deselect reader mode (no reader selected) and unmasked mode, an operator request interrupt occurs.

Several readers may be requesting read-in service simultaneously, but only one can be serviced at a time. The positions of the operator request register are individually reset by selecting the corresponding reader. The remaining positions of the register remain set until the respective readers are selected and serviced.

Sense DSW-LCCS

The Device Status Word-Linecaster Contact Sense (DSW-LCCS) command is used to determine which linecaster contact caused the interrupt.



This command is used after 1130 program analysis of the ILSW-4 indicates that a linecaster contact has caused the interrupt. The DSW-LCCS command loads the contents of the linecaster contact register into the accumulator. Analysis of the DSW-LCCS by 1130 programming determines which linecaster caused the interrupt.

The linecaster contact register is a 16-position register, each position representing the contact on a corresponding linecaster. When a linecaster completes casting a line of type and closes the contact, the associated register position is set to 1. The register is cleared by the Sense DSW-LCCS command.

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