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IBM

Systems Reference Library

IBM 1800 Functional Characteristics

This manual is a reference source for IBM 1800 Data Acquisition and Control System users who require detailed knowledge of the functional and operational characteristics of the system. The functional aspects of the processor-controller and associated features, as well as all available process, data processing, and communications input/output features and devices are described in detail. Operational characteristics of these system features and components are described in terms of program instructions, input/output operations, and processor-controller console functions and displays.

The user of this manual should have a basic knowledge of stored program computer concepts and should be familiar with the information contained in the IBM 1800 System Summary, Order No. GA26-5920.

Preface

This manual is a reference source for IBM Data Acquisition and Control System users who require detailed knowledge of the functional and operational characteristics of the system. The functional aspects of the processor-controller and associated features, as well as all available process, data processing, and communications input/output features and devices are described in detail. Operational characteristics of these system features and components are described in terms of program instructions, input/output operations, and processor-controller console functions and displays.

Method of Presentation

The features and devices of the 1800 system are divided into four categories: (1) processor-controller and associated features, (2) process input/output devices, (3) data processing input/output devices, and (4) communications input/output features or devices. Following the introduction, the information in this manual is presented according to the preceding four categories.

Because of frequent use, the instruction set section of this manual is designed for easy access. Where possible, the description of each instruction in the instruction set is confined to a single page. Each page has a tab containing the mnemonic code of the instruction described. The tab is located at the lower edge of the page. By glancing at the tabs, one can quickly locate any desired instruction.

Prerequisites

The user of this manual should have a basic knowledge of stored program computer concepts. In addition, the user should have read the prerequisite publication, IBM 1800 System Summary, Order No. GA26-5920.

Suggested Reading

The instruction set section of this manual contains examples of assembler language coding. However, no attempt is made to explain all aspects of assembler language programming. Therefore, IBM 1800 Assembler Language, Order No. GC26-5882, is suggested reading.

For other suggested reading material, refer to the IBM 1800 Bibliography, Order No. GA26-5921.

Ninth Edition (August, 1970)

This is a major revision of, and makes obsolete, GA26-5918-7 and Technical Newsletters GN26-0255 and GN26-0260. The entire manual has been rewritten and reorganized for clarity. Technical changes to the text and to illustrations are indicated by a vertical line to the left of the change. Nontechnical changes are not indicated by any special marking.

Significant changes or additions to the specifications contained in this publication are continually being made. Before using this publication in connection with the operation of IBM equipment, check the latest SRL Newsletter for revisions or contact the local IBM Branch Office.

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Introduction

The ever-increasing pace of technology, industry, and business continues to demand larger and larger amounts of reliable, up-to-date information. History is a good teacher, true, but its compression within the past few decades of progress has taught us that today's problems require real-time answers, not a history of past performances. Data of almost every conceivable nature -- available from a myriad of sources -- must be collected, analyzed, and translated into terms that can be used to optimize today's performance.

IBM's answer to the demand for real-time data acquisition, analysis, and control is the IBM 1800 Data Acquisition and Control System. The 1800 system handles a wide variety of process control, data acquisition, and real-time applications. Each system can be individually tailored with modular building blocks to meet specific system requirements.

SYSTEM DESCRIPTION

The 1800 system offers a wide variety of features and devices as follows:

- A processor-controller for editing, control, or data analysis.
- A family of real-time process input/output (I/O) devices such as analog input, analog output, digital input, and digital output.
- A variety of data processing I/O devices such as magnetic tape, disk storage, line printer, graph plotter, card I/O, and paper tape I/O.
- Communications I/O devices such as communications adapters, System/360 adapter, and 2790 Data Communications System adapters.

Processor-Controller

The processor-controller has the following functions and features:

- A central processing unit that provides arithmetic, logic, and control functions for the 1800 system.
- Three index registers, 12 levels of priority interrupt (expandable to 24 by special feature), three data channels (expandable to 15 by special feature), three interval timers, an operations monitor, and an operator's console.
- Up to 32,768 words of core storage. Total system core storage can be expanded to 65,536 words with the addition of an IBM 1803 Core Storage Unit. In this case the processor-controller contains 24,576 words of core storage and an 1803 adapter.
- Basic circuitry and controls for attachment of process input/output equipment.
- Stored program control of input/output and processing.

Within its basic design, the processor-controller has interrupt and core storage cycle stealing capabilities which are used in controlling the various I/O devices attached to the system. The interrupt facility provides an automatic branch from normal program sequence, caused either by external conditions (those in the process) or internal conditions (those within the 1800). Data channels have the ability to delay program execution while an I/O device steals a machine cycle to communicate with core storage. Cycle stealing does not change the logical condition of the processor-controller; therefore it can occur during program instruction execution.

Index registers, one level of indirect addressing, and a complete instruction set with powerful options give the processor-controller high performance for tasks normally encountered in data acquisition and control applications.

Two processor-controllers are available -- IBM 1801 and IBM 1802. The 1801 has no provision for magnetic tape, while the 1802 includes the tape control unit for the IBM 2401/2402 Magnetic Tape Units.

Process Input/Output Features

Real-time process I/O features enable the 1800 system to accept either analog or digital input signals and provide analog or digital output signals for control or display purposes. The modularity of these features allows the 1800 system to be matched to

the process requirements. Process I/O features include:

- Analog input, which converts bipolar voltage or current signals to digital values for use by the processor-controller.
- Digital input, which accepts binary information represented by contact closures or voltage levels.
- Analog output, which converts digital values to precise voltage levels for operating process devices.
- Digital output, which provides binary data to the process in the form of "contact" closures or voltage levels.

Analog input features include analog-to-digital converters, multiplexers, amplifiers, and signal conditioning equipment to handle all types of process analog input signals. High-speed system conversion rates are provided, with program selectable resolution and external synchronization. Analog input capacities are 1,024 relay multiplexer points and 256 solid-state (high-speed) multiplexer points. A second analog-to-digital converter can be added to double the system analog input performance and capacity.

Digital input features provide up to 384 process interrupt points; up to 1,024 bits of contact sense, digital input, or high-speed parallel register input; or 128 high-speed pulse counters.

Analog output features provide up to 128 analog output points for individual or simultaneous operation of a wide range of customer devices.

Digital output features provide up to 2,048 bits of pulse output, electronic "contact" operate, and high-speed register output.

Data Processing I/O Devices

Data processing I/O devices enable the 1800 system to perform the necessary data processing for data analysis, editing, and control purposes. These devices are also used to provide instructions for process and control room operators as well as reports for management review.

To provide the necessary logical and buffering capabilities for I/O device operations on the 1800 system, a control (adapter) feature is available for each device. The following data processing I/O devices can be attached to the 1800 system by means of the I/O attachment features:

- IBM 1053 Printer.
- IBM 1054 Paper Tape Reader.
- IBM 1055 Paper Tape Punch.
- IBM 1442 Card Read Punch.
- IBM 1443 Printer.
- IBM 1627 Plotter.
- IBM 1810 Disk Storage.
- IBM 1816 Printer-Keyboard.
- IBM 2311 Disk Storage Drive (attached via the selector channel and the IBM 2841 Storage Control).
- IBM 2401/2402 Magnetic Tape Unit.

Communications Devices

These devices and adapters permit expansion of 1800 system capabilities so that it can be utilized in applications requiring multiprocessor systems, remote telecommunication or direct communication capabilities, or multipoint real-time data collection or communications. These devices include:

- System/360 adapter.
- Communications adapters.
- 2790 Data Communications System adapters.

The System/360 adapter provides a control and data path for direct attachment of an IBM System/360 in applications where more powerful supervision is required. For example, the System/360 may be used to integrate the commercial aspects of an application with the controlling operations exercised by the 1800 system.

The communications adapter (maximum of four) provides one or two communication paths (line adapters) for connection, over voice grade lines, to remote System/360's, IBM 1130 systems, IBM 2770

Data Communications Systems, IBM 2780 Data Transmission Terminals, or other 1800's. This allows the 1800 system to be integrated into large scale control systems without consideration of the physical location of control systems above or below the 1800 in the control hierarchy.

The 2790 adapter (maximum of two) provides the interface facilities for attaching an IBM 2790 Data Communications System to the 1800 System processor-controller. This 1800/2790 combination provides real-time data collection or communication capabilities with the 1800 being the system controller for the 2790 system.

SYSTEM DATA FLOW

- Data is stored and processed in fixed-length 18-bit words for fast parallel manipulation of data. Each 18-bit word contains 16 data bits; the remaining 2 bits are used for parity checking and storage protection control purposes.

- I/O devices are connected to the processor-controller via a standard I/O interface.

- Adapter circuitry at each I/O device performs the necessary conversion, buffering, and control functions.

- Cycle-stealing capability permits high-speed transfer of data to and from main storage.

A standard I/O interface is used between the processor-controller and all input/output devices. Adapter circuitry to accommodate each type of I/O device is installed in the 1800 system as required. The adapters provide the necessary buffer registers and controls to permit operation on the system. Figure 1 shows the data flow between the processor-controller and the various I/O devices.

In a closed-loop process system, process conditions are monitored and analyzed continuously, and controlling signals are sent to the devices that control the process. Input data is obtained directly from measuring devices in the process area without the need for off-line conversion equipment. Signal conditioning, multiplexing, and conversion functions are performed by the input circuits. The input data, in the 1800 format, is held in registers until called for entry into core storage.

After the input data has been read and analyzed by the processor-controller, the program may select a process control function. Both digital and analog output data can be generated for controlling equipment such as set-point positioners, displays, and telemetry systems.

Data processing information can be entered and retrieved in a variety of forms through the data processing or communication devices and their adapter circuitry.

When any device is ready to send or receive data, it can notify the processor-controller by issuing an interrupt request. The program identifies the reason for the interrupt by sensing the status of indicators associated with each I/O device. The program responds to the interrupt by sending the appropriate I/O command to the device. Each I/O command always places a control word on the out bus to specify the input/output device and the function to be performed. Depending on the intrinsic data rate of the device receiving the control word, the system allows for transfer of data between core storage and the device in one of two ways: under direct program control or by data channel operations.

A data channel transfers data on a high-speed cycle-steal basis, using a data table in core storage for flexibility of scanning rates and patterns. The core storage cycle-stealing capability makes it possible to delay the program for one machine cycle if necessary and to use this cycle to transfer the data word between core storage and the I/O device. Cycle stealing and interrupt servicing are conducted by the processor-controller on a priority basis. This makes it possible to simultaneously control combinations of real-time input/output devices.

APPLICATIONS

The 1800 system is capable of accepting electrical signals, both analog and digital, from such devices as thermocouples, pressure and temperature tranducers, flow meters, analytical instruments, and contacts. The system provides electrical on/off and analog control signals for the customer's controlling devices. With these capabilities and remote communications facilities, the 1800 system can be integrated into large multiprocessor systems with varied real-time applications. Typical applications exist in the area of process control, high-speed data acquisition, and real-time data communications.

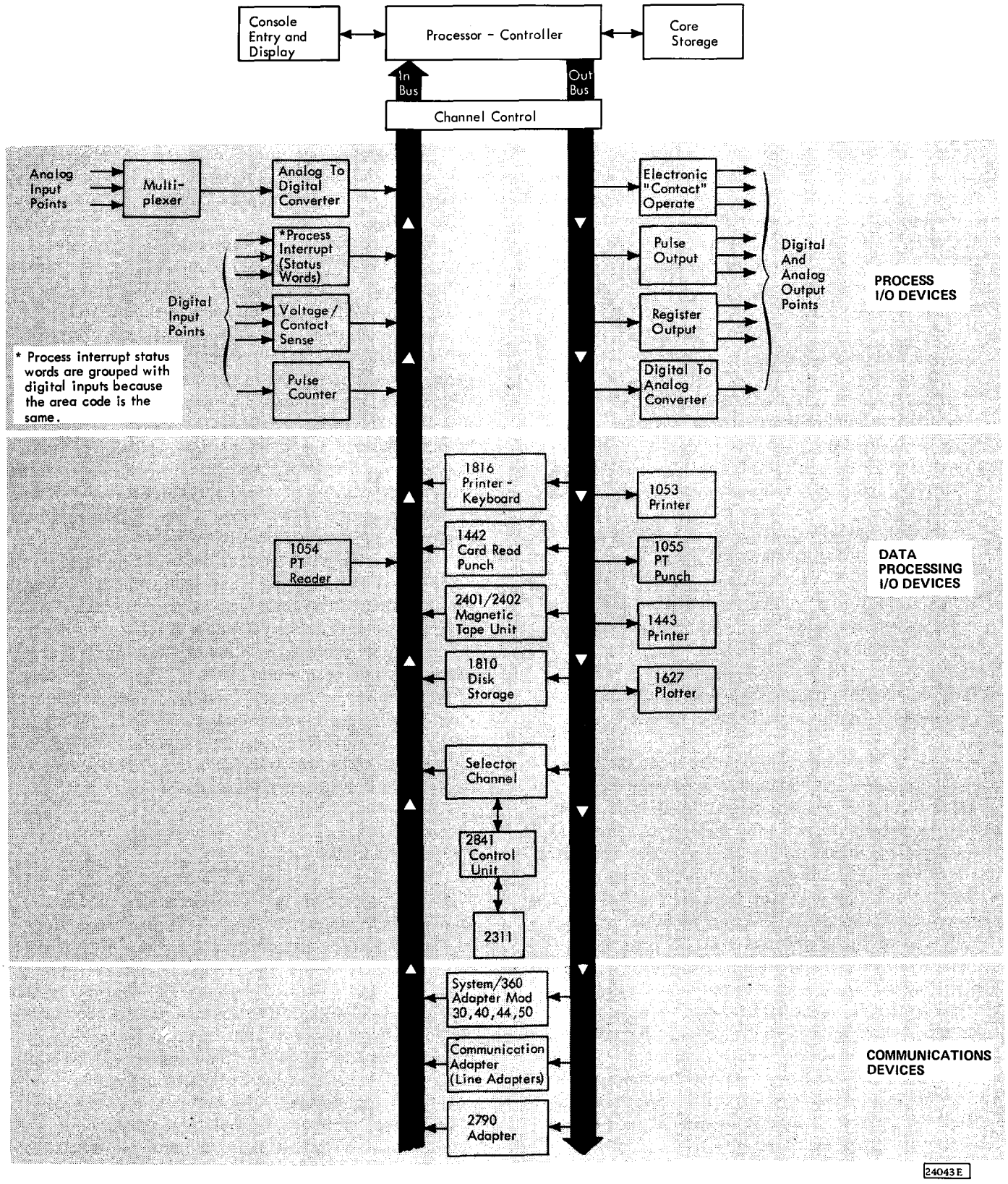


Figure 1. System Data Flow

Process Control

Industrial processing applications are wide and varied, as are the degrees of control that individual processes may require. The 1800 system provides maximum flexibility in the types of process signals it accepts and the variety of output signals and data formats it produces. This allows the 1800 system to provide the degree of control required by the process. The degree of control may vary from simple data gathering and reporting to complete supervisory control where the 1800 monitors and controls the complete process.

High-Speed Data Acquisition

A high-speed data acquisition system may be thought of as a monitoring and controlling facility used to acquire, evaluate, and record data developed during the testing of a system (or assembly, subassembly, or component). Here "system" refers to anything from an anesthetized animal in the research laboratory to a Saturn V booster on a test stand.

Many types of data acquisition systems are used. Some merely send data directly from instrumentation to magnetic tape with a minimum of "quick look" information, data editing, or checking. However, as experimental work on large systems has become more complex and time consuming, a trend toward data acquisition systems with more sophisticated data reduction and real-time display capabilities has occurred. Many systems now include the facilities to automate the data gathering and to reduce the volume of raw data. Data acquisition systems most readily meet these requirements when the system is based on a digital computer.

The 1800 system handles widely divergent applications which involve real-time data acquisition and processing abilities. Inputs may include signals from both digital and analog sources. If desired, the results of analyzing the required data may be displayed in analog or digital form, or used to cause direct functions.

Data Communications

The 1800/2790 Data Communications System combines the sensor-based capabilities of the 1800 system and the man-machine interface of the 2790 system. This system features a high-speed two-way data communications network that accommodates a large volume of short messages from many in-house data entry unit or area station locations to a central processing area. This system has typical applications in manufacturing installations: it can be used for attendance recording, material control, and production control.

Effective production control requires that management know the status of work flow through the various steps of a manufacturing process. Data entry units located at appropriate locations and check points can be used to dynamically record the time spent on each operation, work pile-ups, quantity of parts flow, and so on. This information can be utilized by management to determine the need for additional capacity at specific steps of the operation or the need to shift work load to new areas. Shop load status can be used in determining standard lead times for production scheduling.

Processor-Controllers

The processor-controller (1801 or 1802) is a fixed word-length binary computer that serves as the nerve center of the 1800 system. The ability of a processor-controller to ask for and accept input data, perform the analysis or calculations required, and produce the desired output results is due to the many functional elements of the machine.

The following descriptions pertain to core storage, the aspects of addressing core storage, the formats in which data and instructions are stored and used, the functions of processor-controller registers, and processor-controller data flow.

CORE STORAGE

The 1800 system main storage uses magnetic cores for data and program instruction storage. Each addressable core storage location contains 18 bit positions and is called a word. One of the 18 bits in a word is used for storage protection and one bit is used for parity checking. The remaining 16 bits in each word are data bits.

Five core storage sizes are available in the processor-controller. The IBM 1803 Core Storage Unit provides facilities for an additional four core storage sizes for the system, bringing the total number of sizes to nine. System core storage sizes and cycle times -- the time required to transfer a word to or from a core storage location -- are as follows:

Storage Size (18-bit words)	Storage Cycle Time
4,096	2 or 4 μs
8,192	2 or 4 μs
16,384	2 or 4 μs
24,576	2 or 4 μs
32,768	2 or 4 μs
40,960	2.25 μs
49,152	2.25 μs
57,344	2.25 μs
65,536	2.25 μs

In systems with core storage capacities above 32,768 words, the processor-controller contains 24,576 words of core storage and an 1803 adapter. The 1803 contains either 16,384, 24,576, 32,768, or 40,960 words of core storage depending on which 1803 model is ordered.

Addressing

The processor-controller uses the binary (base 2) numbering system, with internal addressing and console displays in 16-bit binary form. However, for greater ease of operation, programming systems for the 1800 use hexadecimal base 16 notation. This and other notations are shown in Figure 2. Throughout this publication, hexadecimal numbers are preceded by a /.

Core storage addresses consist of 16 bits, providing a /0000 to /FFFF address spectrum. On systems with 32,768 storage words or fewer, not all 16 bits of a storage address are needed to address all available storage positions. The excess storage address bits are ignored, as shown in the following illustration.

Storage Size (18-Bit Words)	Storage Address Bits															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
4,096	▒	▒	▒	▒												
8,192	▒	▒	▒													
16,384	▒	▒														
24,576	▒															
32,768	▒															

▒ Means bit is ignored.

Systems with greater than 32,768 words use all 16 bits.

17857

The programmer should be aware that an address above actual core storage size does not cause an error condition or inhibit access to core storage. The excess storage address bits are ignored, as shown in the preceding illustration, and the core storage location selected by the address bits not ignored is actually addressed.

The address of the first location in core storage is always /0000. The address of the last location in core storage depends on core storage size. The ending core storage address for the various sizes of core storage is shown in Figure 2. During system

Core Storage Address Notation		
Base 10	Base 2	Base 16
4095	XXXX 1111 1111 1111	0FFF
8191	XXX1 1111 1111 1111	1FFF
16383	XX11 1111 1111 1111	3FFF
24575	X101 1111 1111 1111	5FFF
32767	X111 1111 1111 1111	7FFF
40959	1001 1111 1111 1111	9FFF
49151	1011 1111 1111 1111	BFFF
57343	1101 1111 1111 1111	DFFF
65535	1111 1111 1111 1111	FFFF

X Means bit is ignored 178111

Figure 2. Address Notation

operation, sequential core storage addresses are used to read instructions from core storage for execution and during transfer of data to or from core storage. The core storage address may be increased or decreased through the full address spectrum (/0000 through /FFFF). Depending on core storage size, multiple excursions through portions of core storage or wraparound may occur more than once with one pass through the address spectrum. Wraparound occurs when the first core storage location (/0000) appears contiguous with the last core storage location.

Figure 3 illustrates how wraparound occurs for each core storage size. Note the unique differences in the 24,576; 40,960; 49,152; and 57,344 word models.

Reserved Storage Locations

Some core storage locations are reserved for exclusive use by specific features of the processor-controller. Reserved locations and the features they are reserved for are as follows:

Storage Location	Feature
/0001	CE interrupt
/0002	CE interrupt
/0004	Interval timer A
/0005	Interval timer B
/0006	Interval timer C
/0008 - /0022	Interrupt addresses

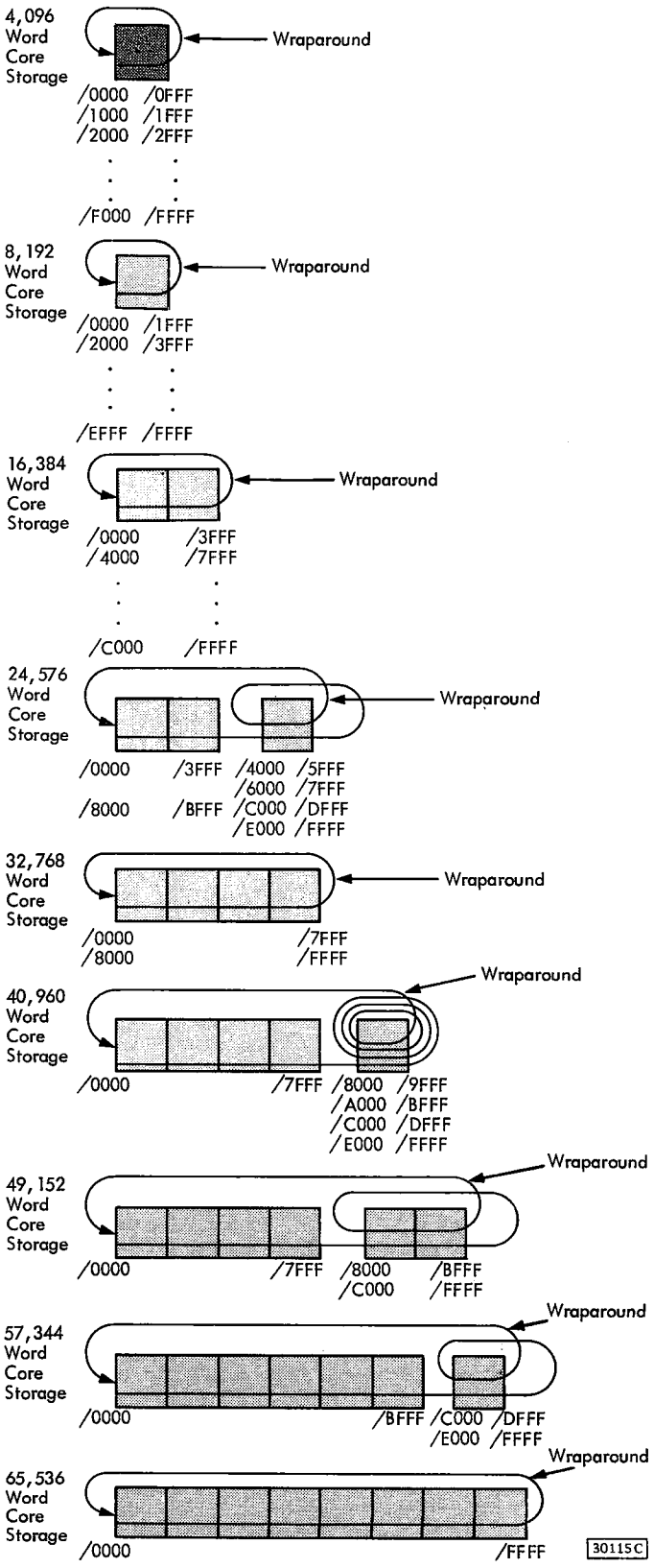
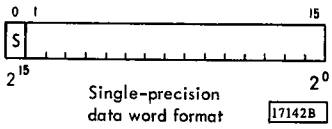


Figure 3. Address Wraparound

DATA REPRESENTATION

The standard or single precision data word is 16 bits in length as shown in the following illustration. The sign bit (position 0) is always 0 for positive numbers and 1 for negative numbers. Positive numbers are

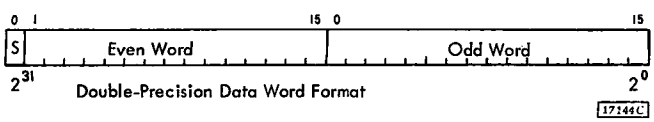


always in true binary form, whereas negative numbers are in 2's complement form. The 2's complement of a binary number is defined as its 1's complement increased by one. The 1's complement of a binary number is the number that results by replacing each 1 in the number (including sign) with a 0 and each 0 with a 1. The following example illustrates the 2's complement procedure.

Positive number	0001101001001100
1's complement	1110010110110011
Add 1	1
Resulting 2's complement	1110010110110100

Bit positions 1 through 15 of a single precision data word represent decimal values of 2^{14} through 2^{0} respectively. Thus the largest single precision positive number that can be represented is $2^{15}-1$ or 32,767 (a sign bit of 0 and 1's in all other bit positions). The largest negative number is -2^{15} or -32,768 (a sign bit of 1 and 0's in all other bit positions). The number zero is represented by all bits being 0. There is no negative zero.

A double precision data word, as shown in the following illustration, can also be used. The double precision data word consists of 32 bits, extending the maximum positive number that can be represented to 2,147,483,647 ($2^{31}-1$) and the maximum negative number to -2,147,483,648 (-2^{31}). Two adjacent words in core storage must be used, with the leftmost word at an even address and the rightmost word at the next sequential (odd) address.



REGISTERS

The following registers are used in the manipulation of data and can be displayed on the processor-controller console. These registers are also used uniquely in specific operations described later.

Index Registers

Three index registers (XR) are standard features of the processor-controller. The XR's are addressed by the tag bits (positions 6 and 7) of an instruction as follows:

Tag Bits	XR
01	1
10	2
11	3

Operations on an XR, such as load, store, or modify, are accomplished through instructions in the basic instruction set. The contents of an XR or of the instruction register (I) are usually used to perform address modification.

Storage Address Register

All processor-controller references to storage are under direct control of the storage address register (SAR). Data channel references to storage are under control of the channel address register (CAR) for the active data channel. (See "Data Channel Control.")

Instruction Register

The instruction (I) register has 16 positions and holds the address of the next instruction to be executed. The contents of the I-register are automatically increased for sequential operation of instructions.

Storage Buffer Register

The 16-bit storage buffer register (B) is used for buffering all word transfers with core storage. All data enters or leaves core storage via the B-register.

Arithmetic Factor Register

The 16-bit arithmetic factor register (D) is used to hold one operand for arithmetic and logical operations. The accumulator provides the other factor.

Accumulator

The accumulator (A) is a 16-bit register that contains the results of any arithmetic operation. It can be loaded from or stored into core storage, shifted right or left, and otherwise manipulated by specific arithmetic and logical instructions.

Contents of the accumulator are changed by some instructions that do not indicate specific accumulator operations.

Accumulator Extension

The accumulator extension (Q) is a 16-bit low-order extension of the accumulator. It is used during multiply, divide, shifting, and double precision arithmetic.

Shift Control Counter

This six-bit counter is used primarily to control shift operations.

Temporary Accumulator

The temporary accumulator (U) is a 16-bit register used to save the contents of the accumulator while the accumulator is being used for other operations such as effective address generation.

Operation Code Register

The five-bit operation code register (OP) is used to hold the operation code portion of an instruction.

ARITHMETIC OPERATIONS

The arithmetic operations of the processor-controller include add, subtract, multiply, and divide. Negative data is always stored and operated upon in 2's complement form. Addition and subtraction can be done in single or double precision. Multiplication operates on two single precision words to produce a double precision product. Division allows the dividend to be double precision and uses a single precision divisor to produce a single precision quotient and a single precision remainder.

Overflow and Carry Indicators

The two indicators associated with the accumulator are overflow and carry. The overflow indicator can be turned on by add, subtract, or divide operations, and indicates a result larger than what can be represented in the accumulator. The overflow indicator can also be turned on by a load status instruction. Once the overflow indicator is on, it cannot be changed except by testing the indicator or by executing a load status or store status instruction.

The carry indicator provides the information that a carry from or borrow by the high-order position of the accumulator has occurred. The carry indicator is dynamic and changes with each add or subtract operation. The carry indicator is also affected by shift left, load status, store status, and compare instructions.

INSTRUCTION FORMATS

Two basic instruction word formats, shown in Figure 4, are used in the 1800 system. The bits within the instruction words are used in the following manner:

OP (Operation Code): These five bits define which operation is to be performed by the processor-controller.

F (Format): This bit controls the instruction word format. When F is 0, the instruction is a single word in length and is referred to as a short instruction. When F is 1, the instruction is two words in length and is referred to as a long instruction.

T (Tag): These two bits specify the base register (an index register, the instruction register, or address portion of a long instruction) used in address modification, or the location (an index register or displacement) of the shift count.

DISP (Displacement): During address modification, these eight bits are usually added to the instruction

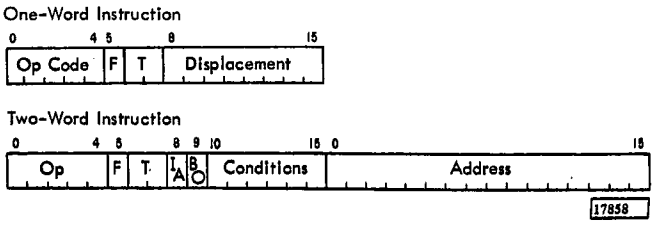


Figure 4. Instruction Formats

register or the index register specified by the tag bits. The modified address is defined as the effective address (EA). (See "Effective Address Generation" in this section.)

If negative, the displacement is in 2's complement form, with the sign in bit position 8. The sign is automatically extended to the higher-order bits (0 through 7) when the displacement is used in EA generation, or as an add-to-core-storage operand.

IA (Indirect Address): This bit is used only in long instructions. If IA is 0, addressing is direct. If IA is 1, addressing is indirect. Indirect addressing is explained under "Effective Address Generation" in this section. (See load index and modify index and skip instructions for exceptions.)

BO (Branch Out): This bit is used with store status, branch or skip on condition, and modify index and skip instructions. Refer to the individual instructions for the functions of this bit.

COND (Condition): These bits specify the conditions that are interrogated during a BSC or BSI instruction.

ADDRESS: These 16 bits usually specify a core storage address in a long instruction. The contents of these bits can be used in effective address generation.

EFFECTIVE ADDRESS GENERATION

The location of a single or double precision word referred to in an instruction is denoted by an address. Most program instructions tell the processor-controller to obtain data at a specified address and perform a certain operation on it. The versatility of the processor-controller allows the address in the instruction being executed to be modified as the specific occasion requires. This modified address is called the effective address.

The effective address (EA) is developed as shown in Figure 5 for most instructions. Exceptions are noted in the "Instruction Set" section.

PROCESSOR-CONTROLLER DATA FLOW

As shown in Figure 6, all instructions and data entering and leaving core storage do so via the B-register. Input devices send data and instructions to the B-register via the in bus. Output devices receive data from the B-register via the out bus.

	Direct Addressing		Indirect Addressing
	F=0	F=1, IA=0	F=1, IA=1
T=00	EA=I+DISP	EA=Addr	EA=V in CSL at Addr
T=01	EA=XR1+DISP	EA=Addr+XR1	EA=V in CSL at "Addr+XR1"
T=10	EA=XR2+DISP	EA=Addr+XR2	EA=V in CSL at "Addr+XR2"
T=11	EA=XR3+DISP	EA=Addr+XR3	EA=V in CSL at "Addr+XR3"

CSL = Core storage location
V = Value

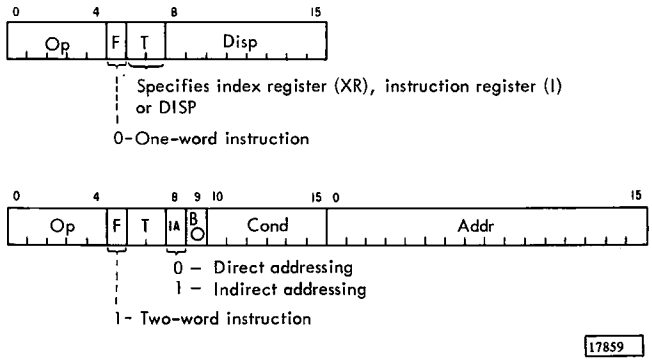


Figure 5. Effective Address Generation

As each stored program instruction is selected, its various parts (Op code, format bit, etc.) are directed to the control registers via the B-register and the out bus. The control registers decode and interpret each instruction before the instruction is executed.

Except for data channel operations (see "I/O Control" section), all instructions and data must first be addressed by the storage address register (SAR) before leaving core storage. SAR obtains the core storage address from the I-register or the A-register. The contents of the I-register are developed by one of the following methods, depending on processor-controller operation.

1. The I-register is incremented for each instruction during sequential operation of the stored program instructions.
2. The effective address of each instruction is developed in the accumulator and then transferred to SAR. The contents of the accumulator are saved in the U-register during effective address computation. If the instruction is a branch, the contents of SAR are transferred to the I-register.

Each word in core storage consists of 18 bits: 16 data bits, a parity bit (P), and a storage protect bit (S). During an operation, the P-bit is

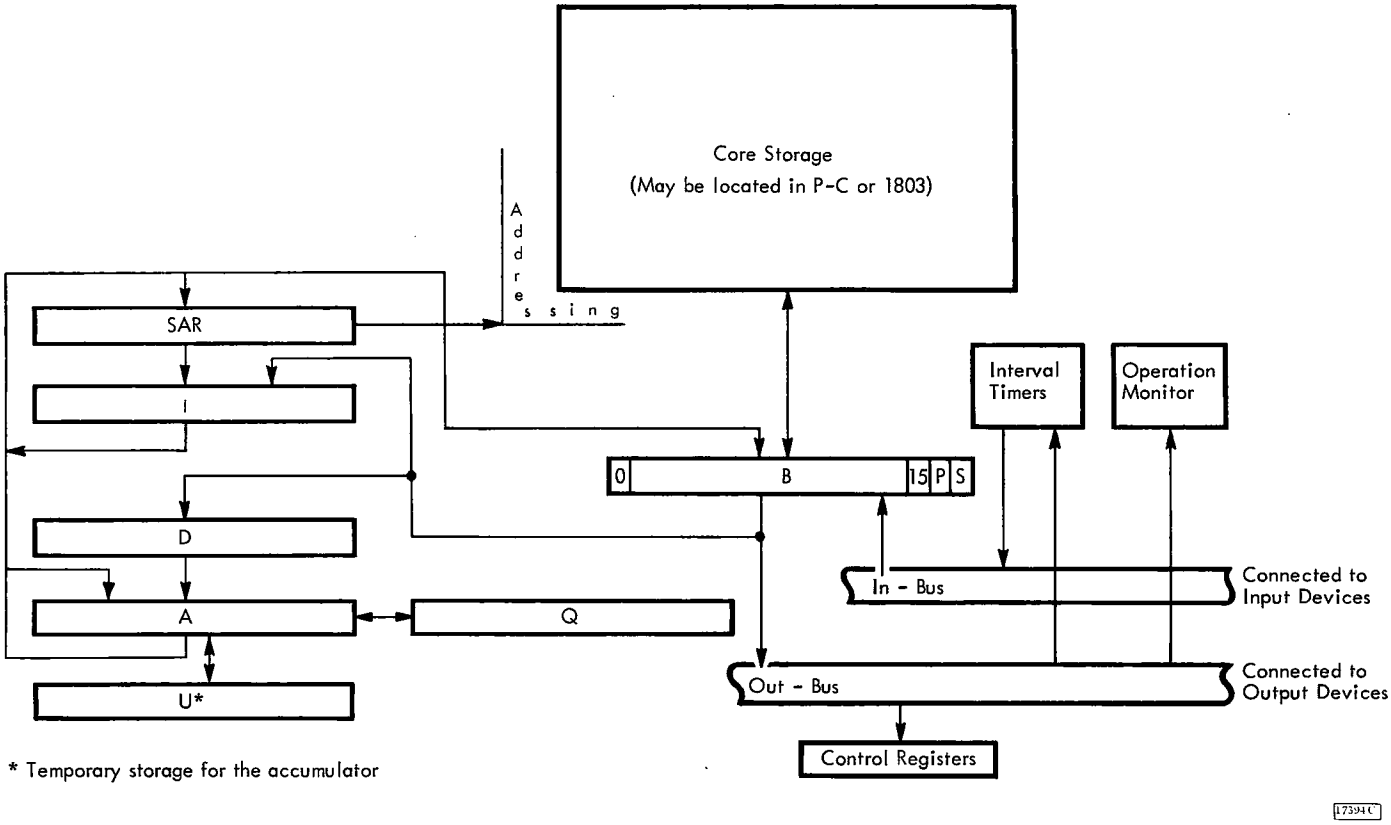


Figure 6. Processor-Controller Data Flow

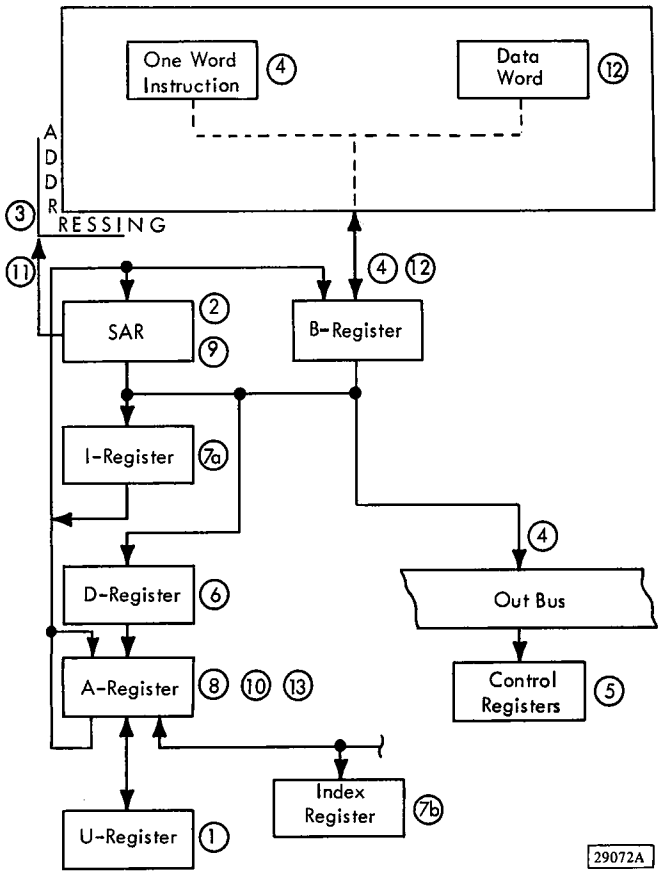
automatically added or removed to maintain odd parity. The S-bit is added or removed by the store status instruction, depending on whether a "read only" condition is desired in the core storage position. The 16 data bits enter or leave core storage via the B-register. The P- and S-bits do so via individual latches. The latches and the B-register together make possible the transfer of 18 bits to and from core storage.

The in bus and the out bus each include 16 data lines and two parity lines. This line combination permits 18-bit transfers to devices such as magnetic tape units.

DATA FLOW EXAMPLES

The following three examples illustrate the data flow for the load accumulator instruction. An example for each type of addressing (short format; long format, direct addressing; long format, indirect addressing) is included. The circled numbers in each illustration correspond to the numbered items included for that illustration.

Short Instruction



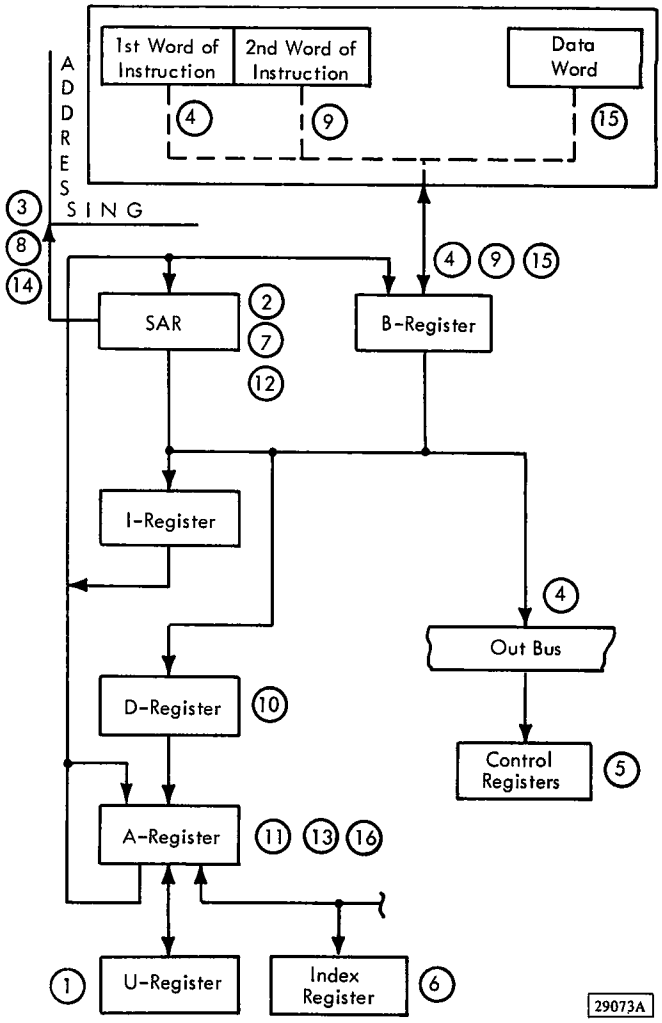
Instruction Cycle

1. A-register transfer to U-register.
2. I-register transfers to SAR. (I-register contents are then increased by 1).
3. SAR addresses the core storage location containing the instruction.
4. Core storage location transfers to the B-register and out-bus.
5. Control registers store various parts of the instruction (Op code, format bit, and tag bits).
6. Displacement is stored in the D-register.
7. a. If tag = 00, I-register transfers to A-register.
   b. If tag ≠ 00, the specified XR transfers to A-register.
8. Displacement (D-register) is added to A-register.

Execute Cycle

9. A-register transfers to SAR (effective address).
10. U-register transfers to A-register.
11. SAR addresses data word.
12. Data word transfers to B-register.
13. B-register loads into A-register (through D-register).

Long Instruction, Direct Addressing



Instruction Cycle 1

1. A-register transfers to U-register.
2. I-register transfers to SAR. (I-register contents are then increased by 1.)
3. SAR addresses the first word of the instruction.
4. First word of the instruction transfers to B-register and out bus.
5. Control registers store various parts of the instruction (Op code, format bit, and tag bits).
6. If tag ≠ 00, the specified XR transfers to A-register.

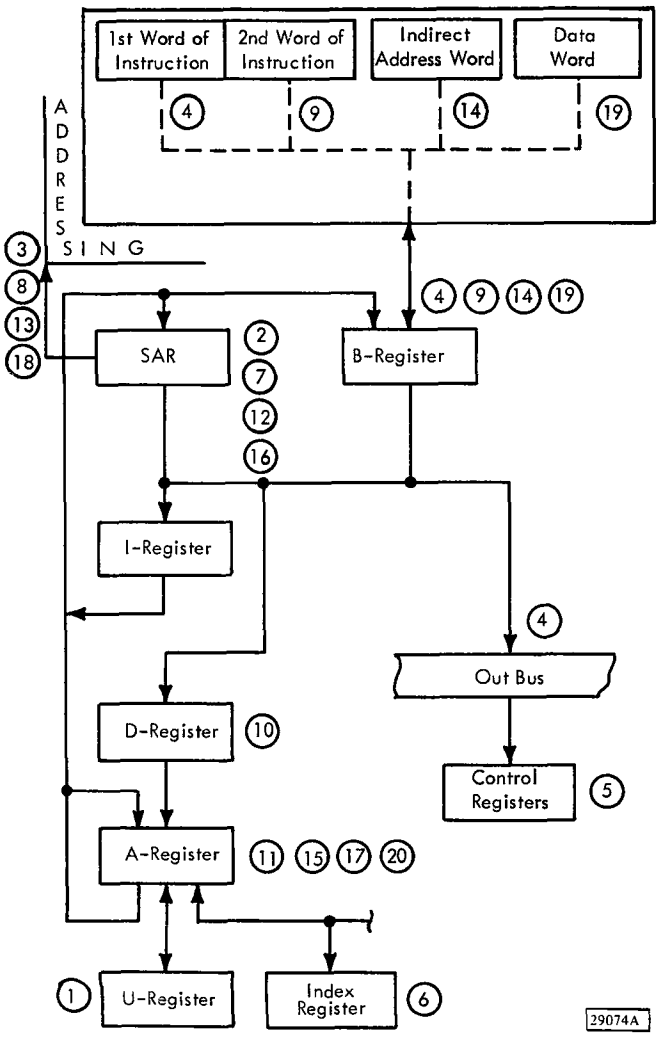
Instruction Cycle 2

7. I-register transfers to SAR. (I-register contents are then increased by 1.)
8. SAR addresses second word of instruction.
9. Second word of instruction (address) transfers to B-register.
10. Address (from B-register) is stored in D-register.
11. a. If tag = 00, D-register transfers to A-register.
    b. If tag ≠ 00, D-register is added to A-register. (A-register contains contents of XR.)

Execute Cycle

12. A-register transfers to SAR (effective address).
13. U-register transfers to A-register.
14. SAR addresses data word at effective address.
15. Data word transfers to B-register.
16. B-register loads into A-register (through D-register).

Long Instruction, Indirect Addressing



Instruction Cycle 1

1. A-register transfers to U-register.
2. I-register transfers to SAR. (I-register contents are then increased by 1.)
3. SAR addresses first word of the instruction.
4. First word of instruction transfers to the B-register and out bus.
5. Control registers store various parts of the instruction (Op code, format bit, and tag bits).
6. If tag ≠ 00, the specified XR transfers to A-register.

Instruction Cycle 2

7. I-register transfers to SAR. (I-register contents are then increased by 1.)
8. SAR addresses second word of instruction.
9. Second word of instruction (address) transfers to B-register.
10. Address (from B-register) is stored in D-register.
11. a. If tag = 00, D-register transfers to A-register.
    b. If tag ≠ 00, D-register is added to A-register. (A-register contains contents of XR).

Indirect Addressing Cycle

12. A-register transfers to SAR.
13. SAR addresses core storage location at address (or address + XR).
14. Core storage location transfers to B-register.
15. B-register transfers to A-register (through D-register).

Execute Cycle

16. A-register transfers to SAR.
17. U-register transfers to A-register.
18. SAR addresses data word at effective address.
19. Data word transfers to B-register.
20. B-register transfers to A-register (through D-register).

Instruction Set

The 1800 system instruction set is divided into five classes of instructions. Figure 7 shows the class, name, indirect addressing capability, and mnemonic for each instruction. A more complete breakdown of each instruction, including hexadecimal representations and assembler language coding examples, is given on the page referenced in Figure 7. A summary of the instruction set is given in Appendix A for quick reference. Instruction execution times are given at the end of this section.

Class	Instruction	Indirect Addressing	Mnemonic	Page
Load and Store	Load Accumulator	Yes	LD	16
	Load Double	Yes	LDD	17
	Store Accumulator	Yes	STO	18
	Store Double	Yes	STD	19
	Load Index	**	LDX	20
	Store Index	Yes	STX	21
	Load Status	No	LDS	24
	Store Status	Yes	STS	23
Arithmetic	Add	Yes	A	25
	Add Double	Yes	AD	26
	Subtract	Yes	S	27
	Subtract Double	Yes	SD	28
	Multiply	Yes	M	29
	Divide	Yes	D	30
	AND	Yes	AND	31
	OR	Yes	OR	32
	Exclusive OR	Yes	EOR	33
Shift	Shift Left Instructions			
	Shift Left Logical (A) *	No	SLA	34
	Shift Left Logical (AQ)*	No	SLT	35
	Shift Left and Count (AQ)*	No	SLC	37
	Shift Left and Count (A)*	No	SLCA	36
	Shift Right Instructions			
	Shift Right Logical (A)*	No	SRA	38
	Shift Right Arithmetically (AQ)*	No	SRT	39
	Rotate Right (AQ)*	No	RTE	40
Branch	Branch and Store I	Yes	BSI	43
	Branch or Skip on Condition	Yes	BSC(BOSC)	41
	Modify Index and Skip	**	MDX	45
	Wait	No	WAIT	47
	Compare	Yes	CMP	48
	Double Compare	Yes	DCM	49
I/O	Execute I/O	Yes	XIO	50

* Letters in parentheses indicate registers involved in shift operations.
** See the section for the individual instruction (MDX and LDX).

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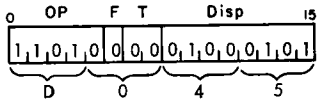
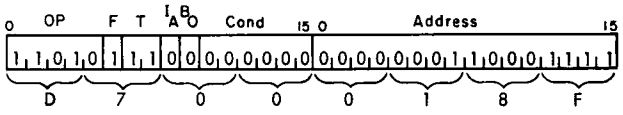
Figure 7. Instruction Set

Hexadecimal Representation





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The hexadecimal representation(s) of each instruction is given with its format(s) and assembler language coding examples. As shown in the preceding example, the hexadecimal number is derived by dividing each word of the instruction into groups of four bits each, and assigning a hexadecimal value corresponding to the binary coded decimal (BCD) value of each group.

Description Symbology

Symbols are used in the descriptions and examples for the instruction. The symbols and their meanings are as follows:

Symbol	Meaning
A	Accumulator
Q	Accumulator extension
Addr	Contents of address portion of a two-word instruction
CSL	Core storage location
Disp	Contents of displacement portion of a one-word instruction
EA	Effective address (see Figure 5)
EA+1	Next higher address from the effective address
I	Contents of the instruction (I) register
V	Value
XR1	Contents of index register 1
XR2	Contents of index register 2
XR3	Contents of index register 3
X	Hexadecimal value (can be 0-F)

Symbol	Meaning
*	Used for hexadecimal values that have limits. Limits are given with each instruction.

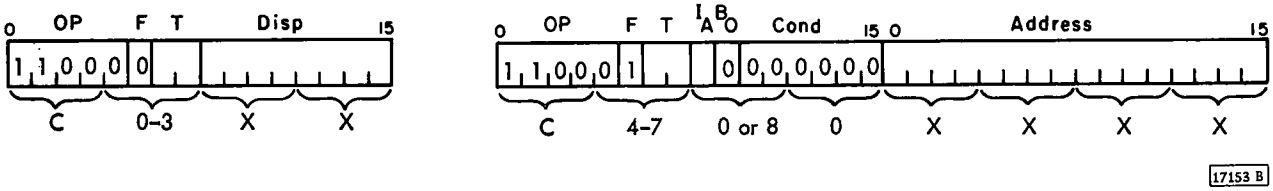
Assembler Language Coding Examples

Assembler language coding examples are provided with each instruction to illustrate the relationship between the assembler language coding and the actual machine language instructions. No attempt is made to explain or define all aspects of assembler language programming. Refer to IBM 1800 Assembler Language, Order No. GC26-5882, for assembler language information.

The assembler language coding examples for short instructions in this section are shown with the label DISP in the operand field. Note that with a short instruction in which an index register is not specified, the operand may reference a relocatable label. However, the label must be located within -128 or +127 words of the referencing instruction. With a short instruction in which an index register is specified, the operand must be an absolute value or a computed absolute value. (A computed absoluted value is a relocatable value minus another relocatable value.)

LOAD ACCUMULATOR (LD)

FORMATS



DESCRIPTION

The accumulator (A) is loaded with the contents of the core-storage location specified by the effective address (EA) of the instruction. The contents of the core-storage location are unchanged.

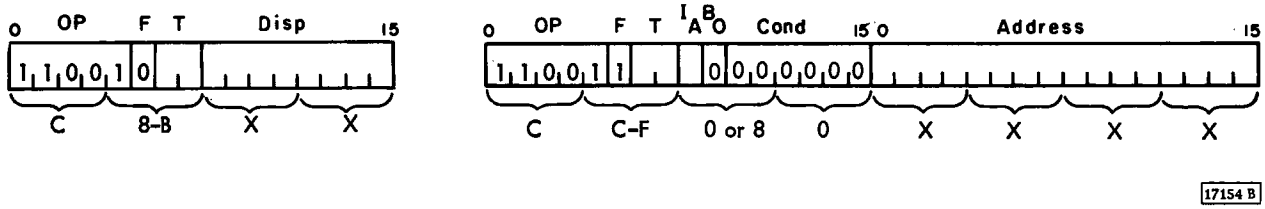
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label 21–25	Operation 27–30	F 32	T 33	35–40	See Note	Hexadecimal Value	Description	Format
	LD			DISP		C0XX	Contents of CSL at EA (I + DISP) are loaded into A	Short Instruction
	LD		I	DISP		C1XX	Contents of CSL at EA (XR1 + DISP) are loaded into A	
	LD		2	DISP		C2XX	Contents of CSL at EA (XR2 + DISP) are loaded into A	
	LD		3	DISP		C3XX	Contents of CSL at EA (XR3 + DISP) are loaded into A	
	LD	L		ADDR		C400XXXX	Contents of CSL at EA (Addr) are loaded into A	Long Instruction Direct Addressing
	LD	L	I	ADDR		C500XXXX	Contents of CSL at EA (Addr + XR1) are loaded into A	
	LD	L	2	ADDR		C600XXXX	Contents of CSL at EA (Addr + XR2) are loaded into A	
	LD	L	3	ADDR		C700XXXX	Contents of CSL at EA (Addr + XR3) are loaded into A	
	LD	I		ADDR		C480XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A	
	LD	I	I	ADDR		C580XXXX	Contents of CSL at EA (V in CSL at "Addr + XR1") are loaded into A	Long Instruction Indirect Addressing
	LD	I	2	ADDR		C680XXXX	Contents of CSL at EA (V in CSL at "Addr + XR2") are loaded into A	
	LD	I	3	ADDR		C780XXXX	Contents of CSL at EA (V in CSL at "Addr + XR3") are loaded into A	

LOAD DOUBLE (LDD)

FORMATS



DESCRIPTION

The accumulator (A) and its extension (Q) are loaded with the contents of the core-storage location specified by the effective address (EA) of the instruction and the next higher core-storage location (EA + 1), respectively. This provides double-precision load for use with double-precision arithmetic. The EA of the instruction must be an even address in order for the instruction to perform as described. If the EA is odd, A and Q are both loaded with the contents of the core-storage location specified by the EA. In any case, the contents of the core-storage locations are unchanged.

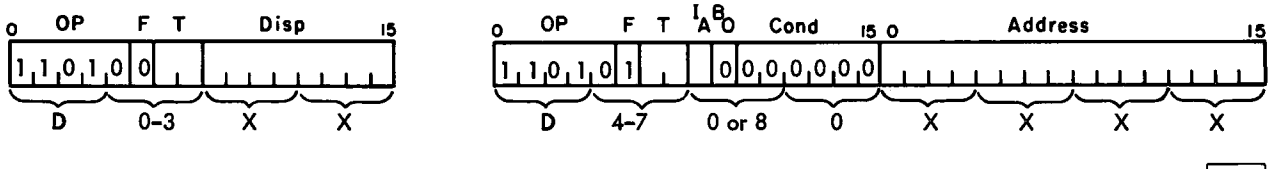
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	LDD			DISP		C8XX	Contents of CSL at EA (I + DISP) and EA + 1 are loaded into A and Q	Short Instruction
	LDD		I	DISP		C9XX	Contents of CSL at EA (XR1 + DISP) and EA + 1 are loaded into A and Q	
	LDD		2	DISP		CAXX	Contents of CSL at EA (XR2 + DISP) and EA + 1 are loaded into A and Q	
	LDD		3	DISP		CBXX	Contents of CSL at EA (XR3 + DISP) and EA + 1 are loaded into A and Q	
	LDD	L		ADDR		CC00XXXX	Contents of CSL at EA (Addr) and EA + 1 are loaded into A and Q	Long Instruction Direct Addressing
	LDD	L	I	ADDR		CD00XXXX	Contents of CSL at EA (Addr + XR1) and EA + 1 are loaded into A and Q	
	LDD	L	2	ADDR		CE00XXXX	Contents of CSL at EA (Addr + XR2) and EA + 1 are loaded into A and Q	
	LDD	L	3	ADDR		CF00XXXX	Contents of CSL at EA (Addr + XR3) and EA + 1 are loaded into A and Q	
	LDD	I		ADDR		CC80XXXX	Contents of CSL at EA (V in CSL at Addr) and EA + 1 are loaded into A and Q	Long Instruction Indirect Addressing
	LDD	I	I	ADDR		CD80XXXX	Contents of CSL at EA (V in CSL at "Addr + XR1") and EA + 1 are loaded into A and Q	
	LDD	I	2	ADDR		CE80XXXX	Contents of CSL at EA (V in CSL at "Addr + XR2") and EA + 1 are loaded into A and Q	
	LDD	I	3	ADDR		CF80XXXX	Contents of CSL at EA (V in CSL at "Addr + XR3") and EA + 1 are loaded into A and Q	

STORE ACCUMULATOR (STO)

FORMATS



DESCRIPTION

The contents of the accumulator (A) are stored in the core-storage location specified by the effective address (EA) of the instruction. The contents of A are unchanged.

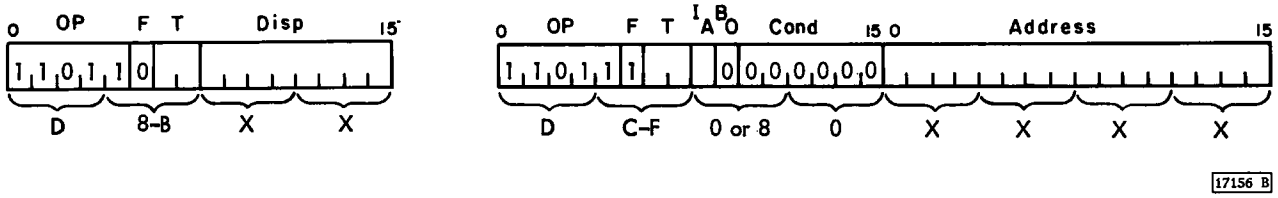
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	Hexadecimal Value	Description	Format
	STO			DISP	D0XX	Contents of A are stored in CSL at EA (I + DISP)	Short Instruction
	STO		1	DISP	D1XX	Contents of A are stored in CSL at EA (XR1 + DISP)	
	STO		2	DISP	D2XX	Contents of A are stored in CSL at EA (XR2 + DISP)	
	STO		3	DISP	D3XX	Contents of A are stored in CSL at EA (XR3 + DISP)	
	STO	L		ADDR	D400XXXX	Contents of A are stored in CSL at EA (Addr)	Long Instruction Direct Addressing
	STO	L	1	ADDR	D500XXXX	Contents of A are stored in CSL at EA (Addr + XR1)	
	STO	L	2	ADDR	D600XXXX	Contents of A are stored in CSL at EA (Addr + XR2)	
	STO	L	3	ADDR	D700XXXX	Contents of A are stored in CSL at EA (Addr + XR3)	
	STO	I		ADDR	D480XXXX	Contents of A are stored in CSL at EA (V in CSL at Addr)	Long Instruction Indirect Addressing
	STO	I	1	ADDR	D580XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr + XR1")	
	STO	I	2	ADDR	D680XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr + XR2")	
	STO	I	3	ADDR	D780XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr + XR3")	

STORE DOUBLE (STD)

FORMATS



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DESCRIPTION

The contents of the accumulator (A) and its extension (Q) are stored in the core-storage location specified by the effective address (EA) of the instruction and the next higher core-storage location (EA + 1), respectively. This provides double-precision store for use with double-precision arithmetic. The EA of the instruction must be an even address in order for the instruction to perform as described. If the EA is odd, the contents of A are stored at the EA and the contents of Q are not stored. In any case, the contents of A and Q remain unchanged.

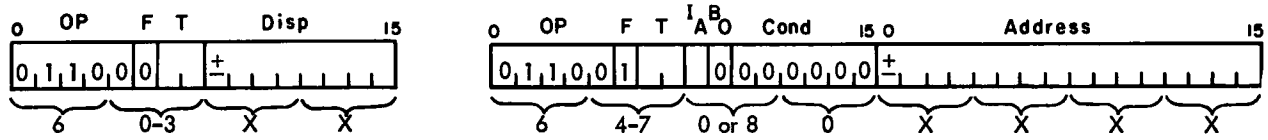
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	STD			DISP		D8XX	Contents of A and Q are stored in CSL at EA (I + DISP) and EA + 1	Short Instruction
	STD		I	DISP		D9XX	Contents of A and Q are stored in CSL at EA (XR1 + DISP) and EA + 1	
	STD		2	DISP		DAXX	Contents of A and Q are stored in CSL at EA (XR2 + DISP) and EA + 1	
	STD		3	DISP		DBXX	Contents of A and Q are stored in CSL at EA (XR3 + DISP) and EA + 1	
	STD	L		ADDR		DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA + 1	Long Instruction Direct Addressing
	STD	L	I	ADDR		DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr + XR1) and EA + 1	
	STD	L	2	ADDR		DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr + XR2) and EA + 1	
	STD	L	3	ADDR		DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr + XR3) and EA + 1	
	STD	I		ADDR		DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA + 1	Long Instruction Indirect Addressing
	STD	I	I	ADDR		DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr.+ XR1") and EA + 1	
	STD	I	2	ADDR		DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr + XR2") and EA + 1	
	STD	I	3	ADDR		DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr + XR3") and EA + 1	

LOAD INDEX (LDX)

FORMATS



T = 00 Load I T = 10 Load XR2 IA = 0 - Load Immediate
T = 01 Load XR1 T = 11 Load XR3 IA = 1 - Load Direct

17157 B

DESCRIPTION

An index register (XR) or the instruction (I) register is loaded with the displacement portion of the instruction, the address word of the instruction, or the contents of the core-storage location specified by the address word. The tag bits indicate which register is loaded. The source of the data is dependent on the instruction format; short or long. In any case, the source of data remains unchanged.

IF SHORT FORMAT (F bit is 0), the register specified by the tag bits is loaded with the displacement portion of the instruction. Before being loaded, the displacement is expanded to a 16-bit word by propagating the value of the sign bit (bit position 8 of the instruction) to the left 8 positions.

IF LONG FORMAT (F bit is 1), the IA bit of the instruction further specifies the source of data. If the IA bit is 0, the register specified by the tag bits is loaded with the address word. If the IA bit is 1, the register specified by the tag bits is loaded with the contents of the core-storage location specified by the address word.

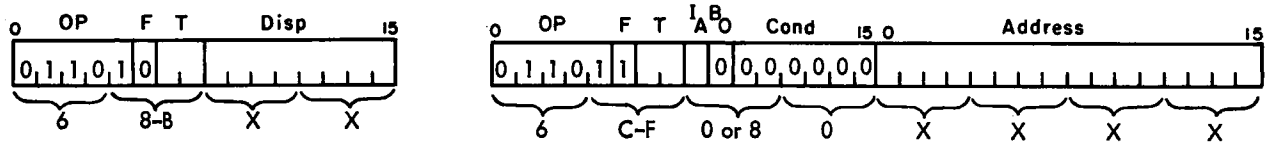
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction

EXAMPLES

Assembler Language Coding				Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F	T 32 33	35 40	See Note	Hexadecimal Value	Description	Format
	LDX			DISP		60XX	Load expanded DISP into instruction register	Short Instruction
	LDX		1	DISP		61XX	Load expanded DISP into index register 1	
	LDX		2	DISP		62XX	Load expanded DISP into index register 2	
	LDX		3	DISP		63XX	Load expanded DISP into index register 3	
	LDX	L		ADDR		6400XXXX	Load Addr into instruction register	Long Instruction Direct Addressing
	LDX	L	1	ADDR		6500XXXX	Load Addr into index register 1	
	LDX	L	2	ADDR		6600XXXX	Load Addr into index register 2	
	LDX	L	3	ADDR		6700XXXX	Load Addr into index register 3	
	LDX	I		ADDR		6480XXXX	Load contents of CSL at Addr into instruction register	Long Instruction Indirect Addressing
	LDX	I	1	ADDR		6580XXXX	Load contents of CSL at Addr into index register 1	
	LDX	I	2	ADDR		6680XXXX	Load contents of CSL at Addr into index register 2	
	LDX	I	3	ADDR		6780XXXX	Load contents of CSL at Addr into index register 3	

STORE INDEX (STX)

FORMATS



T = 00 Store I
T = 01 Store XR1
T = 10 Store XR2
T = 11 Store XR3

17160 B

DESCRIPTION

An index register (XR) or the instruction (I) register is stored in the core-storage location specified by the effective address (EA) of the instruction. The contents of the register stored remains unchanged. The tag bits specify which register is stored and therefore, cannot be used in effective address generation. The EA for a short instruction is (I + Disp). The EA for a long instruction with direct addressing (IA bit is 0) is (Addr). The EA for a long instruction with indirect addressing (IA is 1) is (value in core-storage location at Addr).

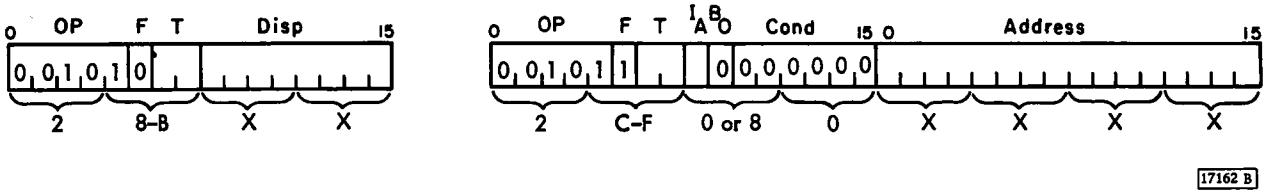
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	STX			DISP		68XX	Store I in CSL at EA (I + DISP)	Short Instruction
	STX		1	DISP		69XX	Store XR1 in CSL at EA (I + DISP)	
	STX		2	DISP		6AXX	Store XR2 in CSL at EA (I + DISP)	
	STX		3	DISP		6BXX	Store XR3 in CSL at EA (I + DISP)	
	STX	L		ADDR		6C00XXXX	Store I in CSL at EA (Addr)	Long Instruction Direct Addressing
	STX	L	1	ADDR		6D00XXXX	Store XR1 in CSL at EA (Addr)	
	STX	L	2	ADDR		6E00XXXX	Store XR2 in CSL at EA (Addr)	
	STX	L	3	ADDR		6F00XXXX	Store XR3 in CSL at EA (Addr)	
	STX	I		ADDR		6C80XXXX	Store I in CSL at EA (V in CSL at Addr)	Long Instruction Indirect Addressing
	STX	I	1	ADDR		6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)	
	STX	I	2	ADDR		6E80XXXX	Store XR2 in CSL at EA (V in CSL at Addr)	
	STX	I	3	ADDR		6F80XXXX	Store XR3 in CSL at EA (V in CSL at Addr)	

STORE STATUS (STS) Store Status Function

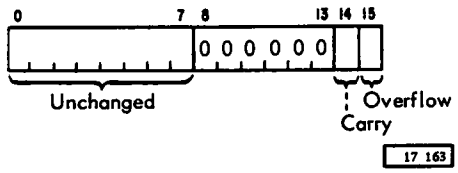
FORMATS



DESCRIPTION

The status of the carry and overflow indicators are stored in bit positions 14 and 15, respectively, of the core-storage location specified by the effective address (EA) of the instruction. The carry and overflow indicators are then reset. Bit positions 0 through 7 of the word at the EA remain unchanged and bit positions 8 through 13 are reset to 0's as shown in the illustration.

If the long format is used, bit 9 (BO) of the instruction must be 0 for a store status function; otherwise a write or clear storage protect bit function is performed as described on the next page.



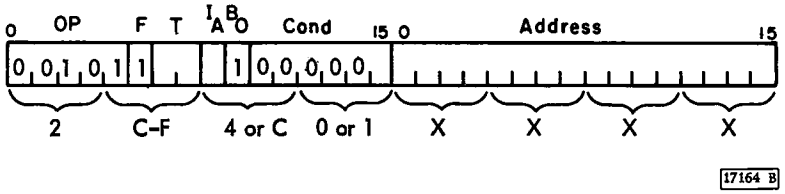
THE CARRY AND OVERFLOW INDICATORS are reset as they are stored.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	Hexadecimal Value	Description	Format
	STS			DISP	28XX	Store status of indicators in CSL at EA (I + DISP)	Short Instruction
	STS		1	DISP	29XX	Store status of indicators in CSL at EA (XR1 + DISP)	
	STS		2	DISP	2AXX	Store status of indicators in CSL at EA (XR2 + DISP)	
	STS		3	DISP	2BXX	Store status of indicators in CSL at EA (XR3 + DISP)	
	STS	L		ADDR	2C00XXXX	Store status of indicators in CSL at EA (Addr)	Long Instruction Direct Addressing
	STS	L	1	ADDR	2D00XXXX	Store status of indicators in CSL at EA (Addr + XR1)	
	STS	L	2	ADDR	2E00XXXX	Store status of indicators in CSL at EA (Addr + XR2)	
	STS	L	3	ADDR	2F00XXXX	Store status of indicators in CSL at EA (Addr + XR3)	
	STS	I		ADDR	2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)	Long Instruction Indirect Addressing
	STS	I	1	ADDR	2D80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr + XR1")	
	STS	I	2	ADDR	2E80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr + XR2")	
	STS	I	3	ADDR	2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr + XR3")	

STORE STATUS (STS) Write or Clear Storage Protect Bit Function

FORMAT



DESCRIPTION

The storage protect bit in the core-storage location specified by the effective address (EA) of the instruction is written or cleared as indicated by bit position 15 of the instruction being 1 or 0, respectively.

A long format instruction (F bit is 1) must be used and bit 9 (BO) of the instruction must be 1 for a write or clear storage protect bit function; otherwise a store status function is performed as described on the preceding page.

The preceding description of the write or clear storage protect bit function is performed only if the write storage protect bits switch on the P-C console is positioned on YES. As long as this switch is on YES, the program has the ability to write or clear storage protect bits as described in the preceding paragraphs. If the switch is on NO, this instruction performs as a no-op (no-operation).

THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

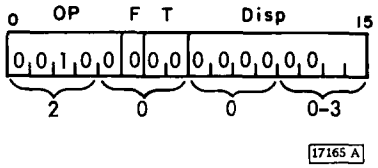
EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	STS	L		ADDR,/40	[1]	2C40XXXX	Clear storage protect bit in CSL at EA (Addr)	Long Instruction Direct Addressing
	STS	L		ADDR,/41		2C41XXXX	Write storage protect bit in CSL at EA (Addr)	
	STS	L	1	ADDR,/40		2D40XXXX	Clear storage protect bit in CSL at EA (Addr+XR1)	
	STS	L	1	ADDR,/41		2D41XXXX	Write storage protect bit in CSL at EA (Addr+XR1)	
	STS	L	2	ADDR,/40		2E40XXXX	Clear storage protect bit in CSL at EA (Addr+XR2)	
	STS	L	2	ADDR,/41		2E41XXXX	Write storage protect bit in CSL at EA (Addr+XR2)	
	STS	L	3	ADDR,/40		2F40XXXX	Clear storage protect bit in CSL at EA (Addr+XR3)	
	STS	L	3	ADDR,/41		2F41XXXX	Write storage protect bit in CSL at EA (Addr+XR3)	
	STS	I		ADDR,/40		2CC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at Addr)	Long Instruction Indirect Addressing
	STS	I		ADDR,/41		2CC1XXXX	Write storage protect bit in CSL at EA (V in CSL at Addr)	
	STS	I	1	ADDR,/40		2DC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR1")	
	STS	I	1	ADDR,/41		2DC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR1")	
	STS	I	2	ADDR,/40		2EC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR2")	
	STS	I	2	ADDR,/41		2EC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR2")	
	STS	I	3	ADDR,/40		2FC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR3")	
	STS	I	3	ADDR,/41		2FC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR3")	

[1] With MPX Version 3, the storage protect operand (/40 and /41) can be symbolically represented by U and P, respectively.

LOAD STATUS (LDS)

FORMAT



DESCRIPTION

The carry and overflow indicators are loaded with the status of bit positions 14 (carry) and 15 (overflow) of the instruction. A 1 bit sets the respective indicator on, and a 0 bit sets the respective indicator off. Normally the carry and overflow status were previously stored in this instruction by a store status instruction. The statuses of bit positions 14 and 15 of the load status instruction are not changed during execution of the instruction. This instruction applies to the short format only.

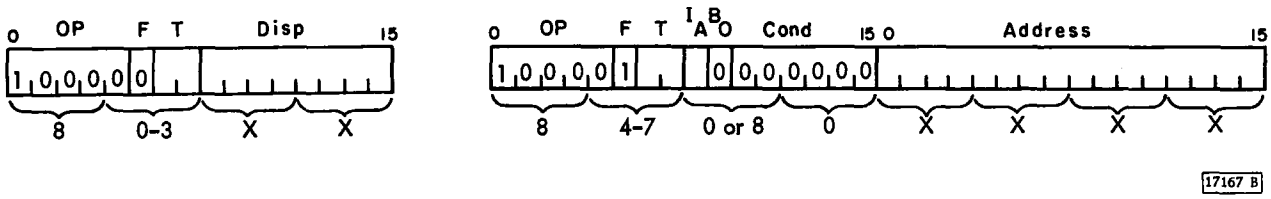
THE CARRY AND OVERFLOW INDICATORS are set according to bit positions 14 and 15 of the instruction, respectively.

EXAMPLES

Assembler Language Coding						Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	LDS			0		2000	Set carry and overflow indicators off	Short Instruction
	LDS			1		2001	Set overflow on and carry off	
	LDS			2		2002	Set overflow off and carry on	
	LDS			3		2003	Set carry and overflow indicator on	

ADD (A)

FORMATS



DESCRIPTION

The contents of the core-storage location specified by the effective address (EA) of the instruction are added algebraically to the contents of the accumulator (A). The sum replaces the contents of A, while core storage remains unchanged. Negative operands and/or negative sums are both in 2's complement form. (See "Data Addition" for details of add operations.)

THE CARRY INDICATOR is turned on by a carry out of the high-order bit position of A during the add operation.

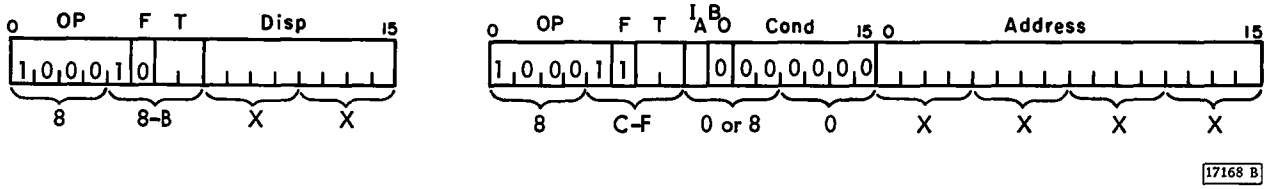
THE OVERFLOW INDICATOR is turned on if the magnitude of the sum is too large to be presented by A; that is, greater than +32,767 or less than -32,768. (This condition is detected by a resultant carry out of one and only one of the two high-order bit positions of A.) If the overflow indicator is already on, it is not changed. The overflow indicator can be reset with a load status instruction, store status instruction, or by testing the indicator with a branch or skip on condition instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	A			D,I,S,P		80XX	Add contents of CSL at EA (I + DISP) to A	Short Instruction
	A		1	D,I,S,P		81XX	Add contents of CSL at EA (XR1 + DISP) to A	
	A		2	D,I,S,P		82XX	Add contents of CSL at EA (XR2 + DISP) to A	
	A		3	D,I,S,P		83XX	Add contents of CSL at EA (XR3 + DISP) to A	
	A	L		A,D,D,R		8400XXXX	Add contents of CSL at EA (Addr) to A	Long Instruction Direct Addressing
	A	L	1	A,D,D,R		8500XXXX	Add contents of CSL at EA (Addr + XR1) to A	
	A	L	2	A,D,D,R		8600XXXX	Add contents of CSL at EA (Addr + XR2) to A	
	A	L	3	A,D,D,R		8700XXXX	Add contents of CSL at EA (Addr + XR3) to A	
	A	I		A,D,D,R		8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A	Long Instruction Indirect Addressing
	A	I	1	A,D,D,R		8580XXXX	Add contents of CSL at EA (V in CSL at "Addr + XR1") to A	
	A	I	2	A,D,D,R		8680XXXX	Add contents of CSL at EA (V in CSL at "Addr + XR2") to A	
	A	I	3	A,D,D,R		8780XXXX	Add contents of CSL at EA (V in CSL at "Addr + XR3") to A	

ADD DOUBLE (AD)

FORMATS



DESCRIPTION

Two words - - the contents of the core-storage location specified by the effective address (EA) of the instruction, and the next higher core-storage location (EA + 1) - - are added algebraically to the contents of the accumulator (A) and its extension (Q). This provides double-precision addition with A and Q considered as one 32-bit accumulator. The sum replaces the contents of A and Q, while core storage remains unchanged. Negative operands and/or negative sums are both in 2's complement form.

The effective address (EA) of the instruction must be an even address for correct operation. If the EA is odd, the contents of the core-storage location specified by the EA are added to both A and Q, and may be added incorrectly in A.

THE CARRY INDICATOR is turned on by a carry out of the high-order bit position of A during the add operation.

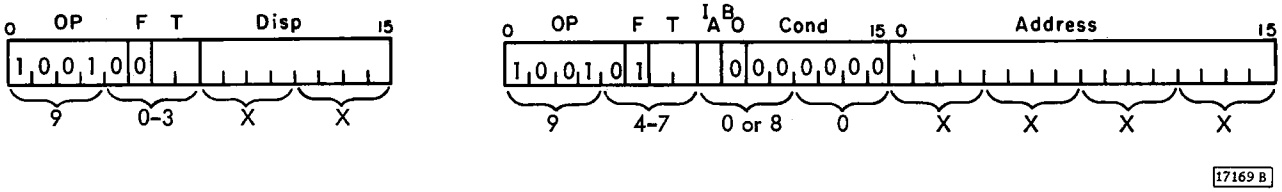
THE OVERFLOW INDICATOR is turned on if the magnitude of the sum is too large to be represented in A and Q; that is, greater than +2,147,483,647 or less than -2,147,483,648. (This condition is detected by a resultant carry out of one and only one of the two high-order bit positions of A.) If the overflow indicator is already on, it is not changed. The overflow indicator can be reset with a load status instruction, store status instruction, or by testing the indicator with a branch or skip on condition instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21 25)	Operation (27 30)	F (32)	T (33)	(35 40)	See Note	Hexadecimal Value	Description	Format
	AD			DISP		88XX	Add contents of CSL at EA (I + DISP) and EA + 1 to A and Q	Short Instruction
	AD		1	DISP		89XX	Add contents of CSL at EA (XR1 + DISP) and EA + 1 to A and Q	
	AD		2	DISP		8AXX	Add contents of CSL at EA (XR2 + DISP) and EA + 1 to A and Q	
	AD		3	DISP		8BXX	Add contents of CSL at EA (XR3 + DISP) and EA + 1 to A and Q	
	AD	L		ADDR		8C00XXXX	Add contents of CSL at EA (Addr) and EA + 1 to A and Q	Long Instruction Direct Addressing
	AD	L	1	ADDR		8D00XXXX	Add contents of CSL at EA (Addr + XR1) and EA + 1 to A and Q	
	AD	L	2	ADDR		8E00XXXX	Add contents of CSL at EA (Addr + XR2) and EA + 1 to A and Q	
	AD	L	3	ADDR		8F00XXXX	Add contents of CSL at EA (Addr + XR3) and EA + 1 to A and Q	
	AD	I		ADDR		8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA + 1 to A and Q	Long Instruction Indirect Addressing
	AD	I	1	ADDR		8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr + XR1") and EA + 1 to A and Q	
	AD	I	2	ADDR		8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr + XR2") and EA + 1 to A and Q	
	AD	I	3	ADDR		8F80XXXX	Add contents of CSL at EA (V in CSL at "Addr + XR3") and EA + 1 to A and Q	

SUBTRACT (S)

FORMATS



DESCRIPTION

The contents of the core-storage location specified by the effective address (EA) of the instruction are subtracted algebraically from the contents of the accumulator (A). The difference replaces the contents of A, while core storage remains unchanged. Negative operands and/or negative differences are both in 2's complement form.

THE CARRY INDICATOR is turned on if a borrow by the high-order bit position of A occurs during the subtract operation.

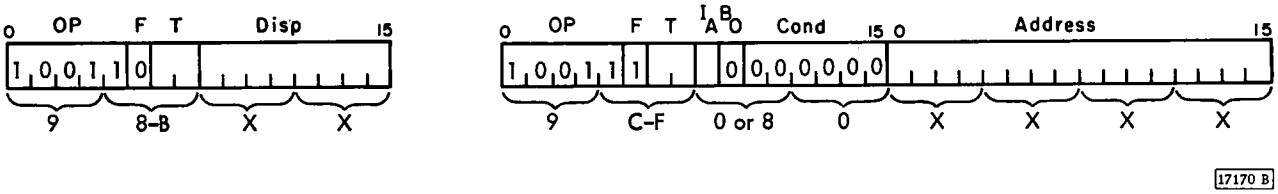
THE OVERFLOW INDICATOR is turned on if the magnitude of the difference is too large to be represented in A; that is, greater than +32,767 or less than -32,768. (This condition is detected by a borrow from one and only one of the two high-order bit positions of A.) If the overflow indicator is already on, it is not changed. The overflow indicator can be reset with a load status instruction or store status instruction, or by testing the indicator with a branch or skip on condition instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	S			D I S P		90XX	Subtract contents of CSL at EA (I + DISP) from A	Short Instruction
	S		1	D I S P		91XX	Subtract contents of CSL at EA (XR1 + DISP) from A	
	S		2	D I S P		92XX	Subtract contents of CSL at EA (XR2 + DISP) from A	
	S		3	D I S P		93XX	Subtract contents of CSL at EA (XR3 + DISP) from A	
	S	L		A D D R		9400XXXX	Subtract contents of CSL at EA (Addr) from A	Long Instruction Direct Addressing
	S	L	1	A D D R		9500XXXX	Subtract contents of CSL at EA (Addr + XR1) from A	
	S	L	2	A D D R		9600XXXX	Subtract contents of CSL at EA (Addr + XR2) from A	
	S	L	3	A D D R		9700XXXX	Subtract contents of CSL at EA (Addr + XR3) from A	
	S	I		A D D R		9480XXXX	Subtract contents of CSL at EA (V in CSL at Addr) from A	Long Instruction Indirect Addressing
	S	I	1	A D D R		9580XXXX	Subtract contents of CSL at EA (V in CSL at "Addr + XR1") from A	
	S	I	2	A D D R		9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr + XR2") from A	
	S	I	3	A D D R		9780XXXX	Subtract contents of CSL at EA (V in CSL at "Addr + XR3") from A	

SUBTRACT DOUBLE (SD)

FORMATS



17170 B

DESCRIPTION

Two words - - the contents of the core-storage location specified by the effective address (EA) of the instruction, and the next higher core-storage location (EA +1) - - are subtracted algebraically from the contents of the accumulator (A) and its extension (Q). This provides double-precision subtraction with A and Q considered as one 32-bit accumulator. The difference replaces the contents of A and Q, while core storage remains unchanged. Negative operands and/or negative differences are both in 2's complement form.

The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of the core-storage location specified by the EA are subtracted from both A and Q and may be subtracted incorrectly in A.

THE CARRY INDICATOR is turned on if a borrow by the high-order bit position of A occurs during the subtract operation.

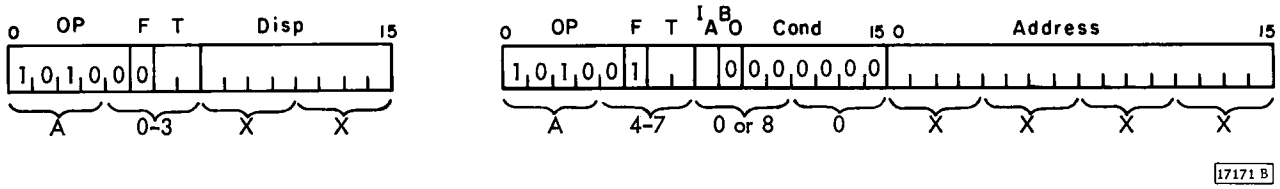
THE OVERFLOW INDICATOR is turned on if the magnitude of the difference is too large to be represented in A and Q; that is, greater than +2,147,483,647 or less than -2,147,483,648. (This condition is detected by a borrow from one and only one of the two high-order bit positions of A.) If the overflow indicator is already on, it is not changed. The overflow indicator can be reset with a load status instruction or store status instruction, or by testing the indicator with a branch or skip on condition instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	Hexadecimal Value	Description	Format
	SD			DISP	98XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q	Short Instruction
	SD		1	DISP	99XX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q	
	SD		2	DISP	9AXX	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q	
	SD		3	DISP	9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q	
	SD	L		ADDR	9C00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q	Long Instruction Indirect Addressing
	SD	L	1	ADDR	9D00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q	
	SD	L	2	ADDR	9E00XXXX	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q	
	SD	L	3	ADDR	9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q	
	SD	I		ADDR	9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q	Long Instruction Indirect Addressing
	SD	I	1	ADDR	9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q	
	SD	I	2	ADDR	9E80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q	
	SD	I	3	ADDR	9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q	

MULTIPLY (M)

FORMATS



DESCRIPTION

The contents of the core-storage location specified by the effective address (EA) of the instruction (multiplicand) are multiplied algebraically by the contents of the accumulator (multiplier). The 32-bit double-precision product replaces the contents of the accumulator (A) and its extension (Q), while core storage remains unchanged. The most significant bits of the double-precision product are in A.

The largest product that can be developed is +1,073,741,824. This occurs when the multiplier and multiplicand are both the largest negative number; -32,768.

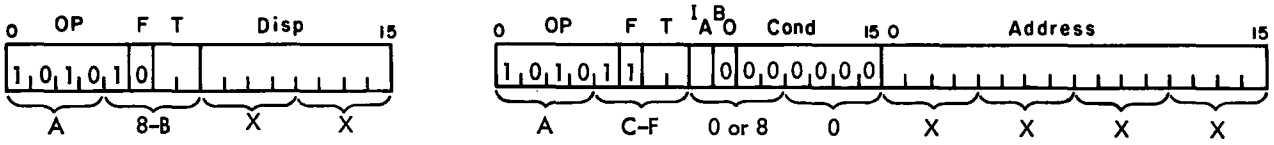
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding						Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	M			DISP		A0XX	Multiply contents of CSL at EA (I+DISP) by A	Short Instruction
	M		I	DISP		A1XX	Multiply contents of CSL at EA (XR1+DISP) by A	
	M		2	DISP		A2XX	Multiply contents of CSL at EA (XR2+DISP) by A	
	M		3	DISP		A3XX	Multiply contents of CSL at EA (XR3+DISP) by A	
	M	L		ADDR		A400XXXX	Multiply contents of CSL at EA (Addr) by A	Long Instruction Direct Addressing
	M	L	I	ADDR		A500XXXX	Multiply contents of CSL at EA (Addr+XR1) by A	
	M	L	2	ADDR		A600XXXX	Multiply contents of CSL at EA (Addr+XR2) by A	
	M	L	3	ADDR		A700XXXX	Multiply contents of CSL at EA (Addr+XR3) by A	
	M	I		ADDR		A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A	Long Instruction Indirect Addressing
	M	I	I	ADDR		A580XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A	
	M	I	2	ADDR		A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A	
	M	I	3	ADDR		A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A	

DIVIDE (D)

FORMATS



17172 B

DESCRIPTION

The contents of the accumulator and its extension form a 32-bit double-precision dividend which is divided algebraically by the contents of the core-storage location specified by the effective address (EA) of the instruction (divisor). The quotient and remainder replace the contents of the accumulator (A) and its extension (Q), respectively, while core storage remains unchanged. The "sign" of the remainder is the same as the "sign" of the dividend. Negative operands and/or negative quotients or remainders are in 2's complement form.

The largest dividend that can be divided correctly is +1,073,774,591 provided the divisor is the largest negative number (–32,768).

THE CARRY INDICATOR is not affected by this instruction.

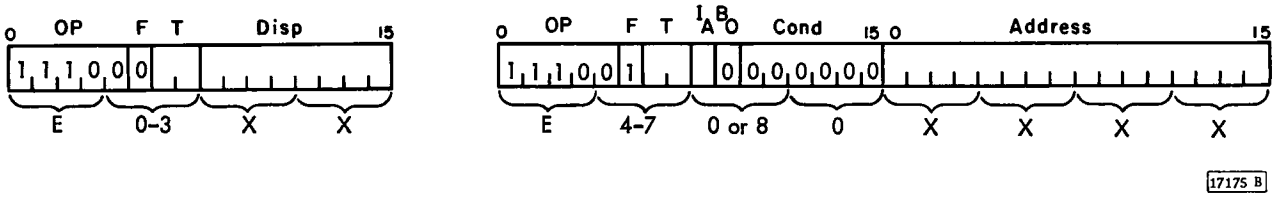
THE OVERFLOW INDICATOR is turned on when a division by zero is attempted or when a quotient overflow condition exists. A quotient overflow occurs if the magnitude of the quotient is too large to be represented in A; that is, greater than +32,767 or less than -32,768. A quotient overflow causes A and Q to be left in an undefined state. A division by zero leaves A and Q unchanged. In either case, the overflow indicator is unchanged if it is already on.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	D			DISP		A8XX	Divide A and Q by contents of CSL at EA (I+DISP)	Short Instruction
	D		1	DISP		A9XX	Divide A and Q by contents of CSL at EA (XR1+DISP)	
	D		2	DISP		AAXX	Divide A and Q by contents of CSL at EA (XR2+DISP)	
	D		3	DISP		ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)	
	D	L		ADDR		AC00XXXX	Divide A and Q by contents of CSL at EA (Addr)	Long Instruction Direct Addressing
	D	L	1	ADDR		AD00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR1)	
	D	L	2	ADDR		AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR2)	
	D	L	3	ADDR		AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)	
	D	I		ADDR		AC80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at Addr)	Long Instruction Indirect Addressing
	D	I	1	ADDR		AD80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")	
	D	I	2	ADDR		AE80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2")	
	D	I	3	ADDR		AF80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")	

LOGICAL AND (AND)

FORMATS



DESCRIPTION

The contents of the core-storage location specified by the effective address (EA) of the instruction are ANDed bit by bit with the contents of the accumulator (A). The result replaces the contents of A, while core storage remains unchanged.

The possible AND conditions are shown in the illustration.

AND

Storage	1	1	0	0
Accum	1	0	1	0
Result	1	0	0	0

17176

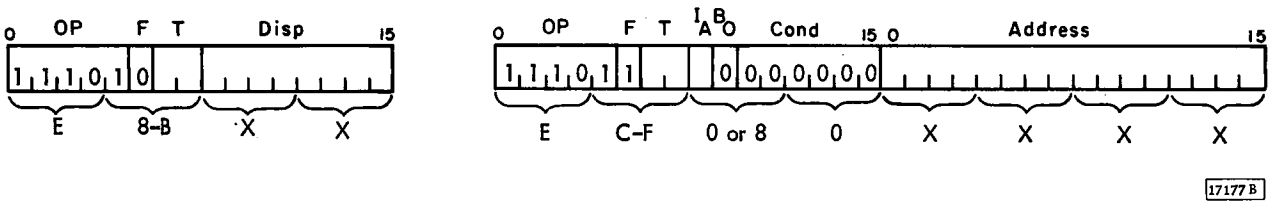
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	AND			DISP		E0XX	AND contents of CSL at EA (I+DISP) with A	Short Instruction
	AND		1	DISP		E1XX	AND contents of CSL at EA (XR1+DISP) with A	
	AND		2	DISP		E2XX	AND contents of CSL at EA (XR2+DISP) with A	
	AND		3	DISP		E3XX	AND contents of CSL at EA (XR3+DISP) with A	
	AND	L		ADDR		E400XXXX	AND contents of CSL at EA (Addr) with A	Long Instruction Direct Addressing
	AND	L	1	ADDR		E500XXXX	AND contents of CSL at EA (Addr+XR1) with A	
	AND	L	2	ADDR		E600XXXX	AND contents of CSL at EA (Addr+XR2) with A	
	AND	L	3	ADDR		E700XXXX	AND contents of CSL at EA (Addr+XR3) with A	
	AND	I		ADDR		E480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A	Long Instruction Indirect Addressing
	AND	I	1	ADDR		E580XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A	
	AND	I	2	ADDR		E680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A	
	AND	I	3	ADDR		E780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A	

LOGICAL OR (OR)

FORMATS



DESCRIPTION

The contents of the core-storage location specified by the effective address (EA) of the instruction are ORed bit by bit with the contents of the accumulator (A). The result replaces the contents of A, while core storage remains unchanged.

The possible OR conditions are shown in the illustration.

OR

Storage	1	1	0	0
Accum	1	0	1	0
Result	1	1	1	0

17178

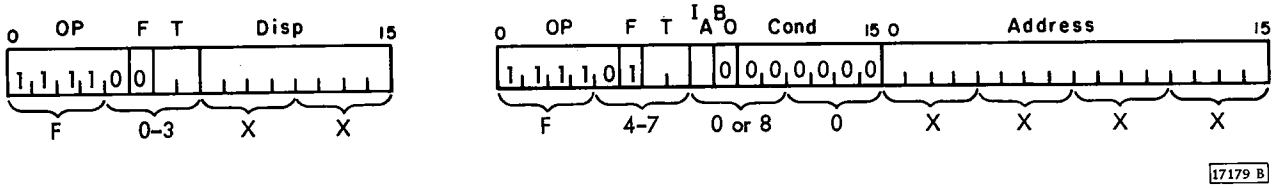
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	OR			DISP		E8XX	OR contents of CSL at EA (I+DISP) with A	Short Instruction
	OR		1	DISP		E9XX	OR contents of CSL at EA (XR1+DISP) with A	
	OR		2	DISP		EAXX	OR contents of CSL at EA (XR2+DISP) with A	
	OR		3	DISP		EBXX	OR contents of CSL at EA (XR3+DISP) with A	
	OR	L		ADDR		EC00XXXX	OR contents of CSL at EA (Addr) with A	Long Instruction Direct Addressing
	OR	L	1	ADDR		ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A	
	OR	L	2	ADDR		EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A	
	OR	L	3	ADDR		EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A	
	OR	I		ADDR		EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A	Long Instruction Indirect Addressing
	OR	I	1	ADDR		ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A	
	OR	I	2	ADDR		EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A	
	OR	I	3	ADDR		EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A	

LOGICAL EXCLUSIVE OR (EOR)

FORMATS



DESCRIPTION

The contents of the core-storage location specified by the effective address (EA) of the instruction are exclusive ORed bit by bit with the contents of the accumulator (A). The result replaces the contents of A, while core storage remains unchanged.

The possible exclusive OR conditions are shown in the illustration.

Exclusive OR

Storage	1	1	0	0
Accum	1	0	1	0
Result	0	1	1	0

17180

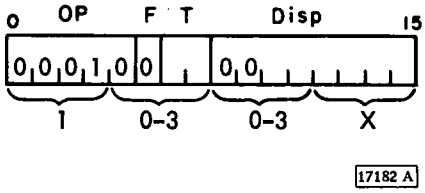
THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	Hexadecimal Value	Description	Format
	EOR			DISP	F0XX	EOR contents of CSL at EA (I+DISP) with A	Short Instruction
	EOR		1	DISP	F1XX	EOR contents of CSL at EA (XR1+DISP) with A	
	EOR		2	DISP	F2XX	EOR contents of CSL at EA (XR2+DISP) with A	
	EOR		3	DISP	F3XX	EOR contents of CSL at EA (XR3+DISP) with A	
	EOR	L		ADDR	F400XXXX	EOR contents of CSL at EA (Addr) with A	Long Instruction Direct Addressing
	EOR	L	1	ADDR	F500XXXX	EOR contents of CSL at EA (Addr+XR1)with A	
	EOR	L	2	ADDR	F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A	
	EOR	L	3	ADDR	F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A	
	EOR	I		ADDR	F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A	Long Instruction Indirect Addressing
	EOR	I	1	ADDR	F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A	
	EOR	I	2	ADDR	F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A	
	EOR	I	3	ADDR	F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A	

SHIFT LEFT LOGICAL A (SLA)

FORMAT



17182 A

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

DESCRIPTION

The bits in the accumulator (A) are shifted left the number of positions specified by the shift count. Vacated bit positions are set to 0. Bits leaving the high-order (bit 0) position of A are shifted into the carry indicator.

The source of the shift count is specified by the tag bits as shown above. The shift count is loaded into the shift control counter from the specified source and then decremented as each shift occurs. The source of the shift count remains unchanged. If a shift count of 0 is specified, this instruction performs as a no-op (no-operation).

Note that bit positions 8 and 9 of the instruction must both be 0.

THE CARRY INDICATOR is turned on for each 1 bit and off for each 0 bit shifted left from the high-order (bit 0) position of A.

THE OVERFLOW INDICATOR is not changed by this instruction.

EXAMPLES

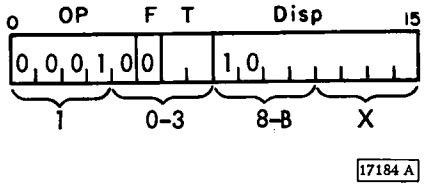
Assembler Language Coding				Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	See Note	Hexadecimal Value	Description	Format
	SLA			1	10*X	Contents of A shift left the number of shift counts in DISP	Short Instruction
	SLA		1		1100	Contents of A shift left the number of shift counts in XR1	
	SLA		2		1200	Contents of A shift left the number of shift counts in XR2	
	SLA		3		1300	Contents of A shift left the number of shift counts in XR3	

DISP (35–40)

1 The third from the high-order hex. digit can be 0, 1, 2, or 3, depending on the value of the shift count.

SHIFT LEFT A AND Q (SLT)

FORMAT



17184 A

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

DESCRIPTION

The bits in the accumulator (A) and its extension (Q) are shifted left, as a 32-bit double-precision, register, the number of positions specified by the shift count. The high-order (bit 0) position of Q is shifted into the low-order (bit 15) position of A. Vacated bit positions are set to 0. Bits leaving the high-order (bit 0) position of A are shifted into the carry indicator.

The source of the shift count is specified by the tag bits as shown above. The shift count is loaded into the shift control counter from the specified source and then decremented as each shift occurs. The source of the shift count remains unchanged. If a shift count of 0 is specified, the instruction performs as a no-op (no-operation).

Note that bit positions 8 and 9 of the instruction must be 1 and 0, respectively.

THE CARRY INDICATOR is turned on for each 1 bit and off for each 0 bit shifted from the high-order (bit 0) position of A.

THE OVERFLOW INDICATOR is not changed by this instruction.

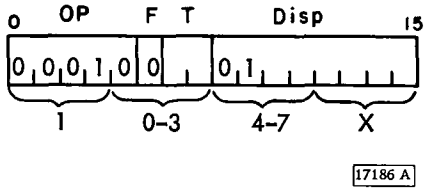
EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	SLT			DISP	1	10*X	Contents of A and Q shift left the number of shift count in DISP	Short Instruction
	SLT		1			1180	Contents of A and Q shift left the number of shift counts in XR1	
	SLT		2			1280	Contents of A and Q shift left the number of shift counts in XR2	
	SLT		3			1380	Contents of A and Q shift left the number of shift counts in XR3	

1 The third from the high-order hex. digit can be 8, 9, A, or B depending on the value of the shift count.

SHIFT LEFT AND COUNT A (SLCA)

FORMAT



Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

DESCRIPTION

If the tag bits in this instruction are both 0 (no index register specified), the instruction performs as a shift left A (SLA) instruction.

If the tag bits are not both 0 (an index register is specified), the bits in the accumulator (A) are shifted left until the shift is terminated by an attempt to shift a 1 bit from the high-order (bit 0) position of A (the 1 bit remains in the high-order position of A after the instruction is terminated) or by the shift count decreasing to 0. Vacated bit positions are set to 0.

The source of the shift count is the index register specified by the tag bits. The shift count is loaded into the shift control counter from the index register and then decreased as each shift occurs. When the shift is terminated, the residual shift count in the shift control counter is loaded back into bit positions 10 through 15 of the specified index register. Bit positions 8 and 9 of the index register are set to zero, while bit positions 0 through 7 of the index register remain unchanged. If the shift count initially specified is 0, or the high-order (bit 0) position of A is initially a 1 bit, this instruction performs as a no-op (no-operation).

Note that bit positions 8 and 9 of the instruction must be 0 and 1, respectively.

THE CARRY INDICATOR is set as in a shift left A (SLA) instruction if the tag bits are both 0. If the tag bits are not both 0, and the shift is terminated by the shift count decreasing to 0, the carry indicator will be off at the end of the operation. In this case, the value of the high-order (bit 0) position of A can be determined only by testing the "sign" of A. If the tag bits are not both 0 and the shift is terminated by an attempt to shift a 1 bit from the high-order (bit 0) position of A, the carry indicator will be on at the end of the operation. The one bit remains in the high-order (bit 0) position of A and the residual shift count, which will be non-0, is in the index register specified by the tag bits.

THE OVERFLOW INDICATOR is not changed by this instruction.

EXAMPLES

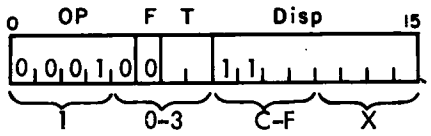
Assembler Language Coding						Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	SLCA			DISP	1	10*X	Contents of A shift left the number of shift counts in DISP	Short Instruction
	SLCA		1		2	1140	Contents of A shift left the number of shift counts in XR1	
	SLCA		2		2	1240	Contents of A shift left the number of shift counts in XR2	
	SLCA		3		2	1340	Contents of A shift left the number of shift counts in XR3	

1 The third from the high-order hex. digit can be 4, 5, 6, or 7, depending on the value of the shift count.

2 These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.

SHIFT LEFT AND COUNT A AND Q (SLC)

FORMAT



17187 A

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

DESCRIPTION

If the tag bits in this instruction are both 0 (no index register specified), the instruction performs as a shift left A and Q (SLT) instruction.

If the tag bits are not both 0 (an index register is specified), the instruction performs in the same manner as a shift left and count A (SLCA) instruction with non-0 tag bits except that bits in both the accumulator (A) and its extension (Q) are shifted as a 32-bit double-precision register. The high-order (bit 0) position of Q is shifted into the low-order (bit 15) position of A. Vacated positions are set to 0.

Note that bit positions 8 and 9 of the instruction must both be 1.

THE CARRY INDICATOR is set as in a shift left A and Q (SLT) instruction if the tag bits are both 0. If the tag bits are not both 0 and the shift is terminated by the shift count decreasing to 0, the carry indicator will be off at the end of the operation. In this case, the value of the high-order (bit 0) position of A can be determined only by testing the "sign" of A. If the tag bits are not both 0 and the shift is terminated by an attempt to shift a 1 bit from the high-order (bit 0) position of A, the carry indicator will be on at the end of the operation. The 1 bit remains in the high-order (bit 0) position of A and the residual shift count, which will be non-0, will be in the index register specified by the tag bits.

THE OVERFLOW INDICATOR is not changed by this instruction.

EXAMPLES

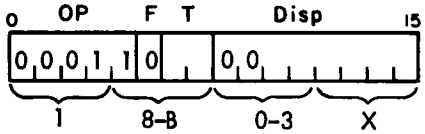
Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	SLC			DISP	1	10*X	Contents of A and Q shift left the number of shift counts in DISP	Short Instruction
	SLC		1		2	11C0	Contents of A and Q shift left the number of shift counts in XR1	
	SLC		2		2	12C0	Contents of A and Q shift left the number of shift counts in XR2	
	SLC		3		2	13C0	Contents of A and Q shift left the number of shift counts in XR3	

1 The third from the high-order hex. digit can be C, D, E or F, depending on the value of the shift count.

2 These instructions are terminated either when an attempt is made to shift a one bit from the high-order position of the accumulator (with a non-zero shift count remaining) or when the shift count has been decremented to zero.

SHIFT RIGHT LOGICAL A (SRA)

FORMAT



17188 A

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

DESCRIPTION

The bits in the accumulator (A) are shifted right the number of positions specified by the shift count. Vacated bit positions are set to 0. Bits leaving the low-order (bit 15) position of A are lost.

The source of the shift count is specified by the tag bits as shown above. The shift count is loaded into the shift control counter and then decremented as each shift occurs. The source of the shift count remains unchanged. If a shift count of 0 is specified, this instruction performs as a no-op (no-operation).

Note that bit positions 8 and 9 of the instruction must both be 0.

THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

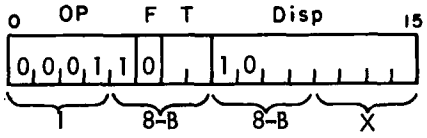
EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	SRA			DISP	1	18*X	Contents of A shift right the number of shift counts in DISP	Short Instruction
	SRA		1			1900	Contents of A shift right the number of shift counts in XR1	
	SRA		2			1A00	Contents of A shift right the number of shift counts in XR2	
	SRA		3			1B00	Contents of A shift right the number of shift counts in XR3	

1 The third from the high-order hex. digit can be 0, 1, 2, or 3, depending on the value of the shift count.

SHIFT RIGHT A AND Q (SRT)

FORMAT



17189 A

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

DESCRIPTION

The bits in the accumulator (A) and its extension (Q) are shifted right, as a 32-bit double-precision register, the number of positions specified by the shift count. The low-order (bit 15) position of A is shifted into the high-order (bit 0) position of Q. Vacated bit positions are filled with the value of the sign (bit position 0 of A). Bits leaving the low-order (bit 15) position of Q are lost.

The source of the shift count is specified by the tag bits as shown above. The shift count is loaded into the shift control counter and then decreased by 1 as each shift occurs. The source of this shift count remains unchanged. If a shift count of 0 is specified, this instruction performs as a no-op (no-operation).

Note that bit positions 8 and 9 of the instruction must be 1 and 0, respectively.

THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

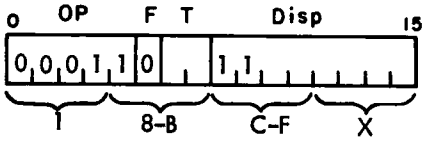
EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	SRT			DISP	1	18*X	Contents of A and Q shift right the number of shift counts in DISP	Short Instruction
	SRT		1			1980	Contents of A and Q shift right the number of shift counts in XR1	
	SRT		2			1A80	Contents of A and Q shift right the number of shift counts in XR2	
	SRT		3			1B80	Contents of A and Q shift right the number of shift counts in XR3	

1 The third from the high-order hex. digit can be 8, 9, A, or B, depending on the value of the shift count.

ROTATE RIGHT A AND Q (RTE)

FORMAT



17190 A

Tag	Shift Count Determined By:
00	Low-Order 6 Bits of Disp
01	Low-Order 6 Bits of XR1
10	Low-Order 6 Bits of XR2
11	Low-Order 6 Bits of XR3

17 181

DESCRIPTION

The bits in the accumulator (A) and its extension (Q) are rotated to the right, as a 32-bit double-precision register, the number of positions specified by the shift count. Bits leaving the low-order (bit 15) position of A are shifted into the high-order (bit 0) position of Q. Bits leaving the low-order (bit 15) position of Q are shifted into the high-order (bit 0) position of A, thus forming a continuous shift loop. No bits are lost in this operation.

The source of the shift count is specified by the tag bits as shown above. The shift count is loaded into the shift control counter and then decreased by 1 as each shift occurs. The source of the shift count remains unchanged. If a shift count of 0 is specified, this instruction performs as a no-op (no-operation).

Note that bit positions 8 and 9 of the instruction must both be on.

THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

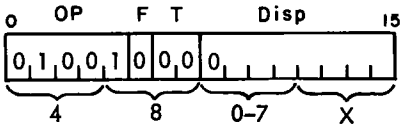
EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	RTE			DISP	1	18*X	Contents of A and Q rotate right the number of counts in DISP	Short Instruction
	RTE		1			19C0	Contents of A and Q rotate right the number of counts in XR1	
	RTE		2			1AC0	Contents of A and Q rotate right the number of counts in XR2	
	RTE		3			1BC0	Contents of A and Q rotate right the number of counts in XR3	

1 The third from the high-order hex. digit can be C, D, E, or F, depending on the value of the shift count.

BRANCH OR SKIP ON CONDITION (BSC OR BOSC) Skip Function

FORMAT



DESCRIPTION

The short format BSC or BOSC instruction provides a skip depending on conditions tested by the instruction. Six conditions, associated with the accumulator (A), can be tested using this short instruction. Conditions to be tested are specified by one bits in the associated bit positions of the displacement field as follows:

Bit Position	Condition Tested
15	Overflow indicator off
14	Carry indicator off
13	Accumulator even
12	Accumulator plus (greater than zero)
11	Accumulator minus (less than zero)
10	Accumulator Zero

If one or more of the specified conditions is true, the next core-storage word (one word) in the instruction stream is skipped and not executed. Therefore, this instruction must be followed by a one word (short) instruction. If none of the specified conditions is true, the skip does not occur and the next instruction in sequence is executed. If no conditions are specified in the instruction, a skip never occurs.

When bit position 9 of the instruction is 1, the instruction is called a BOSC instruction. A short format (skip function) BOSC performs the same skip functions as described in the preceding paragraphs, and also resets the highest priority interrupt level that is on if a skip occurs. This allows lower priority level interrupts to again be accepted by the P-C. (See "Interrupt Operating Characteristics.")

Some skip condition examples as compared to branch condition examples are shown in the table. The BSC or BOSC branch function is described on the next page.

Bit positions: ACC conditions:	Zero	Minus	Plus	Even	Skip (F = 0)	Branch (F = 1)
Test Conditions	1	1	1	0	Always	Never
	0	0	0	0	Never	Always
	0	0	1	0	Plus	Not plus
	1	1	0	0	Not plus	Plus
	0	1	0	0	Minus	Not minus
	1	0	1	0	Not Minus	Minus
	1	0	0	0	Zero	Not zero
	0	1	1	0	Not zero	Zero
	0	0	0	1	Even	Odd
	0	0	1	1	Even or Plus	Odd and minus
	0	1	0	1	Even or minus	Odd and plus

Notes: 1. ACC zero is not a plus condition.
2. Skip and branch columns specify action or ACC condition required for skip or branch.
3. Skip on odd condition, carry on, or overflow on are not possible.

THE CARRY INDICATOR is not reset by this instruction.

THE OVERFLOW INDICATOR is reset when tested by this instruction.

EXAMPLES

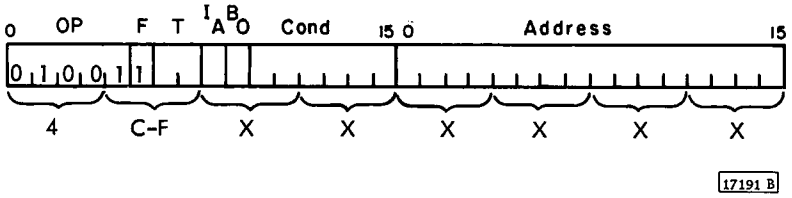
Assembler Language Coding						Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F	T	32	33 35 40	See Note	Hexadecimal Value	Description	Format
	BSC				C,O,N,D,	1	48*X	Skip the next one-word instruction if any condition is true	Short Instruction
	BOSC				C,O,N,D,	2	48*X	Skip the next one-word instruction if any condition is true	

1 The third from the high-order hex. digit can be 0, 1, 2, or 3, depending on which conditions are tested.

2 The third from high-order hex. digit can be 4, 5, 6, or 7, depending on which conditions are tested. This BOSC instruction resets the highest priority interrupt level on if a skip occurs.

BRANCH OR SKIP ON CONDITION (BSC OR BOSC) Branch Function

FORMAT



DESCRIPTION

This long format instruction performs in a manner similar to the short format (skip function) BSC or BOSC instruction in that the same six conditions associated with the accumulator (A) can be tested. Conditions to be tested are specified in the same manner as the short BSC or BOSC instruction described on the preceding page.

If one or more of the specified conditions are true, the next instruction in sequence is executed. If none of the specified conditions is true, a branch is made to the core-storage location specified by the effective address (EA) of the instruction. If no conditions are specified in this instruction, a branch to the EA always occurs. Note that this is reverse logic from the short format (skip function) BSC or BOSC instruction.

If bit position 9 of the instruction is 1, the instruction is called a branch out of interrupt (BOSC) instruction. A long format (branch function) BOSC performs the same branch functions as described in the preceding paragraphs, and also resets the highest priority interrupt level that is on if a branch occurs.

The long format (branch function) BSC or BOSC instruction can be used to return to a mainline program from a subroutine (bit position 9 should be 0) or interrupt routine (bit position 9 should be 1). This is accomplished by making the EA of the BSC or BOSC instruction identical to the EA of a previously executed BSI instruction.

Some branch condition examples as compared to skip condition examples are shown in the table on the preceding page.

THE CARRY INDICATOR is not reset when tested by this instruction.

THE OVERFLOW INDICATOR is reset when tested by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	BSC	L		ADDR,CND	1 3	4C*XXXXX	Branch to CSL at EA (Addr) on no condition true	Long Instruction Direct Addressing
	BSC	L	I	ADDR,CND	1 3	4D*XXXXX	Branch to CSL at EA (Addr+XR1) on no condition true	
	BSC	L	2	ADDR,CND	1 3	4E*XXXXX	Branch to CSL at EA (Addr+XR3) on no condition true	
	BSC	L	3	ADDR,CND	1 3	4F*XXXXX	Branch to CSL at EA (Addr+XR2) on no condition true	
	BSC	I		ADDR,CND	2 3	4C*XXXXX	Branch to CSL at EA (V in CSL at Addr) on no condition true	Long Instruction Indirect Addressing
	BSC	I	I	ADDR,CND	2 3	4D*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR1") on no condition true	
	BSC	I	2	ADDR,CND	2 3	4E*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR2") on no condition true	
	BSC	I	3	ADDR,CND	2 3	4F*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR3") on no condition true	

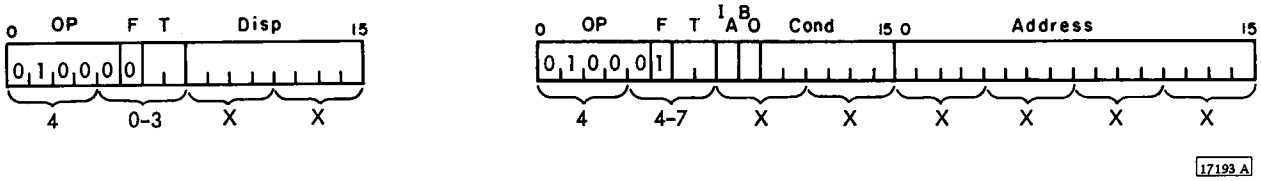
1 The third from high-order hex. digit can be 0, 1, 2, or 3, (BSC) or 4, 5, 6, or 7, (BOSC) depending on which conditions are tested.

2 The third from high-order hex. digit can be 8, 9, A, or B, (BSC) or C, D, E, or F, (BOSC) depending on which conditions are tested.

3 The highest priority interrupt level on is reset if instruction is BOSC and a branch occurs.

BRANCH AND STORE INSTRUCTION REGISTER (BSI)

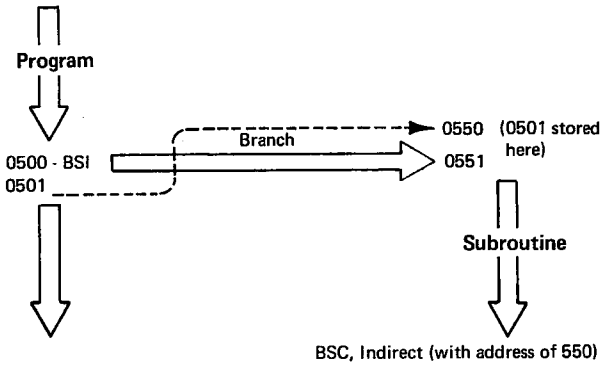
FORMATS



DESCRIPTION

This instruction stores the contents of the instruction (I) register in the core storage location specified by the effective address (EA) of the instruction and then causes a branch to core storage location EA + 1. Program execution proceeds from that location (EA + 1). The stored address is that of the next instruction in the normal sequence.

As shown in the illustration, for example, a BSI located at core-storage location 0500, with an EA of 0550, would store the address 0501 at location 0550 and branch to location 0551. A long format BSC with indirect addressing would be used to return to the mainline program.



When the BSI is a short format instruction (F bit is 0), the branch described in the preceding paragraph is unconditional.

When the BSI is a long format instruction (F bit is 1), the branch is conditional depending on the six test conditions associated with the accumulator. The test conditions and method of specifying the conditions to be tested are defined in the preceding BSC or BOSC instructions. If one or more of the specified conditions is true, the branch does not occur and the next instruction in sequence is executed. If none of the specified conditions are true, the branch occurs as previously described.

Internal, CE, and external level interrupts are not polled during execution of a BSI instruction. Therefore, no interrupt (other than trace) can occur immediately following a BSI instruction. (See "Interrupt" section.)

THE CARRY INDICATOR is not reset by a short or long format BSI instruction.

THE OVERFLOW INDICATOR is not reset by a short format BSI instruction, but is reset if tested with a long format BSI instruction.

EXAMPLES

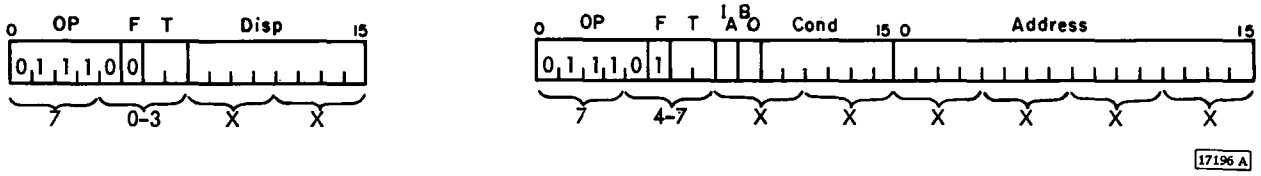
Assembler Language Coding						Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F (32)	T (33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	BSI			DISP		40XX	Store next sequential address in CSL at EA (I + DISP) and branch to EA + 1	Short Instruction
	BSI		1	DISP		41XX	Store next sequential address in CSL at EA (XR1+DISP) and branch to EA + 1	
	BSI		2	DISP		42XX	Store next sequential address in CSL at EA (XR2+DISP) and branch to EA + 1	
	BSI		3	DISP		43XX	Store next sequential address in CSL at EA (XR3+DISP) and branch to EA + 1	
	BSI	L		ADDR,,COND	1	44*XXXXX	If no condition is true, store next sequential address in CSL at EA (Addr) and branch to EA + 1	Long Instruction Direct Addressing
	BSI	L	1	ADDR,,COND	1	45*XXXXX	If no condition is true, store next sequential address in CSL at EA (Addr+XR1) and branch to EA + 1	
	BSI	L	2	ADDR,,COND	1	46*XXXXX	If no condition is true, store next sequential address in CSL at EA (Addr+XR2) and branch to EA + 1	
	BSI	L	3	ADDR,,COND	1	47*XXXXX	If no condition is true. store next sequential address in CSL at EA (Addr+XR3) and branch to EA + 1	
	BSI	I		ADDR,,COND	2	44*XXXXX	If no condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and branch to EA + 1	Long Instruction Indirect Addressing
	BSI	I	1	ADDR,,COND	2	45*XXXXX	If no condition is true. store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and branch to EA + 1	
	BSI	I	2	ADDR,,COND	2	46*XXXXX	If no condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and branch to EA + 1	
	BSI	I	3	ADDR,,COND	2	47*XXXXX	If no condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and branch to EA + 1	

[1] The third from high-order hex. digit can be 0, 1. 2, or 3, depending on which conditions are tested.

[2] The third from high-order hex. digit can be 8, 9. A, or B, depending on which conditions are tested.

MODIFY INDEX AND SKIP (MDX)

FORMATS



DESCRIPTION

This instruction provides a method of modifying the contents of the instruction (I) register, an index register (XR), or a core storage location. A skip function is also provided when modifying an XR or a core storage location. If the modified XR or core storage location changes sign during the operation or is zero after the operation is complete, the next core storage word in the instruction stream is skipped. Programmers should be aware that core storage address above 32,767 (/7FFF) are considered to have negative signs. Therefore, an unwanted skip may occur if care is not exercised when programming across this negative boundary with an MDX instruction.

I-REGISTER MODIFICATION is accomplished using a short format (F bit is 0) MDX instruction with the tag bits both 0 (no index register specified). The displacement portion of the instruction (bits 8 through 15) is expanded to a 16-bit value by propagating the value of bit 8 (sign bit) to the left 8 positions. This expanded displacement is then added to the contents of the I-register and the result is placed in the I-register thus, causing a branch. No skip can occur with this instruction.

A short MDX instruction of /70FF can be used as a dynamic wait instruction. This instruction modifies the I-register by minus 1. Therefore, once the instruction is encountered, it is repeated continuously, allowing interrupts to be serviced. Unless an interrupt subroutine alters the stored return address, the program returns to the MDX instruction at the end of the interrupt subroutine.

INDEX REGISTER MODIFICATION is accomplished using either a short format (F bit is 0) or long format (F bit is 1) MDX instruction. The tag bits must specify the XR to be modified.

A short format MDX instruction causes the displacement portion of the instruction (bits 8 through 15) to be expanded to a 16-bit value by propagating the value of bit 8 (sign bit) to the left 8 positions. This expanded displacement is then added to the XR specified by the tag bits.

A long format MDX instruction without indirect addressing (IA bit is 0) causes the contents of the address word of the instruction to be added to the XR specified by the tag bits. A long format MDX instruction with indirect addressing (IA bit is 1) causes the contents of the core storage location specified by the address word of the instruction to be added to the XR specified by the tag bits.

In any case, when modifying an XR, the next core-storage word in the instruction stream is skipped if the XR changes sign during the operation or is 0 after the operation is complete. Therefore, this instruction should be followed by a short format instruction.

CORE STORAGE MODIFICATION is accomplished using a long format (F bit is one) MDX instruction. The tag bits must both be 0 to modify core storage. The displacement portion of the instruction (bits 8 through 15) is expanded to a 16-bit value by propagating the value of bit 8 (sign bit) to the left 8 positions. This expanded displacement is then added to the contents of the core storage location specified by the address word of the instruction. If the core storage word changes sign during the operation or is zero after the operation is complete, the next core storage word in the instruction stream is skipped. Therefore, this instruction should be followed by a short format instruction.

THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

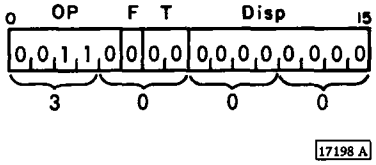
Assembler Language Coding						Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	MDX			DISP		70XX	Add expanded DISP to I (no skip can occur)	Short Instruction
	MDX		1	DISP		71XX	Add expanded DISP to XR1	
	MDX		2	DISP		72XX	Add expanded DISP to XR2	
	MDX		3	DISP		73XX	Add expanded DISP to XR3	
	MDX	L		ADDR,DISP	1	74*XXXXX	Add expanded positive or negative DISP to CSL at Addr (add to core storage)	Long Instruction Direct Addressing
	MDX	L	1	ADDR		7500XXXX	Add Addr to XR1	
	MDX	L	2	ADDR		7600XXXX	Add Addr to XR2	
	MDX	L	3	ADDR		7700XXXX	Add Addr to XR3	
	MDX	I		ADDR,DISP	2	74*XXXXX	This instruction should not be used to modify storage. Use MDX L	Long Instruction Indirect Addressing
	MDX	I	1	ADDR		7580XXXX	Add V in CSL at Addr to XR1	
	MDX	I	2	ADDR		7680XXXX	Add V in CSL at Addr to XR2	
	MDX	I	3	ADDR		7780XXXX	Add V in CSL at Addr to XR3	

1 The third from high-order hex. digit can be 0 through 7.

2 The third from high-order hex. digit can be 8 through F.

WAIT (WAIT)

FORMAT



DESCRIPTION

This short format instruction places the P-C in a wait condition. Data channel and/or interval timer operations continue during a wait condition. The P-C can be restarted by pressing START on the console or by detection of an interrupt. Following completion of an interrupt subroutine; the instruction immediately following the wait instruction is executed provided the branch out of interrupt (BOSC) instruction is the normal indirect subroutine linkage.

THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

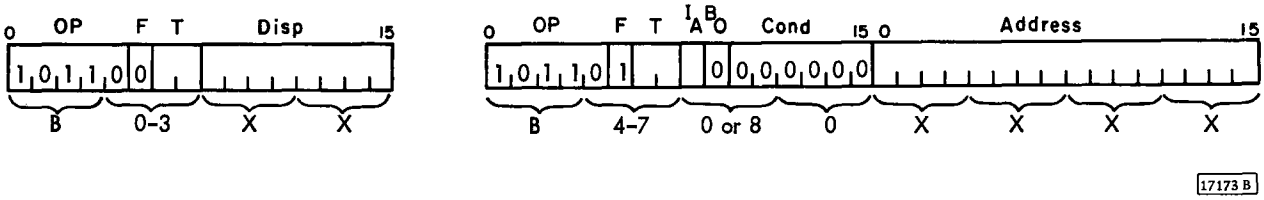
EXAMPLE

Assembler Language Coding					Equivalent Machine Language Instruction			
Label 21–25	Operation 27–30	F 32	T 33	35–40	See Note	Hexadecimal Value	Description	Format
	WAIT			(NOTE)		30XX	Wait until manual start or an interrupt occurs	Short

Note: The value placed in the operand field is optional and can be used to identify different waits.

COMPARE (CMP)

FORMATS



DESCRIPTION

The contents of the accumulator (A) are compared algebraically against the contents of the core-storage location specified by the effective address (EA) of the instruction. The contents of A and core storage remain unchanged. The instruction (I) register, which contains the next sequential instruction address, is modified according to the results of the comparison as follows:

If A is more positive than contents of EA, then I=I and no skip occurs.

If A is less positive than contents of EA, then I=I+1 and one core-storage word is skipped.

If A is equal to contents of EA, then I=I+2, and two core storage words are skipped.

THE CARRY INDICATOR may be altered by this instruction, but has no significance.

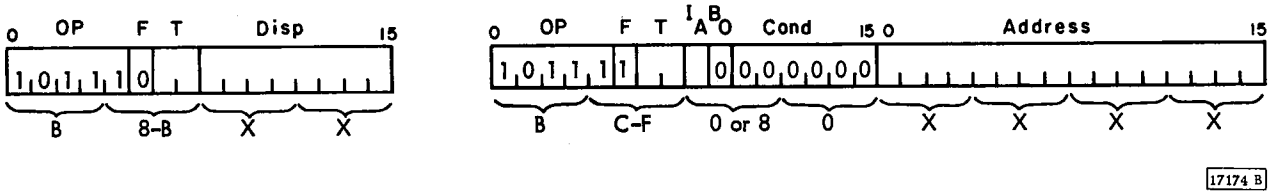
THE OVERFLOW INDICATOR is not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction			
Label (21–25)	Operation (27–30)	F	T (32–33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	CMP			DISP		B0XX	Compare A with contents of CSL at EA (I + DISP)	Short Instruction
	CMP		1	DISP		B1XX	Compare A with contents of CSL at EA (XR1+DISP)	
	CMP		2	DISP		B2XX	Compare A with contents of CSL at EA (XR2+DISP)	
	CMP		3	DISP		B3XX	Compare A with contents of CSL at EA (XR3+DISP)	
	CMP	L		ADDR		B400XXXX	Compare A with contents of CSL at EA (Addr)	Long Instruction Direct Addressing
	CMP	L	1	ADDR		B500XXXX	Compare A with contents of CSL at EA (Addr+XR1)	
	CMP	L	2	ADDR		B600XXXX	Compare A with contents of CSL at EA (Addr+XR2)	
	CMP	L	3	ADDR		B700XXXX	Compare A with contents of CSL at EA (Addr+XR3)	
	CMP	I		ADDR		B480XXXX	Compare A with contents of CSL at EA (V in CSL at Addr)	Long Instruction Indirect Addressing
	CMP	I	1	ADDR		B580XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")	
	CMP	I	2	ADDR		B680XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR2")	
	CMP	I	3	ADDR		B780XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")	

DOUBLE COMPARE (DCM)

FORMATS



17174 B

DESCRIPTION

The contents of the accumulator (A) and its extension (Q) form a 32-bit double-precision word which is compared algebraically against the contents of the core storage location specified by the effective address (EA) of the instruction and the next higher core-storage location (EA + 1). The contents of A, Q, EA, and EA + 1 remain unchanged. The instruction (I) register, which contains the next sequential instruction address, is modified according to the results of the comparison as follows:

If A and Q is more positive than the contents of EA and EA + 1, then I=I and no skip occurs.

If A and Q is less positive than the contents of EA and EA + 1, then I=I+1 and one core-storage word is skipped.

If A and Q is equal to the contents of EA and EA + 1, then I=I+2 and two core storage words are skipped.

The EA must be even for correct operation. If the EA is odd, A and Q are both compared against the contents of EA.

THE CARRY INDICATOR may be altered by this instruction, but has no significance.

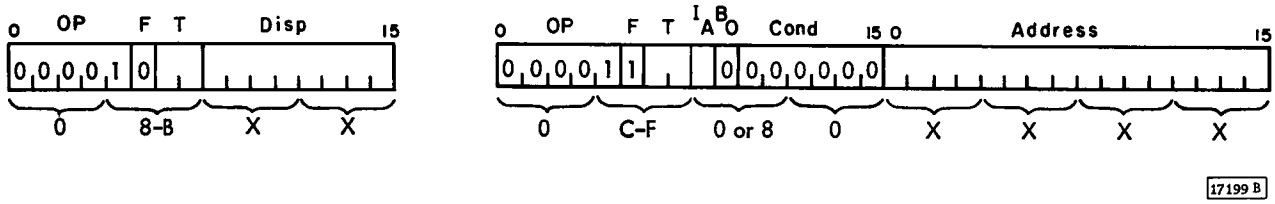
THE OVERFLOW INDICATOR is not changed by this instruction.

EXAMPLES

Assembler Language Coding					Equivalent Machine Language Instruction		
Label (21–25)	Operation (27–30)	F	T (32–33)	(35–40)	See Note	Hexadecimal Value	Description	Format
	DCM			DISP		B8XX	Compare A and Q with contents of CSL at EA (I + DISP) and EA + 1	Short Instruction
	DCM		I	DISP		B9XX	Compare A and Q with contents of CSL at EA (XR1+DISP) and EA + 1	
	DCM		2	DISP		BAXX	Compare A and Q with contents of CSL at EA (XR2+DISP) and EA + 1	
	DCM		3	DISP		BBXX	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA + 1	
	DCM	L		ADDR		BC00XXX	Compare A and Q with contents of CSL at EA (Addr) and EA + 1	Long Instruction Direct Addressing
	DCM	L	I	ADDR		BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA + 1	
	DCM	L	2	ADDR		BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA + 1	
	DCM	L	3	ADDR		BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA + 1	
	DCM	I		ADDR		BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA + 1	Long Instruction Indirect Addressing
	DCM	I	I	ADDR		BD80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR1") and EA + 1	
	DCM	I	2	ADDR		BE80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR2") and EA + 1	
	DCM	I	3	ADDR		BF80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR3") and EA + 1	

EXECUTE I/O (XIO)

FORMATS



DESCRIPTION

The XIO instruction is used for all input/output operations. The effective address (EA) of the instruction specifies the core-storage location of an input/output control command (IOCC). The IOCC specifies the device to be selected, the function to be completed on that device, and if necessary, the core storage location associated with information sent to or received from the selected device. IOCC's are described in detail in the "Input/Output Control" section of this manual. IOCC's for each specific device are included within the section for that device.

The EA of the XIO instruction must be an even address. Thus, IOCC's must also be located on even address boundaries.

No interrupts are polled during execution of an XIO instruction. Therefore, no interrupt can occur immediately following an XIO instruction. (See "Interrupt" section.)

THE CARRY AND OVERFLOW INDICATORS are not changed by this instruction.

EXAMPLES

Assembler Language Coding						Equivalent Machine Language Instruction			
Label 21 25	Operation 27 30	F 32	T 33	35 40	See Note	Hexadecimal Value	Description	Format
	XIO			DISP		08XX	Execute IOCC in CSL at EA (I + DISP) and EA + 1	Short Instruction
	XIO		1	DISP		09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA + 1	
	XIO		2	DISP		0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA + 1	
	XIO		3	DISP		0BXX	Execute IOCC in CSL at (XR3+DISP) and EA + 1	
	XIO	L		ADDR		0C00XXXX	Execute IOCC in CSL at EA (Addr) and EA + 1	Long Instruction Direct Addressing
	XIO	L	1	ADDR		0D00XXXX	Execute IOCC in CSL at EA (Addr + XR1) and EA + 1	
	XIO	L	2	ADDR		0E00XXXX	Execute IOCC in CSL at EA (Addr+XR2) and EA + 1	
	XIO	L	3	ADDR		0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA + 1	
	XIO	I		ADDR		0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA + 1	Long Instruction Indirect Addressing
	XIO	I	1	ADDR		0D80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA + 1	
	XIO	I	2	ADDR		0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA + 1	
	XIO	I	3	ADDR		0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA + 1	

AVERAGE INSTRUCTION EXECUTION TIMES

The average time required to perform a given instruction is shown in Figure 8.

DATA ADDITION

The arithmetic section of the P-C performs additions in successive machine cycles that are 1/4 μs (2 or 2.25 μs core storage) or 1/2 μs (4 μs core storage) in duration. The number of machine cycles required to complete the addition depends on the numbers being added and the resulting carries. As shown in Figure 9, the augend (A-register) and addend (D-register) are exclusive ORed and ANDed each machine cycle. The results of the exclusive OR function are placed in the A-register. The results of the AND function are ignored except for any carries that may occur. The carries are shifted one position to the left and placed in the D-register. (These bits represent carries that would result from a normal binary add operation.) Each time a carry occurs, another machine cycle is initiated in which the A- and D-registers are exclusive ORed and ANDed again. This process continues until there are no further carries, at which time the correct sum exists in the A-register.

The length of each carry chain depends on the numbers involved and varies from 0 to 15. In Figure 9, a carry chain of four (bit positions 2 through 5) caused five machine cycles. The first four of these cycles were included in the core storage cycle that read the addend from core storage. Only carry chain lengths of four and greater cause extra 1/4 or 1/2 μs machine cycles.

Total Execution Time

Two core storage cycles are required in the execution of an add instruction: one for instruction readout and effective address computation, and one for data readout and data addition. Figure 10 is a sequence chart for the "average" add operation in which the F-bit is 0, the tag bits are not both 0, and the carry chain length does not exceed four. The sequence chart is for a 2 μs core storage system.

The times in the table below pertain to the 2 μs core storage.

- Add 2 μs to execution times when indirect addressing is specified.
- Add 12.5% for 2.25 μs core storage or 100% for 4 μs core storage.

Instruction	F = 0		F = 1	
	T=0	T≠0	T=0	T≠0
LD	4-1/4	4-1/4	6	6-1/4
STO	4-1/4	4-1/4	6	6-1/4
LDD	6-1/4	6-1/4	8	8-1/4
STD	6-1/4	6-1/4	8	8-1/4
(1) A	4-1/2	4-1/2	6-1/4	6-1/2
(1) S	4-1/2	4-1/2	6-1/4	6-1/2
(1) AD	6-3/4	6-3/4	8-1/2	8-3/4
(1) SD	6-3/4	6-3/4	8-1/2	8-3/4
(1) M	15-1/4	15-1/4	17	17-1/4
(1) D	42-3/4	42-3/4	44	44-1/2
AND	4-1/4	4-1/4	6	6-1/4
OR	4-1/4	4-1/4	6	6-1/4
EOR	4-1/4	4-1/4	6	6-1/4
(2) BSI	2 to 4-1/4	2 to 4-1/4	2 to 6	2 to 6-1/4
(2) BSC	2	2	2 to 4	2 to 4-1/4
(3) SLA	2 + N/4	2 + N/4	-	-
(3) SLT	2 + N/4	2 + N/4	-	-
(4) SLCA	2 + N/4	2-1/2 + N/4	-	-
(4) SLC	2 + N/4	2-1/2 + N/4	-	-
(3) SRA	2 + N/4	2 + N/4	-	-
SRT	2 + N/4	2 + N/4	-	-
(5) RTE	2 + N/4	2 + N/4	-	-
WAIT	2	2	2	2
(6) XIO	6-1/4 to 8-1/4	6-1/4 to 8-1/4	8 to 10	8-1/4 to 10-1/4
LDX	2-1/4	2-1/4	4-1/4	4-1/4
STX	4-1/4	4-1/4	6	6
MDX	2-1/2	2-1/2	10-1/4	4-3/4
LDS	2	2	-	-
STS	4-1/4	4-1/4	6	6-1/4
(1) CMP	4-1/2	4-1/2	6-1/4	6-1/2
(1) DCM	6-3/4	6-3/4	8-1/2	8-3/4

(1) Execution times include an average add time of 2-1/4 μs.

(2) If a skip or branch is not executed, the instruction performs as a NOP with an execution time of 2.0 μs. If the skip or branch is executed, the second execution time is applicable.

(3) N = P-4, where P is the number of positions shifted, and N must be positive or zero.

(4) If T ≠ 0 and more than four (4) shifts occur, then 1/2 μs is added to the execution time as shown to restore the specified index register from the shift counter.

(5) A shift of 1, 2, 3, or 4 positions requires 2 μs, with 1/4 μs added for each additional shift position up to 15. Therefore, a shift of 5 positions takes 2.25 μs, a shift of 6 positions takes 2.5 μs, etc., up to 15 positions which takes 4.75 μs.

A shift of 16, 17, 18, or 19 positions requires 2.25 μs, with 1/4 μs added for each additional shift position up to 31. Therefore, a shift of 21 positions takes 2.5 μs, a shift of 22 positions takes 2.75 μs, etc., up to 31 positions which takes 5 μs.

(6) The longer times apply to read and write functions, the shorter times to all other functions.

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Figure 8. Instruction Execution Times, Average

Machine Cycles	AUGEND (A-reg) and ADDEND (D-reg) Contents	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	A_0	0	1	1	0	1	1	1	0	0	0	1	1	1	0	1	0
	D_0	1	1	1	1	0	0	1	1	0	0	0	1	1	1	0	1
*First	A_1	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1
	D_1	1	1	0	0	0	1	0	0	0	0	1	1	0	0	0	0
*Second	A_2	0	1	0	1	1	0	0	1	0	0	0	1	0	1	1	1
	D_2	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
*Third	A_3	0	1	0	1	0	0	0	1	0	1	0	1	0	1	1	1
	D_3	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
*Fourth	A_4	0	1	0	0	0	0	0	1	0	1	0	1	0	1	1	1
	D_4	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
**Fifth	A_5	0	1	1	0	0	0	0	1	0	1	0	1	0	1	1	1
	D_5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

* Occurs during the 2, 2.25, or 4 μs core storage cycle required to read the addend from core storage.

** Extra 1/4 or 1/2 μs machine cycle.

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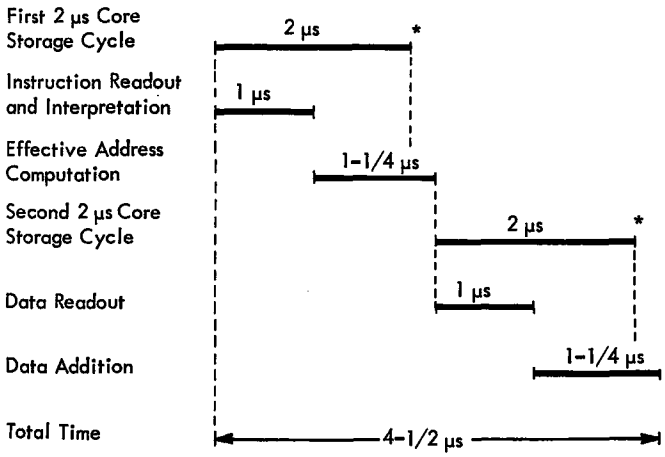
Figure 9. Data Addition Example



*Cycle steals can occur here without stopping effective address computation or data addition.

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Figure 10. Add Instruction Sequence Chart

Carry Chain Length	Probability (%)	Cumulative (%)	Time (μs)
0	1.3363	1.3363	2.00
1	9.8892	11.2255	2.00
2	27.0115	38.2370	2.00
3	27.7178	65.9548	2.00
4	17.3702	83.3250	2.25
5	8.9237	92.2487	2.50
6	4.2404	96.4891	2.75
7	1.9485	98.4376	3.00
8	0.8789	99.3165	3.25
9	0.3906	99.7071	3.50
10	0.1709	99.8780	3.75
11	0.0732	99.9512	4.00
12	0.0305	99.9817	4.25
13	0.0122	99.9939	4.50
14	0.0046	99.9985	4.75
15	0.0015	100.0000	5.00

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Figure 11. Mathematical Analysis of Addition of all Possible Number Pairs

Time Probabilities for Data Addition

Figure 11 shows a mathematical analysis of all possible number pairs that can be added with the A- and D- registers.

THE CARRY CHAIN LENGTH column lists all possible carry chain lengths up to the maximum of 15.

THE PROBABILITY column contains percentage figures which are related to the carry chain length. For example, a carry chain length of four occurs during 17.37% of all add operations.

THE CUMULATIVE column is merely a progressive summation of the probability percentages. For example, 83.32% of all add operations involve carry chain lengths of four or less. Incidentally, this relationship is the basis for the average execution time given in this section for add instructions.

THE TIME column shows the time required for data readout and data addition (see Figure 10) with a 2 μs core storage system. The average data readout and data addition time for adding all possible numbers at random is 2.16 μs.

Input/Output Control

Input/output (I/O) operations transfer information between core storage and I/O devices. Input/output devices include card read punches, magnetic tape units, disk storage devices, printer-keyboard devices, printers, plotters, communications devices, and process control equipment. The 1800 also has features that are internal to the processor-controller (P-C) but are considered I/O devices by the program. These features include the P-C console, the interval timers, the operations monitor, and the interrupt mask register.

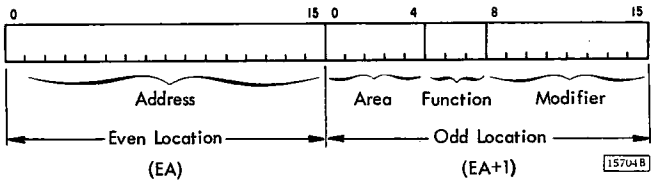
I/O device operations are controlled by adapters. Each I/O device has its own adapter. This adapter may be separate from the I/O device or included as an integral part of the I/O device. For example, the 1443 Printer has a separate adapter; the 1810 Disk Storage contains its own adapter. In any case, the adapter provides the logical and buffering capabilities needed to operate its specific I/O device. From a programming point of view, most adapter functions merge with I/O device functions.

With the exception of internal I/O devices, each I/O device adapter has standard signal connections to the P-C and responds to a standard set of signals from the P-C. This "I/O unit to P-C" connection is called the I/O interface. It enables the P-C to control all I/O operations with a common set of instructions.

INPUT/OUTPUT CONTROL COMMANDS

The 1800 system uses the execute I/O (XIO) instruction to control all I/O operations. The effective address (EA) of the XIO specifies the core storage location of a two-word input/output control command (IOCC). The IOCC specifies the device to be selected, the function to be performed with the selected device, and if necessary, the core storage location associated with information sent to or received from the selected device.

Execution of the XIO instruction causes the IOCC to be read from core storage and the function specified is performed on the selected device. The basic format of an IOCC is shown in the following illustration.



Area

The five-bit area field specifies the device to be used in the I/O operation. In some cases, the area code may represent a group of devices, such as magnetic tape units or printer-keyboards. In these cases, the modifier field specifies the particular device within the group.

Area codes are preassigned to each type of I/O device that can be ordered for the 1800 system. A list of these devices and their respective area codes is shown in Figure 12.

Function

The three-bit function field specifies the primary function or operation to be performed. Eight primary I/O function codes are provided; these are explained next.

000 -- CUSTOMER ENGINEERING (CE) MODE: This function code is used to remove some I/O devices from on-line status and place them in CE mode, or vice versa.

001 -- WRITE: This function code causes a single word to be transferred from core storage to an I/O device. The core storage location of the single word is specified by the IOCC address word. The current contents of the accumulator are destroyed by execution of a write function. It is the programmer's responsibility to save the accumulator contents, if necessary.

010 -- READ: This function code causes a single word to be transferred from an I/O device to core storage. The core storage location is specified by the IOCC address word. The current contents of the accumulator are destroyed by execution of a read function. It is the

I/O Device	Area Code	
	Decimal	Binary
Console Operations	0	(00000)
1816/1053 Printers (first 4)	1	(00001)
1442 Card Read Punch (first)	2	(00010)
1054/1055 Paper Tape Units	3	(00011)
1810 Disk Storage (first drive)	4	(00100)
1627 Plotter	5	(00101)
1443 Printer	6	(00110)
2790 Adapter (first)	7	(00111)
1810 Disk Storage (second drive)	8	(01000)
1810 Disk Storage (third drive)	9	(01001)
Analog Input	10	(01010)
Digital Input (Digital and Pulse Count)	11	(01011)
Digital and Analog Output (DO, ECO, RO, AO)	12	(01100)
System/360 Adapter	13	(01101)
2401/2402 Magnetic Tape Units	14	(01110)
1816/1053 Printers (second 4)	15	(01111)
Analog Input Expander	16	(10000)
1442 Card Read Punch (second)	17	(10001)
Selector Channel	18	(10010)
2790 Adapter (second)	19	(10011)
Comm Adapter (fourth)	20	(10100)
Comm Adapter (first)	21	(10101)
Comm Adapter (second)	22	(10110)
Comm Adapter (third)	23	(10111)

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Figure 12. Area Codes

programmer's responsibility to save the accumulator contents, if necessary.

011 -- SENSE INTERRUPT: This function code causes the interrupt level status word (ILSW) of the highest priority interrupt level requesting service at the time the IOCC is issued to be loaded into the accumulator. It is the programmer's responsibility to save the current contents of the accumulator, if necessary. Sense interrupt function is common to all I/O devices; therefore, no area code need be specified.

100 -- CONTROL: This function code causes the selected device to interpret the modifier and/or address field as a specific control action.

101 -- INITIALIZE WRITE: This function code initiates a write operation with a device that will subsequently transfer data from core storage via a data channel. The IOCC address word specifies the starting core storage address of a table that contains data words and control information.

110 -- INITIALIZE READ: This function code initiates a read operation with a device that will subsequently transfer data to core storage via a data channel. The IOCC address word specifies the starting core storage address of a table that contains control information and reserved locations for the data words read.

111 -- SENSE DEVICE: This function code causes the device status word (DSW) of the selected device to be loaded into the accumulator. It is the programmer's responsibility to save the current contents of the accumulator, if necessary. If IOCC modifier bit 15 is on, all program resettable indicators in the DSW sensed are reset. Devices with more than one DSW use the modifier bits to select the desired DSW.

Not all I/O devices respond to all eight function codes. The function codes to which a particular device responds are described in the section for that device. Appendix B contains a consolidated listing of area, function, and modifier combinations for all devices.

Modifier

The eight-bit modifier field provides further definition, if necessary, for either the function code or area code. For example, if the area code specifies a 1443 Printer, and if the function is initialize write, then a particular modifier code specifies the suppress-space operation. In this case, the modifier field extends the function.

However, if the area code specifies a group of I/O devices (such as 1053 Printers), and if the function is write, then the specific printer within the group is indicated by the modifier field. In this case, the modifier field extends the area code.

Address

The 16-bit address word has various uses, as determined by the IOCC function code. For example:

1. With a function of initialize write or initialize read, the address word specifies the starting address of a table in core storage.
2. With a function of control, the address word may further define the function code or may be ignored, depending on the particular device.

3. With a function of write or read, the address word specifies the core storage address of the data word.
4. With a function of sense interrupt, sense device, or CE mode, the address word is ignored.

DIRECT PROGRAM CONTROL

Direct program control (DPC) is one of two basic methods used to control data transfer between core storage and I/O devices, the second method being data channel control. Under direct program control, individual characters or data words are transferred at a rate controlled by the program and the maximum speed of the I/O device. Each character or data word is transferred to or from core storage by means of a separate XIO instruction. Data transfer is continued on a character-by-character or word-by-word basis by the program in response to interrupt requests from the I/O devices. The program performs the following steps for each interrupt:

1. Branches to an I/O routine, where an XIO sense DSW is executed to identify the interrupting condition and reset it.
2. Issues an XIO to transfer the next data word if desired.
3. Turns off the interrupt request indicator.
4. Branches back to the mainline program.

Devices operating under direct program control are relatively low-speed devices and include:

1053 Printer.
1054 Paper Tape Reader.
1055 Paper Tape Punch.
1627 Plotter.
1816 Printer-Keyboard.

Some devices operate under direct program control or data channel control, depending on the system configuration. These devices include:

Analog input.
Analog output.
Digital input.
Digital output.

Direct Program Control Operation

Figure 13 illustrates direct program control operation. The numbered steps that follow correlate with the circled numbers in Figure 13.

1. An XIO instruction is read from core storage for execution.
2. The effective address (EA) of the XIO is developed in the A-register and transferred to the storage address register (SAR). The EA is the address of the IOCC.
3. SAR bit position 15 is forced on to select location EA+1, which contains the IOCC area code, function code, and modifiers.
4. Area code, function code, and modifiers are transferred to the device specified by the area code via the out bus.
5. SAR bit position 15 is turned off to select location EA, which contains the IOCC address word.
6. The IOCC address word is transferred to the B-register. If the function is control, the address word is sent to the device via the out bus. If the function is read or write, the address word is sent to the SAR.
7. If the function is read or write, SAR addresses the core storage location to or from which data is transferred.

Immediately following the one-word transfer to or from core storage, the XIO is terminated and the next sequential instruction is executed. Normally, several data words must be transferred to complete message transfer. This is accomplished by recognition of a device interrupt each time the device is ready to send or receive a data word. P-C recognition of the interrupt causes a branch to a program subroutine associated with the device interrupt. The interrupt subroutine includes an XIO sense DSW with reset bit on to reset the interrupting condition. It also includes an XIO to read or write the next data word.

The interrupt subroutine must also modify the address portion of the IOCC for the next data word, perform a table look-up for translation of the device character if required, and maintain a program word count to indicate the end of message if necessary.

The exit from the interrupt subroutine must be accomplished with a branch-out-of-interrupt (BOSC) instruction. This operation restores the interrupt circuitry so that future interrupt requests at the same or lower priority levels can be acknowledged.

Device Busy

It is possible for the program to issue an XIO to a device that is busy responding to a previous XIO. Each device that could be placed in this situation provides a busy indicator in its device status word (DSW). This indicator signals that the device has not finished the previous command. If busy is ignored, erroneous operation of the I/O device will occur and undetected errors may result.

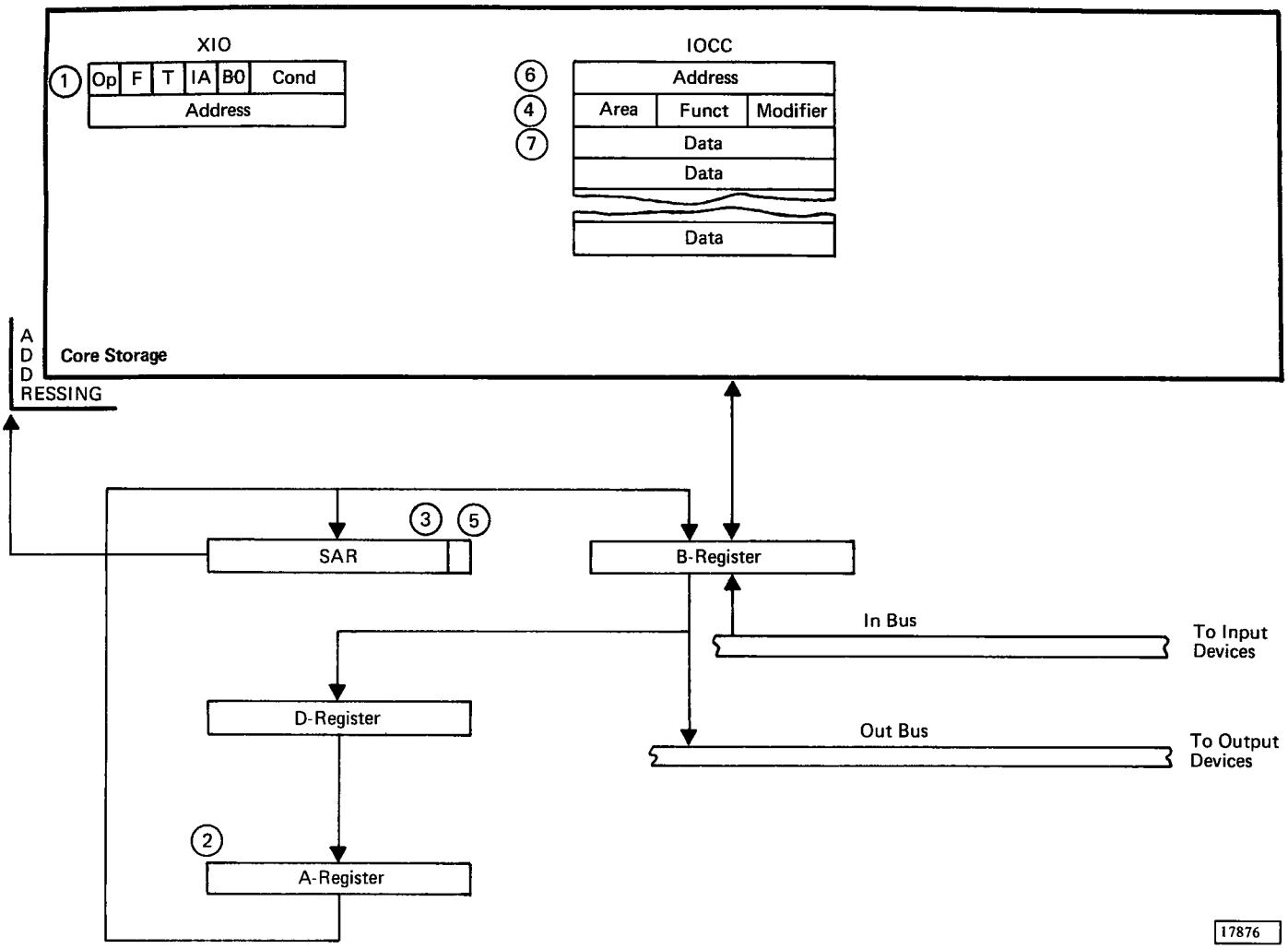

Figure 13. Direct Program Control Operation

It is up to the program to ensure, by testing the busy indicator, that the device has completed the previous operation and is ready to accept new information. Usually, no indication is given to signal incorrect use of the device. Blast instructions are available on some devices and can be used to clear a device that is hung up in a busy state. Caution should be used to ensure sufficient time to complete the previous XIO command before deciding to blast.

DATA CHANNEL CONTROL

Data channels provide a method of controlling data transfer between core storage and I/O devices without requiring execution of an XIO instruction to effect transfer of each data word. A data channel is initialized for a data transfer operation with a single XIO instruction. The XIO specifies the location of a data table in core storage and, if necessary, the number of words associated with the data transfer operation. The data channel then takes control of the data transfer operation while program execution resumes.

The data channel has priority over program execution to the extent that when an I/O device is ready to send or receive a data word, the data channel has the ability to suspend instruction execution, if necessary, while the data word is transferred to or from core storage. This transfer normally takes one core storage cycle (2, 2.25, or 4 μs) and is referred to as a cycle steal. As soon as transfer of the data word is completed, instruction execution resumes if it was suspended for the data transfer.

A data channel transfer operation may occur at the end of any core storage cycle and does not require

that an instruction in progress be completed. P-C data or logical conditions are not disturbed during data transfer via a data channel except for the core storage locations receiving data from an input device.

Three data channels are standard features of the 1800 system; 12 more are available on an individual basis. Thus, it is possible to have more than one data channel attempting data transfer at the same time. When this occurs, the data channels are serviced according to their assigned priority. This data channel priority is not related in any way to the interrupt feature.

The maximum time before the highest priority data channel is serviced is 2.25, 2.50, or 4.50 μs, depending on core storage cycle time. If more than one data channel requests data transfer, instruction execution is suspended until all requesting data channels have been serviced.

Devices operating under data channel control are relatively high-speed devices and include:

1442 Card Read Punch.
1443 Printer.
1810 Disk Storage.
2401/2402 Magnetic Tape Unit.
2790 Adapter.
Communications adapter.
Selector channel.
System/360 adapter.

Some devices operate under direct program control or data channel control, depending on the system configuration. These devices include:

Analog input.
Analog output.
Digital input.
Digital output.

Data channel devices are initialized with a single XIO initialize read or XIO initialize write. After a data channel device is initialized, the program is released for other processing.

Data Channel Functional Components

CHANNEL ADDRESS REGISTER (CAR): CAR is a 16-bit register used to store the core-storage address of the next word that will be addressed during an operation with its associated data channel. Each data channel has its own CAR and is assigned to an I/O device. A data channel and its associated CAR are selected when the assigned I/O device is addressed by the IOCC area code and modifiers.

CHANNEL ADDRESS BUFFER (CAB): CAB is a 16-bit register that is used by all CAR's to address core storage. When a data channel operation occurs, the CAR for the requesting data channel is transferred to CAB to address core storage. While CAB is addressing core storage, CAR is usually increased by 1 in preparation for the next data transfer.

Channel Address Register Checking

A CAR check is provided to ensure that the first word addressed by a selected CAR is the first word of the correct data table. The CAR check is performed in one of two ways, depending on whether the I/O device is capable of chaining data tables.

Non-chaining devices are:

1442 Card Read Punch.
1443 Printer.
1810 Disk Storage.
2790 adapter.
Selector channel*

Chaining devices are:

2401/2402 Magnetic Tape Unit.
Analog input.
Analog output.
Communications adapter.
Digital input.
Digital output.
System/360 adapter.

A CAR check is made for all devices after the IOCC address word is transferred to the selected CAR. A bit-by-bit comparison is made between the contents of the selected CAR and the contents of the B-register. If any of the corresponding bits are not equal, a CAR check error occurs. This error terminates subsequent data channel operations for the assigned I/O device and initiates an internal interrupt. The I/O device cannot request a data channel operation until the interrupt level status word for the internal interrupt level is sensed and the I/O device is reinitialized by another XIO.

Another CAR check is made for chaining devices each time the I/O device chains to a different data table. The CAR check at the beginning of the second data table and in all subsequent data tables in the

*Data chaining with the selector channel is accomplished through use of channel command words as described in the "Selector Channel" section.

chain is accomplished as follows: The first word of the data table (second data table, third data table, and so on) must contain its own address. After the first word of the data table is addressed, a bit-by-bit comparison is made between the contents of the selected CAR and the B-register. If any of the corresponding bits are not equal, a CAR check error occurs. Subsequent data channel operations are terminated, and a bit is set in the device status word for the device.

I/O Device Functional Components

WORD COUNT REGISTER: A word count register is provided in each of the following I/O devices assigned to a data channel:

1810 Disk Storage.
2401/2402 Magnetic Tape Unit.
Analog input.
Analog output.
Digital input.
Digital output.
System/360 adapter.

The word count register is loaded with the contents of the word count portion (bit positions 2 through 15) of the data table and is decreased by 1 each time a data word is transferred from or to the data table. For I/O devices without chaining ability, the word count must be stored in the first word of the data table. For devices with chaining ability, the word count must be stored in the first word of the first data table and in the second word of all subsequent data tables in the chain.

BYTE COUNT REGISTER: A byte count register is provided in each of the following devices assigned to a data channel:

Communications adapter (each line adapter).
Selector channel.

The byte count register for each line adapter is analogous with the word count register, except that the count represents the number of character locations supplied by the data table (two characters per word). The selector channel byte count register contains the number of eight-bit bytes in the input or output area. It is loaded from the byte count specified in the channel command word and usually decreased by 1 each time a byte is transferred from or to core storage. (See "Selector Channel" for details.)

The following table gives the word or byte count capacities for all data channel devices requiring word or byte count control:

Device	Number of Bits Available	Word Count Bit Positions	Max Count Accepted by Device
1443	7	9-15	60 or 72
1810	9	7-15	321
2401/2402	14	2-15	16,383
AI	14	2-15	16,383
CA (Line Adapter)	12	4-15	4,095
DAO	8	8-15	255
DI	8	8-15	255
Selector Channel	16	0-15	65,535
System/360 Adapter	14	2-15	16,383

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SCAN CONTROL REGISTER: A scan control register is provided in each device that has chaining capabilities. Scan control bits must be stored in the first word (bit positions 0 and 1) of the first data table and in the second word (bit position 0 and 1) of the second and all subsequent data tables in a chain. The following is a list of the devices that have a scan control register:

2401/2402 Magnetic Tape Unit.
Analog input.
Analog output.
Communications adapter (each line adapter).
Digital input.
Digital output.
System/360 adapter.

The scan control register controls I/O device and data channel operation at the end of the data table as follows:

Bit 0	Bit 1	
0	0	Perform single scan of data table and stop with an interrupt.
0	1	Perform scan of data table and stop (no interrupt).
1	0	Perform continuous scan of this data table or subsequent data table; cause an interrupt at the end of this table.
1	1	Perform continuous scan of this data table or subsequent data table; cause no interrupt.

Data Chaining

When a continuous scan is indicated by the scan control register in a device having chaining ability, the device automatically requests three data channel cycles after the word count has been decreased to 0. The first data channel cycle is used to transfer the word following the data table to the selected CAR. The address in this word is the address of the next data table. The second cycle addresses the first word of the new data table and performs a CAR check using the contents of this word. Therefore, the first word of the second data table must contain its own address. The third cycle addresses the second word of the data table and transfers it to the device. This word contains the scan control bits and word count for the data table. The I/O device is then ready for independent data channel operation.

In this manner, the data channel can be used to implement a scatter read/write mode; that is, data from various core storage locations can be transferred with one continued operation. This method of using the data channel in a continuous mode is called data chaining because the data tables are essentially connected together.

The length of time between data transfer cycles on a data chaining operation is a maximum of three core storage cycles on a device using the highest priority data channel. It may be greater than this for devices using lower priority data channels, depending on whether they must wait for higher priority data channel operations to be completed.

Data Channel Operation

Figure 14 illustrates the basic concept of data channel operation. All devices assigned to data channels use this basic concept, except for the selector channel and 2790 adapter. Concepts for these devices are presented in their respective sections of this manual.

The numbers that follow correlate with the circled numbers in Figure 14.

1. An XIO is read from core storage for execution.
2. The effective address (EA) of the XIO is developed in the A-register and transferred to the SAR. The EA is the address of the IOCC.
3. SAR bit position 15 is forced on to select location EA+1, which contains the IOCC area code, function code, and modifiers.
4. Area code, function code, and modifiers are transferred to the device specified by the area code via the out bus.
5. SAR bit position 15 is turned off to select location EA, which contains the IOCC address word.
6. The address word is transferred to the CAR for the selected data channel and device. The program is now released for other processing.
7. The contents of the selected CAR and of the B-register are compared. A CAR check occurs if they are found to be different.
8. The device requests a data channel operation that causes CAR to transfer to CAB. CAB addresses core storage while CAR is increased by 1.
9. The first word of the data table is transferred to the I/O device. This word contains the scan control bits (bit positions 0 and 1) and word count (bit positions 2 through 15). This completes the first data channel operation.
10. When another data channel operation is requested, CAR (increased in step 8) transfers the next higher address to CAB. CAB addresses core storage while CAR is increased by 1.
11. The first data word is transferred to or from the I/O device via the out bus. The word count register in the I/O device is decreased by 1, thus completing the second data channel operation.

Steps 10 and 11 are repeated each time the device requests another data channel operation. Between data channel operations, the P-C continues program execution. With each data transfer, CAR is increased by 1 and the word count is decreased by 1. This sequence continues until the last word of the data table is transferred. The last word is sensed by the word count reaching 0 or through some indicator in the device. If the device does not have chaining ability, no more demands for data transfer are made until the device is reinitialized with another XIO.

If the device has chaining ability and the scan control bits indicate a continuous scan, the device automatically requests three data channel operations to implement chaining to the next data table. The following numbered steps describe the chaining sequence and correspond to the circled numbers in Figure 14.

12. During the first data channel operation, the word following the last data word in the first table is transferred to the selected CAR. This word must contain the next table address.
13. When the next data channel operation is requested, CAR transfers its contents to CAB to address core storage.
14. The first word of the next data table is transferred to the B-register. This word must contain its own address.

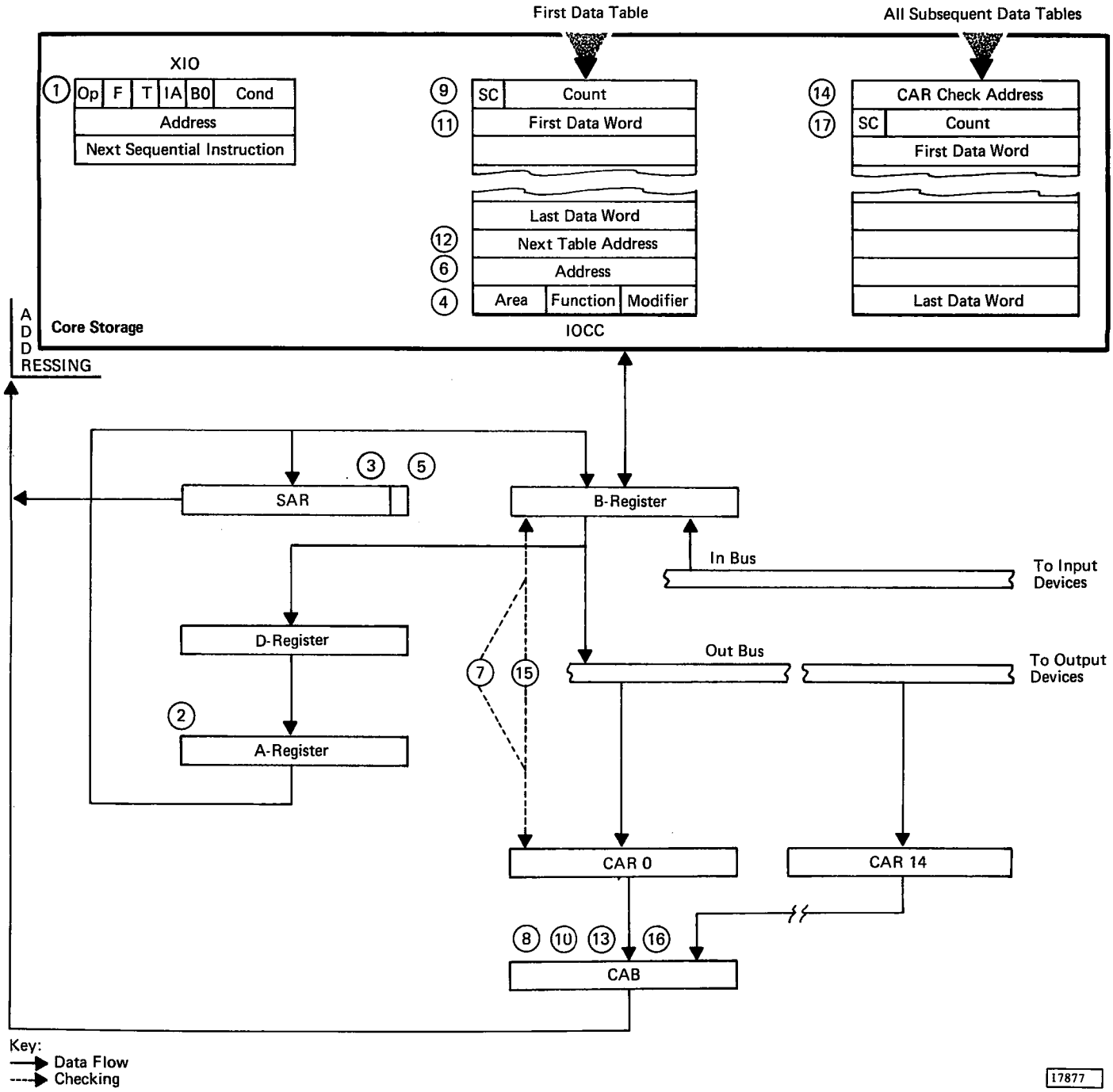

Figure 14. Data Channel Control Operation

15. The contents of the selected CAR and of the B-register are compared. If they are alike, CAR is increased by 1; otherwise, a CAR check occurs.
16. When another data channel operation is requested, CAR transfers the next higher address to CAB. CAB addresses core storage while CAR is increased by 1.
17. The scan control bits and word count are transferred to the I/O device. This completes the chaining operation.

The data channel and device are now ready for continued data transfer operations via the data channel. Each time a data word is transferred, CAR is

increased by 1 and the word count is decreased by 1. This sequence continues until the word count reaches 0. When the word count reaches zero, operation continues in the manner indicated by the scan control bits for the current data table.

Data Overrun

A device operating asynchronously to the program could request data transfer but not receive service in the time alotted by the device because of other, higher priority devices. This condition, data overrun, can occur with both input and output devices. Devices with the potential for data overrun provide an indicator in their device status words to enable the program to detect this condition.

Data Channel Assignment

Data channels are assigned specific priorities in order to establish a sequence for servicing them when more than one data channel is attempting data transfer. Data channel 1 has the highest priority, and the order of the priority follows the numeric sequence of the data channel numbers, with data channel 15 having the lowest priority.

When a system is ordered, the various devices and features desired are automatically assigned to data channels according to the intrinsic data rates and operational characteristics of those devices and features. The following is a listing of the devices and features in the sequence that they are assigned to data channels. The first system-included device encountered in the list is assigned to data channel 1. Each subsequent device in the system configuration is normally assigned to the next sequential data channel.

Selector channel.
2401 model 3.
2401 model 2.
1810 - drive 1.
1810 - drive 2.
1810 - drive 3.
2401 model 1.
1442 (first).
1442 (second).
2790 adapter 1.
2790 adapter 2.
Analog input basic data channel adapter 2 (1801/2).
Analog input basic data channel adapter 1 (1801/2).
Analog input expander data channel adapter 2 (1826).
Analog input expander data channel adapter 1 (1826).
1443.
CA line adapter 1.
CA line adapter 2.
CA line adapter 3.
CA line adapter 4.
CA line adapter 5.
CA line adapter 6.
CA line adapter 7.
CA line adapter 8.
System/360 adapter.
Digital - analog output.
Digital input.

A different set of data channel assignments can be obtained upon request if unique requirements dictate different priorities. When changing data channel assignments from the normal priorities, the following considerations are important:

1. Assigning high intrinsic data rate devices such as the selector channel, 2401/2402, and 1810 to data channels with lower priorities than those specified in the preceding list may affect optimum performance in overlapped operations and result in random overrun conditions.
2. If two data channels are assigned to an analog-to-digital converter (random or comparator), analog input data channel adapter 2 must have a higher priority than analog input data channel adapter 1.
3. If the priority of the data channel assigned to a device is lower than the priority of a data channel assigned to digital input or digital output, then the device may become locked out during data channel operations with large data tables. This problem can be partially alleviated by using smaller data tables.

Two or more devices can share a data channel if desired, but concurrent operation of two devices sharing a data channel is not possible. When sharing data channels programming considerations and physical wiring limitations should be considered. IBM systems programs assume that no devices share data channels. The physical wiring limitations are presented in the 1800 Data Acquisition and Control System Configurator, Order No. GA26-5919.

INPUT/OUTPUT TERMINATION

Input/output operations using devices under direct program control are terminated when the device completes the single function requested by the program.

Data channel I/O operations are terminated when the end of the last core storage data table is reached and chaining is not specified.

INPUT/OUTPUT INTERRUPTS

Interrupts from I/O devices may occur because of completion of an I/O operation, certain error conditions, or operator intervention at the I/O device. These interrupts allow the P-C to provide the proper programmed response to conditions that occur in I/O devices.

Conditions responsible for I/O interrupt requests are preserved in the device status word for each I/O device until they are reset by an XIO sense device with reset (modifier bit 15 on) from the program. Interrupt philosophy and device status word are explained in detail under "Interrupt".

ONLINE DIAGNOSTIC CONSIDERATIONS

The 1800 system provides a means for limited online diagnosis of problems occurring in most data processing features without interrupting customer operations. Such online diagnosis is limited to cases in which it will not affect user operations. In any case, the user must be notified when any online diagnosis is performed.

A feature that makes this service approach possible is CE core storage. This storage is intended to be available for maintenance or diagnostic purposes at all times. It is particularly useful for operation of CE exerciser programs. Access to it is accomplished only by CE interrupt, unless the Features II Compatibility feature has been installed.

In a 2 or 2.25 μs system, CE storage is available in each 8K group. In a 4 μs system, it is available in only the first 8K, unless Features II Compatibility has been installed.

Features II Compatibility is installed only at the time the communications adapter, selector channel, or 2790 adapter is installed on the system. If any of these features has been installed, main storage programs can read or write in CE storage, although CE storage programs cannot read or write in main storage. Data written in CE storage by main storage programs may be lost if the area is needed for maintenance or diagnostic purposes.

Addresses for CE storage locations are shown in the following illustration.

	System Storage in 8k Increments							
	1st	2nd	3rd	4th	5th	6th	7th	8th
CE Storage Address in Hex	0000 ↓ 00FF	2000 ↓ 20FF	4000 ↓ 40FF	6000 ↓ 60FF	8000 ↓ 80FF	A000 ↓ A0FF	C000 ↓ C0FF	E000 ↓ E0FF
	1100 ↓ 11FF	3100 ↓ 31FF	5100 ↓ 51FF	7100 ↓ 71FF	9100 ↓ 91FF	B100 ↓ B1FF	D100 ↓ D1FF	F100 ↓ F1FF

CE storage is accumulative with each 8k increment. For example, a system with three 8k increments contains CE storage shown by shaded area.

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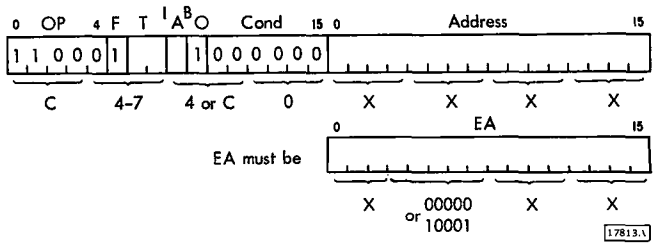
To assist CE's in maintaining complex I/O devices such as the communications adapters (CA's), 2790 adapters, and selector channel, the Multiprogramming Executive (MPX) Operating System accumulates the following error information:

1. Error logs for CA's, 2790 adapters, and selector channel.
2. Tables of error statistics for each CA line adapter.
3. A CA trace buffer.

These error logs and statistics are invaluable aids in online diagnosis and substantially reduce the time required to service these devices. If a 2790 system is used with the 1800 system without the associated MPX error logging support, the customer must be prepared to relinquish the 1800 system for offline diagnosis and maintenance of the 2790 system. In addition, provisions for error logging as a diagnostic aid should be included in the customer programs.

MPX maintains the error logs and statistics tables in CE storage on a real-time basis. Seven modified instructions are used by MPX to maintain the error information in CE storage. The instructions are described in the following paragraphs.

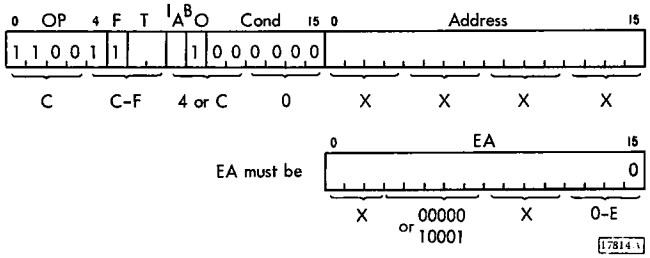
Load Accumulator (LD)



DESCRIPTION: The contents of the CE storage location specified by the effective address (EA) of the instruction replace the contents of the accumulator (A). The contents of the CE storage location are unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

INDICATORS: The carry and overflow indicators are not changed by this instruction.

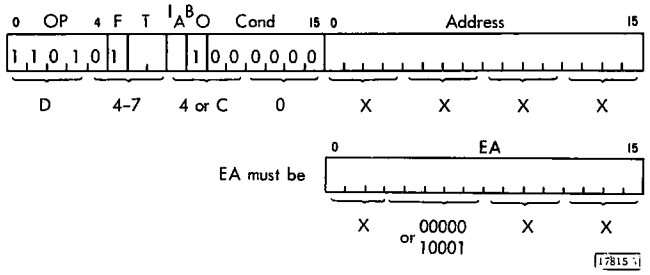
Load Double (LDD)



DESCRIPTION: The contents of the CE storage location specified by the effective address (EA) of the instruction and the next higher CE storage location (EA+1) are loaded into the accumulator (A) and its extension (Q), respectively. The EA of the instruction must be an even address for correct operation. If the EA is odd, the contents of that location are entered into both A and Q. The contents of CE storage are unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

INDICATORS: The carry and overflow indicators are not changed by this instruction.

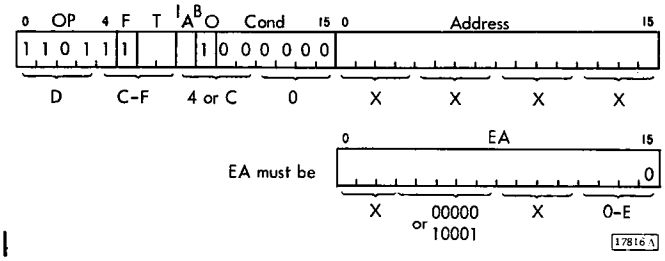
Store Accumulator (STO)



DESCRIPTION: The contents of the accumulator (A) replace the contents of the CE storage location specified by the effective address (EA) of the instruction. The contents of A are unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

INDICATORS: The carry and overflow indicators are not changed by this instruction.

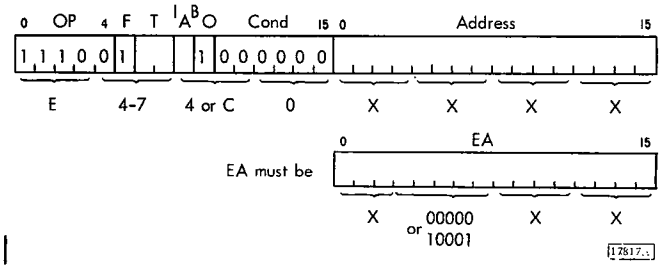
Store Double (STD)



DESCRIPTION: The contents of the accumulator (A) and its extension (Q) are stored at the CE storage location specified by the effective address (EA) of the instruction and the next higher CE storage location (EA+1), respectively. The EA of the instruction must be an even address. If the EA is odd, the contents of A are stored at the EA, and the contents of Q will not appear in CE storage. The contents of A and Q remain unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

INDICATORS: The carry and overflow indicators are not changed by this instruction.

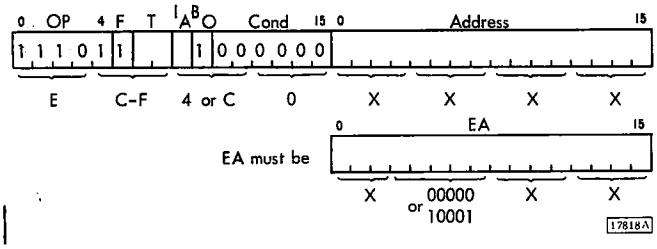
Logical AND (AND)



DESCRIPTION: The contents of the CE storage location specified by the effective address (EA) of the instruction are ANDed bit by bit with the contents of the accumulator (A). The result replaces the contents of A, and the CE storage location remains unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

INDICATORS: The carry and overflow indicators are not changed by this instruction.

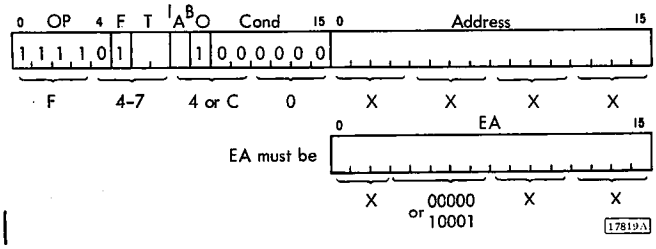
Logical OR (OR)



DESCRIPTION: The contents of the CE storage location specified by the effective address (EA) of the instruction are ORed bit by bit with the contents of the accumulator (A). The result replaces the contents of A, and CE storage remains unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

INDICATORS: The carry and overflow indicators are not changed by this instruction.

Logical Exclusive OR (EOR)



DESCRIPTION: The contents of the CE storage location specified by the effective address (EA) of the instruction are exclusive ORed bit by bit with the contents of the accumulator (A). The result replaces the contents of A, and CE storage remains unchanged. Indexing and indirect addressing are performed in the same manner as with normal instructions. (Indirect addressing uses main storage addresses.)

INDICATORS: The carry and overflow indicators are not changed by this instruction.

Customer Engineering Mode

A CE diagnostic program can enable or disable CE mode in certain I/O devices by executing an XIO instruction. The IOCC referenced by the XIO must contain the area code of the device to be placed in CE mode and a function of 000. CE mode is enabled if IOCC modifier bit 15 is on and disabled if modifier bit 15 is off.

When a device is in CE mode, its device status word (DSW) is altered to make the device appear not ready and not busy, which is offline status. The true status of ready and busy is located elsewhere in the DSW and is used for diagnosis.

Interrupts from a device operating in CE mode occur on the CE interrupt level and not on the normal assigned interrupt level of the device. Because CE interrupt level is the lowest priority level, service programs are executed only when main storage programs are not operating on interrupt routines.

Once a CE interrupt is recognized, all subsequent interrupts (except internal) are effectively masked until a branch out of CE interrupt (BOSC) is executed by the CE program. However, if an internal interrupt occurs while a CE interrupt is being serviced, the CE interrupt is reset and the program branches to the main storage program internal interrupt routine. Upon completion of the routine, instead of returning to CE storage, the program branches to the corresponding main storage address. Thus, a branch out of the internal interrupt routine returns to an address undefined by the program if the internal interrupt routine is entered by interrupting a CE program. However, most programming systems provide a restart procedure for internal interrupts.

The programmer should realize that a CE service program can possibly cause an interrupt from a wait instruction in main storage. When this occurs, the branch out of the CE interrupt program will be to the instruction following the wait instruction.

CE interrupt utilizes core storage locations /0001, /0002, and /000A. A CE interrupt stores the contents of the instruction (I) register at location /000A in main storage (even if this location is storage protected) and branches to location /0001 in main storage or location /0001 in CE storage, depending on the position of the aux/main switch on the CE panel. A branch out of CE interrupt returns indirectly to the main storage program via location /000A.

Interrupt

To allow for coordination of overlapped I/O operation and provide for a smooth flow of productive processing, a method of switching from one program routine to another is necessary. For this purpose, the 1800 includes an interrupt feature.

The interrupt feature provides an automatic branch from the normal program sequence. The branch is caused by an external or internal condition. Examples of conditions which would normally be used to cause interrupts are:

- An external process condition that requires an immediate change in program execution has been detected.
- A device, such as the printer-keyboard, has completed the transfer of a character and now requests the next character.
- A magnetic tape unit initialized and selected on a data channel has completed the required data transfer and signals the processor-controller with a scan complete.
- An interval timer has concluded the recording of a preset time interval.
- An undefined operation code has been detected during instruction readout and therefore cannot be executed.

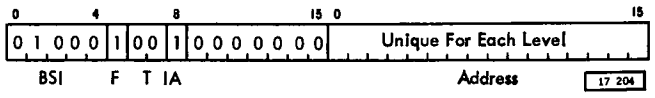
INTERRUPT PHILOSOPHY

Because of the large number and widely varying types of interrupt requests, it is often not practical to cause a branch to a unique address for each request. For the same reason, it is frequently not desirable to use only one branch address for all interrupt requests and to require the program to determine the individual request(s) requiring service. Therefore, it is expedient to group individual requests into a lesser number of priority levels. This accomplishes two functions. First, it allows all interrupt requests common to a specific interrupt level to have the privilege of interrupting immediately if the only other requests present are of a lower priority level. Conversely, it permits interrupt requests connected to a higher priority level to temporarily terminate servicing on a lower level and immediately interrupt to the higher priority level. Service is returned to the initial request only after all higher level requests have been serviced. Second, because a unique branch can be defined for each interrupt priority level, many interrupt requests can be assigned to a common priority level and be serviced by a common interrupt subroutine.

OPERATING CHARACTERISTICS

The important operating characteristics of the 1800 interrupt system are as follows:

1. When an interrupt request is recognized, the P-C inhibits normal access to core storage, generates a branch and store instruction register (BSI) instruction with indirect addressing, and places the instruction in the B-register. The format of this forced BSI is shown in the following illustration. The content of the address portion of the BSI is unique for each interrupt level and denotes the core storage location containing the indirect address (interrupt vector) for that level.



2. The first request recognized on a given priority level prevents future requests on that or lower priority levels from interrupting until the service completion of the first interrupt is signaled by a branch out operation. However, interrupts that occur on the same level for which an interrupt is being serviced can be recognized and serviced by the program if the interrupt level status word (ILSW) is interrogated again before the branch out is executed. If an interrupt request is detected for a higher priority level than that in progress, the program is immeidately interrupted again. This is called nesting of interrupts.
3. When more than one request is connected to any one priority level, the program must identify the individual request(s) causing the priority level to be active.

4. After service completion of any level interrupt, the priority circuits must be signaled to reset the priority status of the highest priority level that is active. This reset permits lower priority requests, that may have been temporarily constrained, to be accepted by the P-C. The reset is accomplished by issuing a branch out of interrupt (BOSC) instruction. This instruction should not be confused with a branch or skip on condition (BSC) instruction used in normal subroutine linkage back to a mainline program. The difference is that bit 9 (BO) is on for a BOSC and off for a BSC.

INTERRUPT LEVELS

As shown in Figure 15, a maximum of 27 interrupt levels are available for grouping interrupt requests. Internal, trace, CE, and 12 external interrupt levels are standard features. Twelve additional external interrupt levels (two groupings of six each) are available as special features. Note in Figure 15 that the priority level of each interrupt, as well as its unique core storage address associated with the forced BSI, are listed in decimal form. Note also that all but the trace and CE interrupt levels have an interrupt level status word (ILSW). The ILSW is used to identify the specific interrupt request(s) causing the interrupt level to request service.

Interrupt	Priority Level	Core Storage Location		ILSW	
		Decimal	Hex		
Internal	1	8	8	Yes	Basic
Trace	26	9	9	No	
** CE	27	10	A	No	
*External 0	2	11	B	Yes	
1	3	12	C	Yes	
2	4	13	D	Yes	
3	5	14	E	Yes	
4	6	15	F	Yes	
5	7	16	10	Yes	
6	8	17	11	Yes	
7	9	18	12	Yes	
8	10	19	13	Yes	
9	11	20	14	Yes	
10	12	21	15	Yes	
11	13	22	16	Yes	
12	14	23	17	Yes	Special Feature Group 1
13	15	24	18	Yes	
14	16	25	19	Yes	
15	17	26	1A	Yes	
16	18	27	1B	Yes	
17	19	28	1C	Yes	
18	20	29	1D	Yes	Special Feature Group 2
19	21	30	1E	Yes	
20	22	31	1F	Yes	
21	23	32	20	Yes	
22	24	33	21	Yes	
23	25	34	22	Yes	

* External interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE interrupt stores the return link in core storage location /000A and starts execution at core storage location /0001. Interrupts are prevented in the same manner as for the standard forced BSI.

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Figure 15. Interrupt Levels

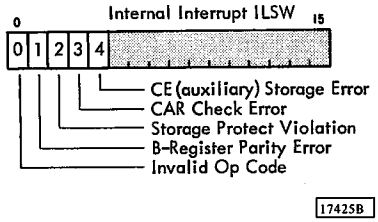
Internal Interrupt

The internal interrupt is a processor-controller interrupt that occurs when any one of the following four error conditions occurs:

1. An invalid Op code is detected.
2. A parity error (even number of bits on) is detected in the B-register during data transfer to or from core storage.
3. A storage protect violation occurs from an attempt to write into a "read only" core storage location.
4. A channel address register (CAR) check error occurs either as a CAR check or as the result of a parity error having caused a command reject.

Each of these four internal error conditions is assigned to a specific bit position in the internal interrupt ILSW (bit positions 0 through 3). If your system has the data channel expander feature, an 1803 Core Storage Unit, a selector channel, a communications adapter, or a 2790 adapter, an additional indicator is provided in the internal interrupt ILSW (bit position 4). This indicator is the CE (auxiliary) storage error indicator and is turned on if the condition causing the internal interrupt occurs while CE storage is being accessed. The condition causing the internal interrupt will also be indicated in the ILSW (bit positions 0 through 3).

All internal interrupt ILSW indicators are reset when the ILSW is sensed to determine the interrupting condition. Internal interrupt conditions are assigned to the ILSW as shown in the following illustration.



The internal interrupt level cannot be masked (prevented from causing an interrupt). However, an XIO or BSI prevents an internal interrupt for one instruction.

Trace Interrupt

A trace interrupt occurs after every instruction if the processor-controller is in program operation with the console mode switch in the trace position. Trace interrupt cannot be masked and does not have an ILSW. However, an XIO prevents a trace interrupt for one instruction.

CE Interrupt

The CE (customer engineer) interrupt can be initiated from the CE panel or from a device operating in CE mode. CE interrupt cannot be masked and does not have an ILSW. However, an XIO or BSI prevents a CE interrupt for one instruction.

CE interrupt is the lowest level interrupt on the system. However, all higher priority interrupt levels (except internal interrupt) are effectively masked once CE interrupt is recognized by the processor-controller.

External Interrupts

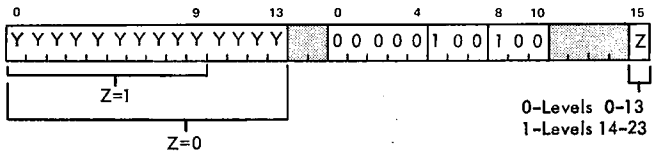
External interrupts can be initiated by any of the devices on the system. A maximum of 16 interrupt requests from devices on the system can be grouped to one external interrupt level. The interrupt requests are assigned to external interrupt levels by the user. Each external interrupt level can be masked or unmasked by the program. An XIO or BSI also prevents external interrupts for one instruction. An ILSW is provided for each external interrupt level to enable identification of the specific interrupt request(s) causing the interrupt level to request service.

Interrupt Level Masking

A mask register is provided for masking and unmasking of external interrupt levels. An interrupt level that is masked cannot initiate a request for service until it has been unmasked. Therefore, an interrupt request on a level that is masked does not cause a request for service, and no record of the interrupt request is made in the processor-controller. However, the interrupt request is retained by the device adapter for recognition when the interrupt level is unmasked.

All external interrupt levels are automatically masked when the reset or immediate stop switch is pressed, or when electrical power is first applied to the processor-controller. They remain masked until unmasked by the program.

For program operation, XIO control is used to control the mask register. Two XIO controls are required to mask/unmask all 24 external interrupt levels. Depending on modifier bit 15 of the input/output control command (IOCC), external levels 0 through 13 or 14 through 23 can be simultaneously masked/unmasked. If modifier bit 15 is off, the status of bits 0 through 13 of the IOCC address word determines whether external interrupt levels 0 through 13 are masked or unmasked. If modifier bit 15 is on, the status of bits 0 through 9 of the IOCC address word determines whether external interrupt levels 14 through 23 are masked or unmasked. In either case, an address bit being on masks the corresponding external interrupt level, while an address bit being off unmasks the corresponding external interrupt level. The format of the IOCC for the XIO control is shown in the following illustration. The execution of this instruction does not affect the contents of the accumulator.



Y = 1 masks corresponding interrupt level.

Y = 0 unmasks corresponding interrupt level.

Note that the area code is 00000 and that modifier bits 8 through 10 must be 100.

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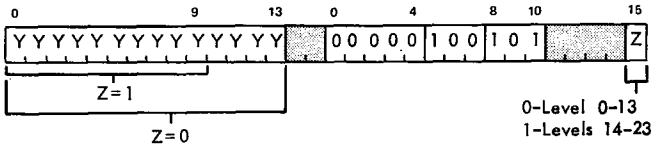
Note: Interrupt level status words, device status words, and process interrupt status words are not affected by the mask operation.

Programmed Interrupts

External interrupt levels can be activated by the program. An XIO control is used to turn on individual external interrupt levels so they will request service. This type of interrupt is known as a programmed interrupt. The external interrupt levels are divided into two groups (0 through 13, and 14 through 23) as in interrupt level masking. Therefore, two instructions must be executed to turn on external interrupt levels in both groups.

If the IOCC modifier bit 15 is off, the status of bits 0 through 13 of the IOCC address word determines which external interrupt levels (0 through 13) are turned on. If the IOCC modifier bit 15 is on, the status of bits 0 through 9 of the IOCC address word determines which external interrupt levels (14 through 23) are turned on. In either case, an address bit being on turns on the corresponding external interrupt level, while an address bit being off has no effect on the corresponding external interrupt level. The IOCC format for programmed interrupts is shown in the following illustration.



Y = 1 turns on corresponding interrupt level.

Y = 0 has no effect on corresponding interrupt level.

Note that the area code is 00000 and that modifier bits 8 through 10 must be 101.

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Programmed interrupts will not occur if either of the following conditions exists:

1. The interrupt level is masked before an XIO control attempts to turn on the corresponding interrupt level.
2. A programmed interrupt level is turned on, but an XIO control masks that interrupt level before the forced BSI occurs. As a result, the programmed interrupt level is turned off.

Programmed interrupts might not occur if an XIO control masks or unmasks any interrupt level before the forced BSI occurs for a programmed interrupt.

Another XIO control to turn on the programmed interrupt is needed to reinitiate the interrupt.

It should be noted that execution of an XIO control to turn on a programmed interrupt does not affect the interrupt level status words, device status words, or process interrupt status words.

Programmed Interrupt Programming Note

A BOSC following an XIO control which turns on an external interrupt level as high or higher than the level currently being serviced resets the programmed interrupt just turned on. For example, while in a routine servicing interrupt level 4, an XIO control to program interrupt on level 2 followed by a BOSC would reset programmed interrupt level 2 and not reset level 4. To prevent this condition the following technique can be used for programmed interrupts.

```
XIO     MSK1  }
XIO     MSK2  }   Prevent all interrupts
BOSC    + -Z      Clear current interrupt level
NOP
XIO     UMSK1 }
XIO     UMSK2 }   Restore interrupt mask register
XIO     PROG1     Set program interrupt
BSC     I EXIT    Exit current level
```

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Interrupt Polling

Interrupt requests from the I/O features and devices are assigned to interrupt levels according to customer requirements. The statuses of the interrupt requests are sent to the processor-controller via the in-bus. Since interrupt requests can occur at any time relative to program events, there must be some method of ensuring that interrupt requests are sent to the processor-controller only when the in-bus is not being used for data transfer. The method used in the 1800 is called interrupt polling.

Two polling cycles are required to sample the interrupt requests for all 27 interrupt levels. Interrupt requests for internal interrupt level and external interrupt levels 0 through 13 are polled as a group. Interrupt requests for external interrupt levels 14 through 23 as well as trace and CE interrupt levels are polled as another group. The group that is polled on any given cycle is not readily predictable because the first group polled after an interrupt is the group that was being polled when the interrupt occurred.

Both groups are polled during any core-storage cycle other than the first core-storage cycle of an instruction. During the first core-storage cycle of an instruction, only one group is polled; this group can be either 0 through 13, or 14 through 23. Therefore, unmasking an interrupt level for an instruction that takes only one core-storage cycle (MDX, LDX, LDS, for example) does not ensure that the interrupt requests for that level will be polled.

Any data channel (cycle steal) operation occurring during an instruction terminates interrupt polling. In this case, interrupt polling is not resumed until the first core storage cycle of the next instruction.

Interrupt polling is inhibited during:

1. XIO and BSI.
2. Load, display, or initial program load (IPL) modes.
3. Clear storage operations.

STATUS WORDS

The I/O devices of the 1800 system and some of the system features contain status indicators. The on/off condition of each status indicator informs the operating program of the status of an operation or the condition of a device.

Status indicators are also contained in the process being monitored or controlled by the 1800 system. Both system- and process-oriented indicators project their individual conditions to the processor-controller via the in-bus for program interrogation.

Some of the status indicators may reflect a condition in the device or process that requires a program response. These indicators are assigned to interrupt levels and initiate interrupt requests when they are turned on.

The status words used in the 1800 are:

- Device status words (DSW). The status word for the selector channel is known as the channel status word (CSW); it is functionally the same as a DSW.
- Process interrupt status words (PISW).
- Interrupt level status words (ILSW).

Device Status Word Indicators

DSW indicators usually fall into three general categories:

1. Error or exception interrupt conditions.
2. Normal data- or service-required interrupts.
3. Routine status conditions.

These indicators are always read into the accumulator (A) by means of an XIO sense device. They can then be interrogated under program control.

A unique DSW exists for each device. Some devices have more indicators than can be contained in one word. Therefore, more than one status word may be associated with a particular device. The area and modifier bits of the input/output control command (IOCC) specify the device whose DSW is to be sensed and, if the device has more than one status word, the particular word desired.

Some of the indicators in a DSW can be reset under program control. Modifier bit 15 being on in an XIO sense device specifies reset of all program-resettable indicators in the DSW sensed. Indicators in a DSW that cannot be reset by the program are turned off when the respective conditions in the device are reset. Any DSW interrupt indicator must be reset by the routine that services the interrupt. Otherwise, the on condition of the indicator will turn the interrupt bit right back on. A table of DSW's is provided in Appendix C. The functions of each indicator in a DSW are explained in the respective section for each device.

Since the P-C is much faster than the I/O devices, they must operate asynchronously. It is therefore possible to sense the status of a device during the short period of time that the status is being changed. When using the status of a DSW indicator to branch in a short program loop, the following technique should be used to ensure that the final status of the device is sensed.

1. With the resetting modifier bit off, sense the DSW.
2. When the status of the selected indicator changes, sense the DSW again with the resetting modifier bit on. The data from the last sense reflects the valid machine condition.

Process Interrupt Status Word Indicators

Process interrupt status word (PISW) indicators are physically located in the 1800 system. They are turned on by the closing of a contact or the shifting of a voltage in a remote customer process.

PISW's are read into the processor-controller (P-C) with an XIO sense device or XIO read. The difference between the function of the two instructions is where the PISW is stored. An XIO read stores the PISW at the core storage location specified by the address word of the IOCC. The XIO sense device stores the PISW in the accumulator. When a PISW is read using either of these two instructions, all indicators in the PISW are unconditionally reset.

Assignment of PISW Bit Positions

Process interrupt points are terminated on 16-position terminal blocks within the 1800 system. The terminal block positions are assigned to PISW's as specified by the customer on a PISW assignment form. The following paragraph defines assignment restrictions.

Twenty-four 16-point groups of process interrupt termination points are available. Each of these 16-point groups is divided into four sets of four points each for PISW assignment. The sets in each 16-point group are 0 through 3, 4 through 7, 8 through 11, and 12 through 15. Each set of four can be assigned to the same PISW or to different PISW's. Each PISW can have 16 points assigned (four sets of four points each); these points correspond to the positions of the PISW. As shown in Figure 16, for example, terminal block positions 0 through 3 may be assigned to bit positions 0 through 3 of one PISW; terminal block positions 4 through 7 may be assigned to bit positions 4 through 7 of a second PISW; and so on. In like manner, terminal block positions 0 through 7 could be assigned to bit positions 0 through 7 of one PISW, and terminal block positions 8 through 15 could be assigned to bit positions 8 through 15 of a second PISW. However, no cross assignment such as position 0 of the terminal block to bit position 1 of a PISW is permitted. Position 0 must be assigned to bit position 0, 1 to 1, ... and 15 to 15.

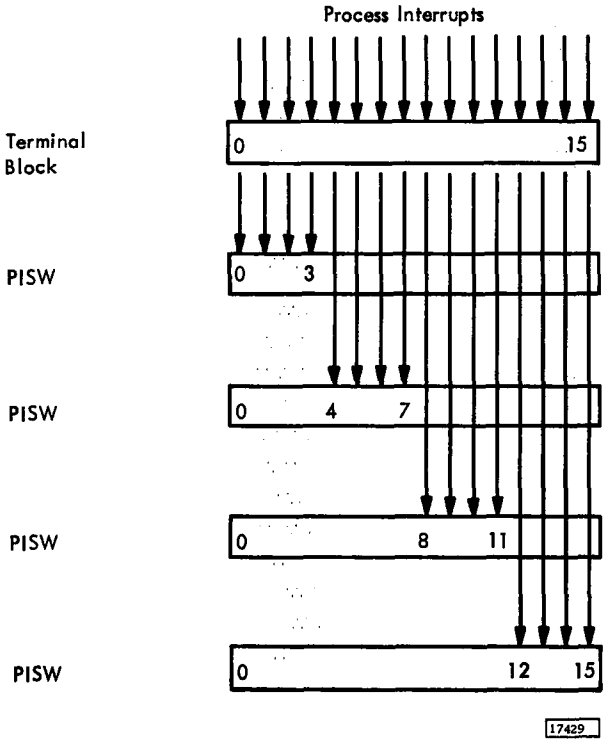


Figure 16. PISW Bit Position Assignment (Typical)

Process Interrupt Status Word Address Assignment

PISW's are considered to be digital inputs, but each PISW has its own unique address. Twenty-four PISW's are available and are numbered 1 through 24. The PISW's are assigned addresses 2 through 25, respectively. PISW's are addressed by modifier bits of an XIO sense device or XIO read. Process interrupts can be assigned in groups of 4 to any one of 24 PISW's (maximum 16 points per PISW). When sensed, all PI status bits assigned to that PISW will be reset.

Interrupt Level Status Words

The interrupt facility includes one 16-position interrupt level status word (ILSW) for each interrupt level. (Trace and CE interrupt levels are exceptions, as they are unique interrupts and require no ILSW for interrupt request identification.)

As shown in Figure 17, each ILSW bit is assigned to a PISW or a specific device. PISW indicators are ORed into the assigned ILSW bit position. Similarly, all DSW interrupt indicators from the assigned device are ORed into the single ILSW bit position assigned to the device. Whenever any one of the ORed interrupt indicators from a PISW or DSW is active, the respective ILSW bit is turned on, causing the interrupt level to request service.

An ILSW is read into the accumulator by an XIO sense interrupt level. The programmer does not specify the particular ILSW in the XIO sense interrupt level used to read an ILSW. This specification is fixed; that is, each ILSW is assigned to its interrupt level by means of circuitry. The XIO sense interrupt operation places the ILSW of the highest priority level requesting service into the accumulator.

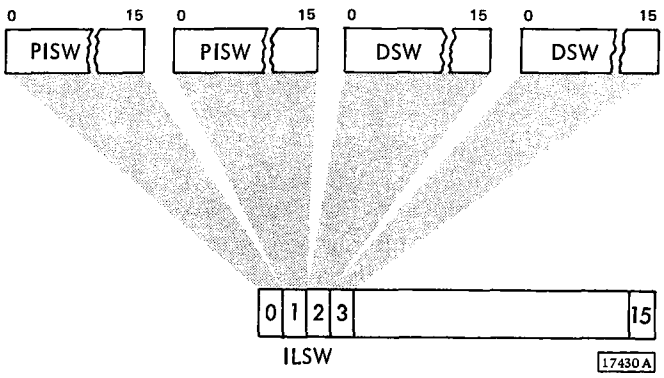


Figure 17. Relationship of Status Words

After a request for service has been recognized and the ILSW of the requesting interrupt level has been read into the accumulator by an XIO sense interrupt level, the program determines which bit position in the ILSW caused the interrupt. This bit position identifies the DSW or PISW that has the interrupt-initiating indicator. The DSW or PISW is then analyzed by the program to determine which indicator in the DSW or PISW caused the interrupt.

It should be noted that except for internal interrupts, none of the DSW/PISW interrupt indicators ORed into ILSW bit positions is reset when the ILSW is read into the accumulator. The indicators in a DSW are not reset until they are read into the accumulator with an XIO sense device with reset (IOCC modifier bit 15 on). Indicators in a PISW are unconditionally reset when read by an XIO sense device or XIO read.

Interrupt Level Status Word Assignment

Each external interrupt level has its own 16-position interrupt level status word (ILSW) to reflect the status of interrupt requests connected to the interrupt level. Each device or PISW is assigned to a specific ILSW, and a particular bit position in that ILSW, by the customer. Because each interrupt level has a fixed priority, the customer essentially assigns interrupt priority when he assigns a device or PISW to an ILSW bit position.

Devices and PISW's are assigned to ILSW bit positions on the interrupt level status word assignment form. Assignment of devices or PISW's to ILSW's should begin with the leftmost bit position (bit 0) and progress to the next higher bit position for each device or PISW assigned to the ILSW. The following paragraphs describe restrictions on ILSW assignment.

A device (DSW) or PISW must be assigned to one and only one ILSW bit position. For example, each device in the first group of four 1816/1053's must be assigned to a different ILSW bit position for the same interrupt level. Similarly, each device in the second group of four 1816/1053's must be assigned to a different ILSW bit position for the same interrupt level. (It can be the same interrupt level as the first group.)

If the process interrupt routine in the Time Sharing Executive System or Multiprogramming Executive Operating System is used, each PISW must be assigned to its corresponding ILSW. For example, PISW 1 must be assigned to ILSW 0, PISW 2 must be assigned to ILSW 1,... and PISW 24 must be assigned to ILSW 23. Three PISW's are provided with each process interrupt adapter. The PISW's for any one process interrupt adapter must be assigned within either 0 through 11 or 12 through 23 interrupt level groupings. In addition, only one area code may be represented by any one ILSW bit.

The following interrupt requests must be assigned to an ILSW for all systems:

TI	Timer interrupt (combined interrupt from all three interval timers)
Typ-1	First 1053 or 1816 (circuitry basic in processor-controller)
2401/2	1802 processor-controller only
CI	Console interrupt (can be assigned to any unused bit position on any available interrupt level)

The following interrupt requests must be assigned to an ILSW only if the feature is ordered for the system:

Typ-2, Typ-3, Typ-4	1053's
Typ-5	1053 or 1816
Typ-6, Typ-7, Typ-8	1053's
1054/5	1054/1055
1442-1	First 1442 adapter
1442-2	Second 1442 adapter
1443	1443 controls
1627	1627 controls
1810-1	1810 (first drive) model A1, A2, A3, B1, B2, or B3
1810-2	1810 (second drive) model A2, A3, B2, or B3
1810-3	1810 (third drive) model A3 or B3
2790-1	First 2790 adapter
2790-2	Second 2790 adapter
360/CA	System/360 adapter
AIB	Analog input basic (any ADC in 1801/2)
AIBC	Analog input basic with comparator (in 1801/2)
AIE	Analog input expander (in 1826)
AIEC	Analog input expander with comparator (in 1826)
CA/LA1	First CA (line adapter 0)
CA/LA2	First CA (line adapter 1)
CA/LA3	Second CA (line adapter 0)
CA/LA4	Second CA (line adapter 1)

CA/LA5	Third CA (line adapter 0)
CA/LA6	Third CA (line adapter 1)
CA/LA7	Fourth CA (line adapter 0)
CA/LA 8	Fourth CA (line adapter 1)
DAO	Digital-analog output
DI	Digital input (DI, PC, or PISW)
SC	Selector channel

PROGRAMMED OPERATION

The 1800 system may be programmed to service interrupt requests in several alternate manners, depending on the interrupt configuration. For example:

- A PISW and other interrupt requests are intermixed on the same interrupt level. If a process interrupt request occurs, the ILSW is interrogated first and the PISW is interrogated subsequently.
- PISW's and other interrupt requests are intermixed on the same interrupt level, but the PISW's are given priority on that level. In this case, the PISW's (typically one) are interrogated directly, before the ILSW.
- An interrupt level is completely reserved for PISW's. In this case, the ILSW is interrogated to determine which PISW contains the actual interrupt request.
- An interrupt level is completely reserved for only one PISW. In this case, the program can go directly to the PISW containing the interrupt request.

In general, an interrupt request is recognized at the completion of the instruction being executed when the interrupt request occurs. Exceptions to this practically instantaneous recognition are as follows:

- The instruction being executed when the interrupt request occurs is an XIO, an interrupt-forced branch and store instruction register (BSI), or a normal BSI. These instructions effectively mask all interrupts during their execution and the execution of the next instruction.
- The interrupt request level is masked. The request will be retained by the device adapter for recognition when the interrupt level is unmasked. Programmed interrupts are not retained if masked prior to the execution of the forced BSI for that interrupt.
- The interrupt request is on the same or lower priority level than an interrupt being serviced.

Programming Details

When an interrupt request is recognized, a forced BSI with indirect addressing is generated and executed. The address portion of the forced BSI is unique for each interrupt level, as shown in Figure 15. Program operation from this point is shown in Figure 18 and described in the following paragraphs. The circled numbers in Figure 18 correspond to the numbered descriptions.

1. The interrupt request occurs during execution of the main line program.

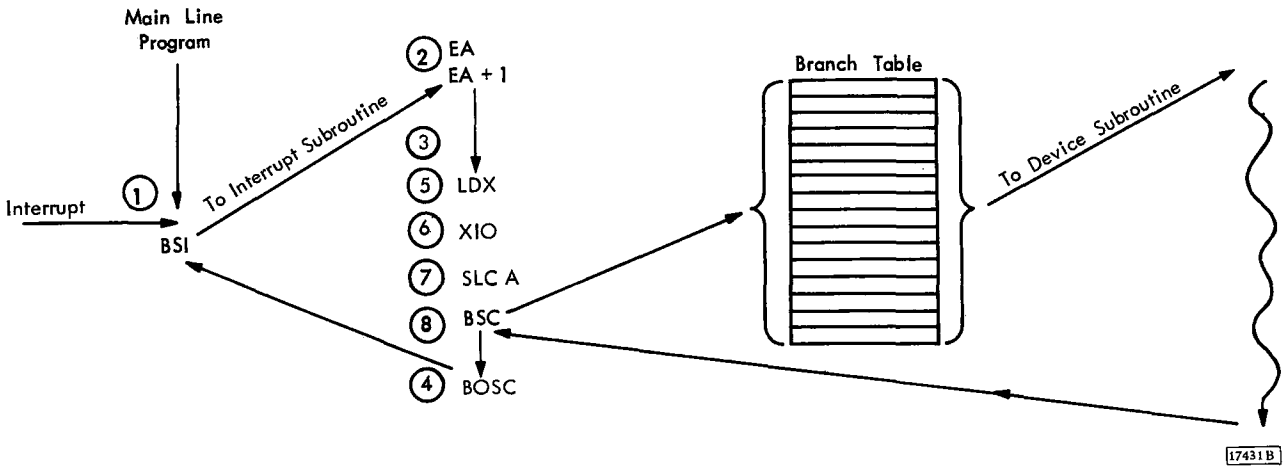


Figure 18. Program Identification of Interrupts

2. The forced BSI with indirect addressing stores the contents of the I-register at the effective address (EA) and causes a branch to the interrupt subroutine at EA + 1. The EA is the address that the user stores at the interrupt vector.
3. The interrupt subroutine stores all data and/or index registers that it will use. Then, before ending, the subroutine restores the same data and/or index registers.
4. The last instruction of the interrupt subroutine is a branch or skip on condition (BOSC, bit 9=1) that returns the program to the address previously stored at the EA of the forced BSI (step 2). This address is the location of the next sequential instruction in the mainline program. The BOSC also resets the interrupt level so that other lower priority levels can be recognized.

If a wait is operative when the interrupt request occurs, the wait is considered complete when the interrupt request is recognized. Following completion of the interrupt subroutine, the instruction immediately following the wait is executed.

Interrupt Request Identification

Because a number of interrupt requests can be assigned to any one priority level, it may be necessary for the program to analyze the ILSW of the requesting interrupt level to determine the source of the interrupt request signal. This analysis is accomplished within the interrupt subroutine as described in the following paragraphs. The numbered descriptions relate to the circled numbers in Figure 18.

5. A load index register (LDX) is used to load an index register with the number of interrupt request signals assigned to the ILSW.
6. An XIO sense interrupt level causes the ILSW of the interrupt level being serviced (highest priority level on) to be read into the accumulator. Only the function field of the input/output control command (IOCC) need be specified. The other fields of the IOCC are not used. The status of the indicators in the devices or PISW's assigned to the ILSW are not affected.
7. A shift left and count A (SLCA) is executed, with the index register loaded in step 5 specifying the number of shift counts. The resulting count in the index register corresponds to the first non-0 ILSW bit in the accumulator.
8. A branch or skip on condition (BSC) with indirect addressing and indexing is executed. The index register used contains the count corresponding to the first non-0 bit in the accumulator. The address portion of the BSC contains the address of the first word of a branch table.

The branch table (Figure 19) consists of a table of addresses. Each address is related to an interrupt request position in the ILSW and specifies the location of a subroutine for that particular interrupt request. For example, if ILSW bit position 0 is on, the last word of the branch table is used and the BSC branch is to the address stored in the last word of the table. If ILSW bit position 1 is on, the BSC branch is to the address stored in the next to the last word of the branch table, and so on.

The preceding sequence of instructions locates the specific subroutine for the ILSW bit that initiated the interrupt. It should be noted that each time the accumulator is shifted (step 7), the shift count is decreased by 1. As the shift count is decreased, the indexed address for the BSC is decreased. Effectively, the branch address of the BSC begins with the address located in the last word of the branch table and progresses toward the first word of the branch table each time the accumulator is shifted. The following is an example of interrupt request identification:

1. Load Index Register: Index register 1 (XR1) is loaded with the maximum number of interrupt request signals connected to the level

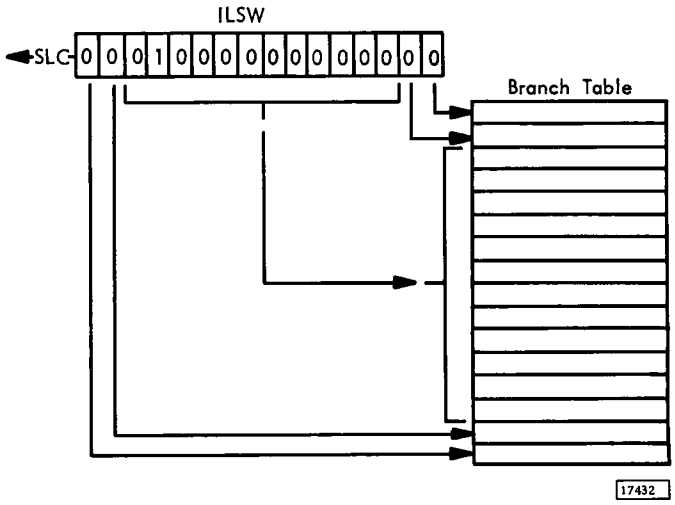
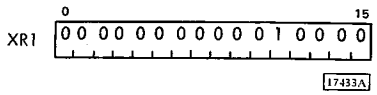
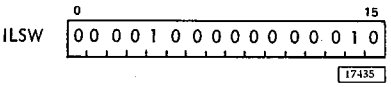


Figure 19. ILSW Branch Table

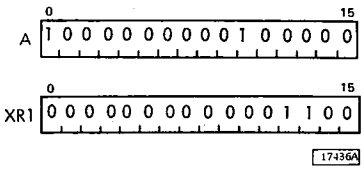
which caused the interrupt. (In this example, assume 16 request lines are connected to the interrupting level.) XR1 appears as shown in the following illustration.



2. Execute I/O: The XIO references a sense interrupt IOCC. The sense interrupt IOCC causes the ILSW of the interrupting priority level to be loaded into the accumulator. The accumulator (for this example) appears as follows:



3. Shift Left and Count: This instruction normalizes the accumulator and leaves a remainder count in the index register. Note in the following illustration that four shifts have reduced the value in XR1 from 16 to 12. Also note that bit position 8 and 9 in the index register are set to 0's regardless of their previous status, and that bit positions 0 through 7 remain unchanged.



4. Branch or Skip on Condition: This instruction, with both indexing and indirect addressing, provides a branch to a subroutine. The location of the subroutine is specified by the EA of the instruction. In this example, EA equals the value in the branch table word located at XR1 (12), plus the address portion of the instruction.

Device Indicator Identification

If the device or PISW requesting service has more than one possible interrupt condition, the program must determine which indicator in the DSW or PISW is responsible for the interrupt request. This identification can be made in almost the same manner as previously described in steps 5 through 8, with the following differences:

1. The LDX (step 5) loads the index register with the maximum number of indicators assigned to the DSW or PISW instead of the number of interrupt request signals assigned to the ILSW.
2. An XIO sense device instead of an XIO sense interrupt level is executed in step 6. The area and/or modifier codes must specify the device or the status word.
3. SLCA and BSC (steps 7 and 8) should be programmed so that all possible interrupting conditions are checked; that is, even if one condition is on, the other conditions are not assumed to be off.

If a device is responsible for an interrupt, the interrupt indicators for that device must be reset after service is complete, but before the branch out of interrupt is performed. This reset is accomplished by issuing an XIO sense device with reset. If a PISW is responsible for an interrupt, the PISW indicators are automatically reset when the PISW is read or sensed for device indicator indentification.

Interrupt Programming Notes

If an interrupt subroutine can be entered from more than one interrupt level, return addresses and intermediate subroutine results can be lost unless care in programming is exercised.

It should also be noted that if only one device or PISW (one interrupt request signal) is assigned to an interrupt level, the program can be written so that only the DSW or PISW is read into the accumulator and interrogated. Because only one interrupt request is assigned to the interrupt level, the ILSW need not be interrogated.

Storage Protection

Storage protection is the ability to protect the contents of core storage locations from change caused by erroneous storing of information during the execution of a program. In the 1800 system, this protection is achieved by providing each core storage location with a storage protect bit. The status of each core storage location is identified as either "read only" or "read/write" by the condition of the storage protect bit.

Read only status is indicated by the storage protect bit being on. A core storage location with read only (protected) status can be accessed, its contents read into the B-register, and its contents regenerated into the same core storage location. However, new information cannot be written into a protected core storage location.

Read/write status is indicated by the storage protect bit being off. A core storage location with read/write (nonprotected) status can be accessed, its contents read into the B-register, and its contents regenerated into the same core storage location. New information can also be written into a nonprotected core storage location.

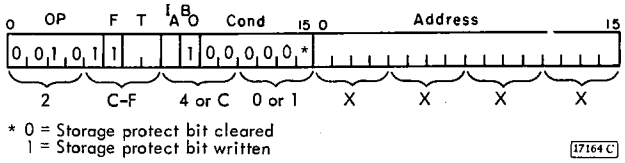
The storage protection feature is not extended to include CE storage with systems that include any of the following: the data channel expander feature, an 1803 Core Storage Unit, a selector channel, a communications adapter, or a 2790 adapter. Therefore, storage protection in CE storage is not possible with these systems.

In systems without the features mentioned in the preceding paragraph, the storage protection feature is extended to include CE storage. Storage protection in CE storage is possible with these systems.

Writing or Clearing Storage Protect Bits

Since each core storage location has its own storage protect bit, any location may be given read only or read/write status. This is accomplished under program control using the store status (STS) instruction with bit 9 (BO) on. The execution of this instruction is under control of the write storage protect bits switch on the processor-controller console. When this switch is in the yes position, STS can change the storage protect bits according to condition bit 15 of the instruction. When the write storage protect bits switch is in the no position, an STS with bit 9 (BO) on performs as a no-operation.

The format of the STS is shown in the following illustration. A detailed explanation of the instruction can be found under "Store Status (STS)" in the instruction set section of this manual.



Storage Protect Violation

Any attempt by the program to write information into a read only protected core storage location results in a storage protect violation. If a storage protect violation occurs at any time other than during data transfer from an I/O device to core storage, an internal interrupt (highest priority interrupt) occurs. Bit 2 of the interrupt level status word for internal interrupt is turned on. The contents of the protected core storage location are not changed. Note that if the console disable interrupt switch is on, internal interrupts are prevented.

If a storage protect violation occurs during data transfer from any I/O device (except interval timers) to core storage, the protected data remains intact and the storage protect violation indicator is turned on in the device status word associated with the I/O device. In this case, no internal interrupt occurs.

When any storage protect violation is detected and the console check stop switch is on, the processor-controller stops at the end of the core storage cycle in which the storage protect violation is detected. If the console check stop switch is off when a storage protect violation is detected, an internal interrupt is initiated or the storage protect violation indicator in the appropriate device status word is set as described in the preceding paragraphs.

Any attempt by the program to read a word having incorrect parity (even number of bits on) from a core storage location results in a parity error. This includes data transfer to an I/O device and initialization cycles (and loading of the channel address register) during an XIO.

If a parity error occurs when reading a word from core storage at any time other than during data transfer to an I/O device, the parity error causes an internal interrupt. Bit 1 of the interrupt level status word for internal interrupt is turned on. Bit 4 of the interrupt level status for internal interrupt is also turned on if CE storage is being accessed at the time the error occurs. Bit 4 is provided only with systems that have the data channel expander feature, an 1803 Core Storage Unit, a selector channel, a communications adapter, or a 2790 adapter. If the disable interrupt toggle switch is on, internal interrupts are prevented.

If a parity error occurs when reading a word from core storage during data transfer to an I/O device, the parity error indicator is turned on in the device status word for that device. In this case, no internal interrupt occurs. It is the responsibility of the program operating that device to initiate retries or other error recovery procedures. The core storage word with incorrect parity can be found by using a routine that loads data from core storage into the accumulator and detects the parity error word at the time an internal interrupt occurs. For example:

```
                •                 •
                •                 •
                •                 •
        LDX     L1    INTRP       Setup interrupt branch address
        STX     L1    8
        LDX     L1    +32,767     XR1=Core storage size
LOOP    LD      1     0
        MDX     1     -1
        MDX           LOOP
                •                 •
                •                 •
                •                 •
INTRP   DC            0           Internal interrupt branch
                •                 •
                •                 •  XR1=Address of error word
                •                 •
        BOSC    1     INTRP       Check next word        23413A
```

Reading from core storage takes place as an instruction is read out to be executed, as an address is read out, and as data is read out. If a parity error occurs during instruction readout, instruction execution is not prevented. Therefore, programmed recovery may not be possible. Also, if a parity error causes an I/O device to reject an XIO initialize read or write during an XIO control cycle, a channel address register (CAR) check will also occur.

A parity check when trying to address CE storage with an invalid address causes an internal interrupt to be generated with bit 4 on in the ILSW.

A parity error also occurs if an attempt is made to store a word having incorrect parity during data transfer from an I/O device to core storage. In this case, the parity error indicator is turned on in the device status word for that device and no internal interrupt occurs. It is the responsibility of the program to initiate retries or other error recovery procedures.

It should be noted that any time a word is written into core storage (during data transfer from an I/O device to core storage), correct parity is automatically generated and stored with the word. Therefore, no parity error can occur when writing into core storage on data transfer from an I/O device; parity is not checked on the write cycle.

When any parity error occurs and the check stop switch is on, the processor-controller stops at the end of the core-storage cycle in which the parity error is detected. If the check stop switch is off, a parity error causes an internal interrupt or sets the parity error indicator in the appropriate device status word, as described in the preceding paragraphs.

Use of an invalid address when addressing CE core storage should be carefully avoided, because of resultant errors which are difficult to analyze and correct. Two separate types of invalid addressing are possible:

1. CE storage address bits 4, 5, and 6 should not be used independently or in any combination. If one or more of these bits are used with an LD, LDD, AND, OR, or EOR instruction and bit 9 of the instruction is on, then a parity error will occur. However, if one or more of these bits are used when addressing CE storage with an STO or STD instruction, nothing occurs and the instruction becomes effectively a no-op.
2. CE storage address bits 3 and 7 must be used together (both on or both off); bit 3 or bit 7 without the other is an invalid address. Use of one bit without the other when addressing CE storage with an LD, LDD, AND, OR, or EOR instruction causes a parity error and forces all bits on in some location of CE storage. Use of one bit without the other when addressing CE storage with an STO or STD instruction causes bits to be forced on in some location of CE storage, but no parity error occurs. When reading out the address in which all bits have been forced on, the storage protect bit is dropped and the character has correct parity.

Interval Timers

Three interval timers are provided. Each timer has a permanent time base, which can be selected by the customer (Figure 20). Each timer can be assigned a different time base.

The timers can be started or stopped individually under program control. Once started, the timers are automatically increased one count at a time through the cycle steal facilities of the processor-controller. The counts of the timers are maintained in core-storage locations /0004 (timer A), /0005 (timer B), and /0006 (timer C). A count is added to a timer each time the assigned time base period for that timer is completed. This count is automatic and does not require a program.

The count of the timers proceeds in a positive direction. When the count reaches the largest positive value (2^{15}-1), the count continues to the most negative value and then through the negative numbers (2's complement) toward zero. When the count reaches zero, an interrupt is requested on the level assigned to the timers. (All three timers are on the same interrupt level and are assigned to an interrupt level by the user.) The timer continues to count after the zero count has been reached.

Once a timer is operating, it continues to increment when the processor-controller is in run, trace, or single instruction with cycle steal mode. A wait may also be executed without affecting the ability of a timer to increment. Further, a timer continues to advance correctly even if it is protected with a storage protect bit. However, any other attempt by the processor-controller or an I/O device to alter the count in a protected timer will cause a storage protect violation.

The internal timers are driven by the basic CPU master oscillator, which has an accuracy limit of ± .05%. The internal timer accuracy is governed by this and will therefore be accurate to within 43 seconds per day, if used as a 'programmed real time clock'.

Core Storage Cycle Times	Available Time Bases (In milliseconds)									
2 or 2.25 µs	0.125	0.25	0.5	1	2	4	8	16	32	64
4 µs	0.25	0.5	1	2	4	8	16	32	64	128

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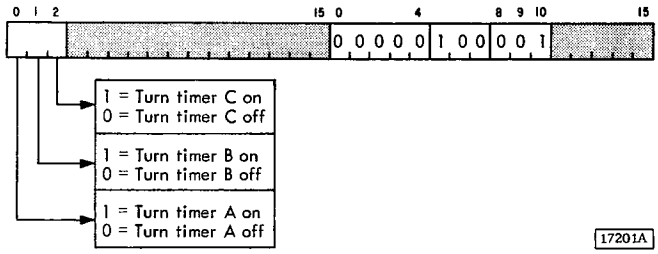
Figure 20. Interval Timer Time Bases

INTERVAL TIMER PROGRAMMING

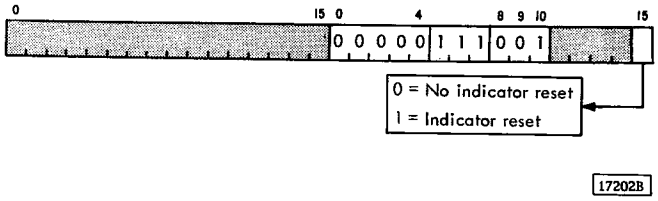
The interval timers are controlled by means of the execute I/O (XIO) instruction. To address the timers, the input/output control command (IOCC) referenced by the XIO must have an area code of 00000, and modifier bits 8 through 10 must be 001. IOCC's used to control the timers are described in the following paragraphs.

Control



This command turns the timers on or off according to the status of address word bit positions 0 through 2.

Sense Device



This command causes the interval timer device status word (DSW) to be loaded into the accumulator. The timer DSW and bit significance are shown in Figure 21.

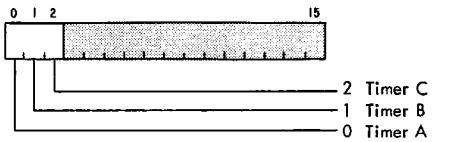


Figure 21. Interval Timer Device Status Word

The operations monitor is a basic feature of the 1800 system. It can be used to check program operation by detecting whether the processor-controller starts to execute a predetermined sequence of instructions within a preselected time interval. The operations monitor consists of an interval timer, an on/off switch on the processor-controller console, a time interval selection switch on the CE panel, and a set of contacts that close when the operations monitor times out. Any one of six time intervals (5, 10, 15, 20, 25, or 30 seconds) may be selected for the operations monitor. (The selection switch is located on the CE panel below the console.)

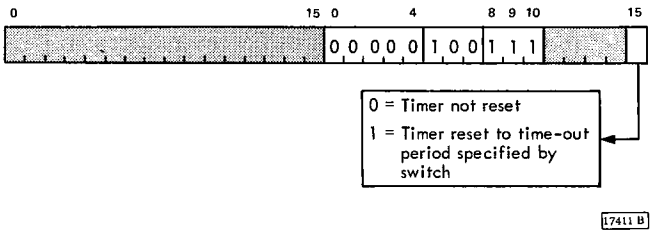
Once the operations monitor is activated by turning the operations monitor on/off switch to the on position, a reset monitor timer command must be executed by the program at intervals frequent enough to prevent the timer from timing out. If a reset timer command is not given during the selected time interval, the timer runs out and an alarm circuit is activated by closure of a set of contacts. The alarm may be audible and/or visible. (An alarm indicator light is located on the console.) Both the alarming device and power required to operate it must be supplied by the customer. (Power is limited to 30 volts and 1 ampere.)

Once the operations monitor alarm is on, it cannot be reset by the program; reset can only be accomplished by manually turning the operations monitor on/off switch to the off position. The cause of the timeout should be identified before the switch is turned back to the on position. Timeout can be caused by power failure, computer hang-up, computer looping, or any departure from the predicted instruction sequence in the program.

OPERATIONS MONITOR PROGRAMMING

The operations monitor is reset by means of the execute I/O (XIO) instruction. The input/output control command (IOCC) referenced by the XIO must have an area code of 00000 and modifier bits 8 through 10 must be 111 to address the operations monitor. The control IOCC, shown in the following illustration, is used to control the operations monitor.

Control



The operations monitor on/off switch must be in the on position to enable monitor operation. The time interval is specified by the time interval selection switch on the CE panel.

Processor-Controller Console

The processor-controller (P-C) console (Figure 22) provides the means for manual control of the P-C during debugging or operating phases.

The basic operating features and controls provide the facility to:

1. Start or stop instruction execution.
2. Address core storage.
3. Set up and store data or instructions.
4. Communicate with the program via sense or program select switches.
5. Control the cycling rate in the run, single storage cycle, single instruction, or single step modes.
6. Interrupt the program manually.
7. Trace each instruction.
8. Reset all control circuitry and storage.
9. Turn power on and off.
10. Indicate basic machine conditions and status.
11. Display storage words and register data.
12. Write or clear storage protect bits.
13. Clear core storage.

PUSHBUTTON SWITCHES AND LIGHTS

There are two rows of pushbutton switches and lights. One row is at the top of the console (Figure 23); another is at the bottom (Figure 24). The following paragraphs describe the functions of these switches and lights.

Clear Storage

This switch (CLEAR STOR) has four functions, described in Figure 25. As the figure indicates, the desired function is selected by setting the mode switch and the write storage protect bits (WSPB) switch to the appropriate positions. The function thus selected can then be executed by holding down CLEAR STOR while pressing START.

The P-C cycles completely through all core storage addresses during the execution of each clear storage function.

Program Load

The program load switch (PROG LOAD) is used to load the first 1442 card or 1054 tape record into core storage. This first card or tape record must contain instructions that initiate the loading of the remaining cards or tape records. (The P-C must be in run mode for program operation.) It should be noted that a program load operation does not alter the status of the interrupt mask register.

The first card or tape record is read into core storage, beginning at the location specified by the I-register. Normally, RESET is pressed before pressing PROG LOAD. This resets the I-register to /0000. After RESET is pressed, the I-register may be manually altered to some address other than /0000. This allows the first card or tape record to be placed at any location in core storage.

In any case, upon completion of the transfer of the first card or tape record to core storage, the P-C automatically branches to location /0000 to begin instruction execution. Therefore, location /0000 should contain a valid instruction.

Only one input device can be used for initial program load (IPL). The first 1442 on the system is used for IPL. The 1054 is used for IPL when there is no 1442 on the system.

When the 1442 is used for IPL, it operates in packed mode. The first card is read into 40 ascending core storage addresses beginning with the address specified by the I-register. The binary data from two card columns is stored in each core storage location. For example, binary data from card column 1 (rows 12 through 5) is read into core storage location /0000 (bit positions 8 through 15), and binary data from card column 2 (rows 12 through 5) is read into the same core storage location (bit positions 0 through 7). Card rows 6 through 9 are not read into core storage. The remainder of the first card is read in the same manner, entering all odd numbered card columns in bit positions 8 through 15 of their respective core storage locations, and even numbered card columns in bit positions 0 through 7 or their respective core storage locations.

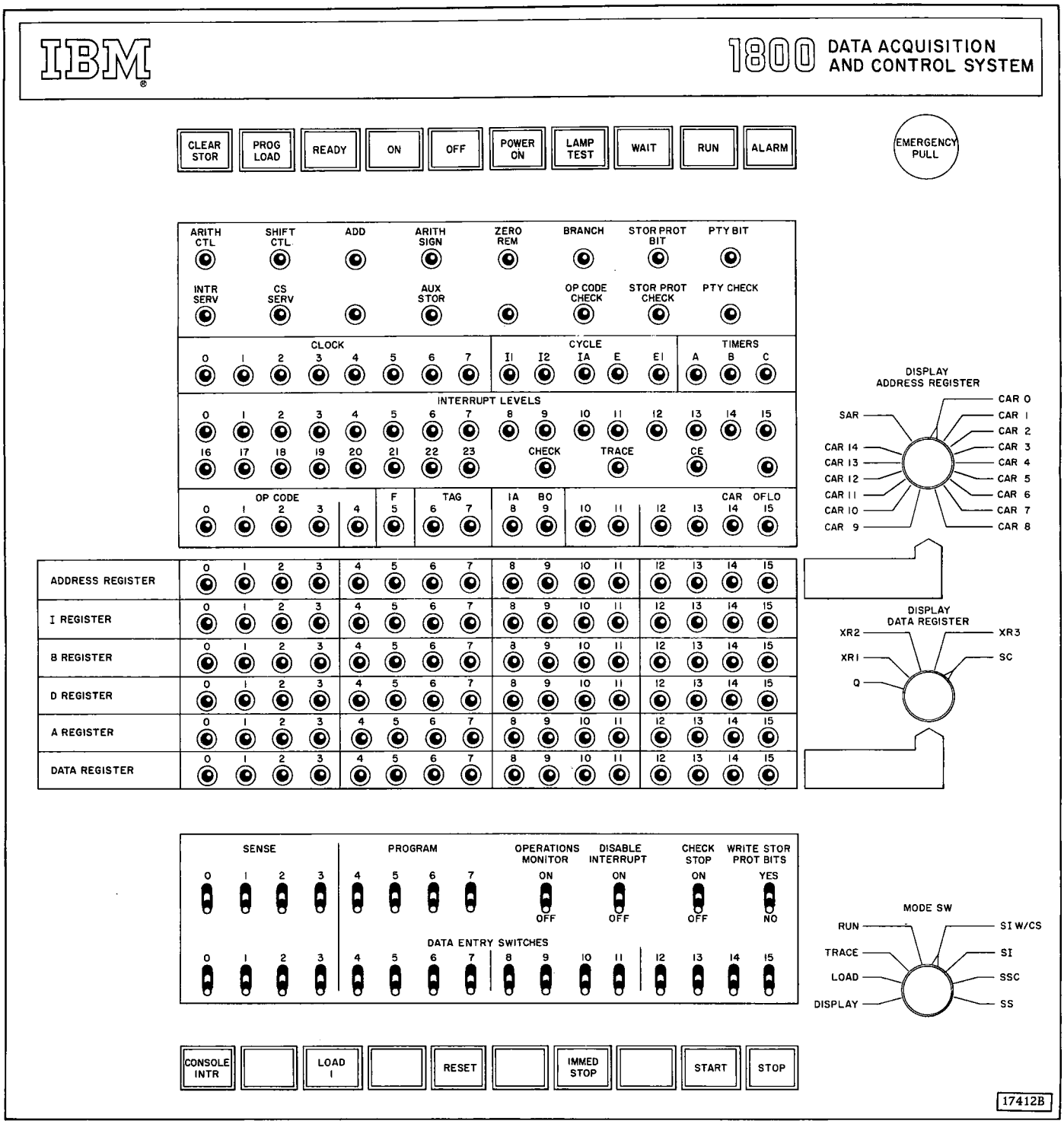


Figure 22. Processor-Controller Console

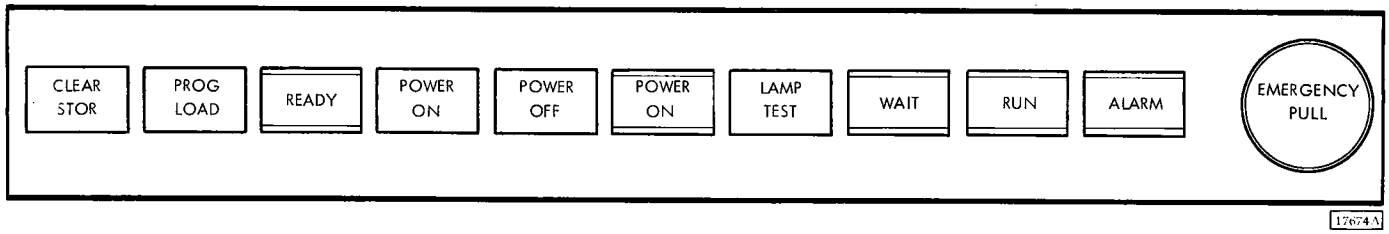


Figure 23. Console Pushbutton Switches and Lights, Top Row

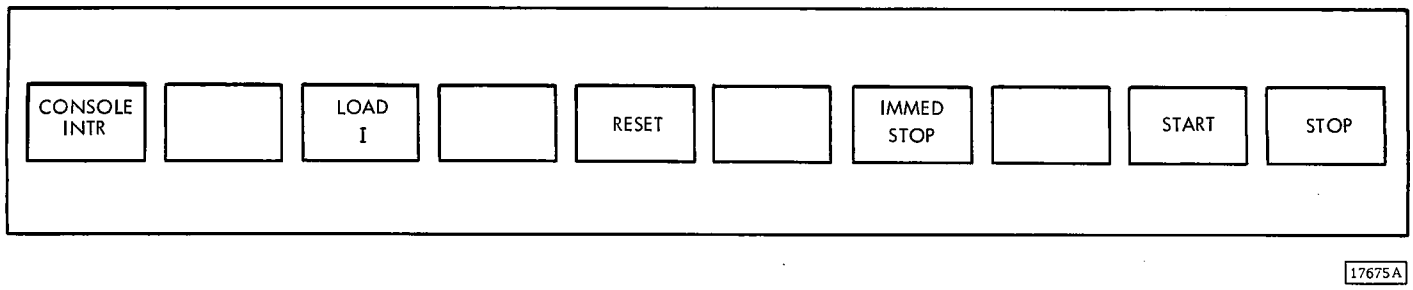


Figure 24. Console Pushbutton Switches and Lights, Bottom Row

Function	Mode Switch	WSPB Switch
1. Store contents of data entry switches in all core storage locations. Storage-protect bits are removed and parity is corrected as required because of bit removal. If all data entry switches are off, only parity bits are left in storage.	Run	Yes
2. Store contents of data entry switches in each core storage location that is unprotected. Locations having protect bits are unchanged.	Run	No
3. Clear storage protect bits. All other data remains unchanged. Parity is automatically corrected in each word in storage.	Display	Yes
4. Search for parity errors. The P-C cycles through storage until stopped by the stop key or a parity error. The check stop switch must be on for a parity error to cause a stop.	Display	No

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Figure 25. Clear Storage Functions

When the 1054 is used for IPL, tape data is loaded into core storage beginning with the address specified by the I-register. The binary data from four tape characters is stored in each core storage location. For example, binary data from the first tape character (channels 1 through 4) is stored in core storage location /0000 (bit positions 0 through 3), ..., binary data from the fourth tape character (channels 1 through 4) is stored in core storage location /0000 (bit positions 12 through 15). Channels 5 through 8 are not loaded into core storage during IPL. This operation continues (loading four tape characters per word) until any channel 5 punch, except within a delete character, is sensed. The channel 5 punch is the end-of-record character and is not read into core storage. Delete characters (punches in channels 1 through 7) are not read into core storage in IPL mode.

Interrupt requests from the 1054 are suppressed while in IPL mode.

Ready

This light is on when the P-C is in an operative condition.

Power On

This switch is used to turn on the power supplies within the P-C.

Power Off

This switch is used to turn off the power supplies within the P-C.

Power On

This light is used to indicate that the P-C power supplies are operative.

Lamp Test

This switch is pressed to apply lamp voltage to all console lamps. Its purpose is to verify operation of all console lamps.

Wait

This light is used to indicate that the P-C is in load or display mode, has been halted by a wait instruction, or has been halted by the operator pushing STOP or IMMED STOP.

Run

This light is used to indicate that the P-C is operating under program control.

Alarm

This light is used to indicate that the operations monitor has timed out. The customer may install an audible alarm to operate in conjunction with the alarm light. See "Operations Monitor" section.

Emergency Pull Switch

This pull switch is for emergency use only. If it is pulled out, all electrical power within the 1801/1802 is turned off, including power to the blowers that cool the electronic circuitry. Turning the blowers off in this manner may damage some of the circuitry. This switch must be reset by a customer engineer.

Console Interrupt

This switch (CONSOLE INTR) enables the operator to interrupt P-C operation. The console interrupt level is assigned by the customer. The program toggle switches may be used in conjunction with console interrupt to specify the console interrupt routine. However, this relationship between the program switches and console interrupt exists only by virtue of the program. There is no internal relationship between the two.

Load I

This switch is used with the mode switch in the load position to transfer the contents of the data entry toggle switches to the I-register. The P-C is in the stopped condition when it terminates the load I operation.

Reset

This switch is used to reset all basic timing, controls, registers (except index registers and address registers), and I/O devices. The interrupt mask register is reset with all bits on. The digital input and digital-analog output registers are not reset. The reset switch is effective only when the P-C is not in a run state, as indicated by the run light being off.

Immediate Stop

This switch (IMMED STOP) stops the P-C at the end of the core storage cycle in operation when the switch contacts close.

All basic timing, controls, registers (except index registers and address registers), and I/O devices are reset. IMMED STOP can also be used to stop data channel (cycle stealing) operations that are no longer under program control.

Start

If the ready light is on, this switch initiates P-C operations, as specified by the mode switch.

Stop

This switch stops the P-C at the end of the instruction in operation when the stop switch contacts close. The P-C registers and I/O devices are not reset. Data channel operations can be stopped only by pressing the immediate stop switch.

If an interrupt that can force a BSI (by being on an unmasked level higher than any in progress) occurs at the same time STOP is pressed, STOP must be pressed again to be effective. Pressing START causes the program to resume operation.

MODE SWITCH

This eight-position rotary switch (Figure 26) is used in conjunction with START to extend operator control of the P-C. The effects of the eight settings of this switch are described next.

SINGLE INSTRUCTION WITH CYCLE STEAL (SI W/CS): Pressing START with the mode switch on SI W/CS causes the execution of one instruction. Data channel operations can occur during execution of the instruction.

SINGLE INSTRUCTION (SI): Pressing START with the mode switch on SI causes the execution of one instruction. Data channel operations are prevented.

SINGLE STORAGE CYCLE (SSC): Pressing START with the mode switch on SSC causes one storage cycle. Single storage cycle operations (usually called single cycle operations) can be used in conjunction with the console cycle lights to step through instructions and analyze P-C operation.

SINGLE STEP (SS): Pressing START with the mode switch on SS causes one basic P-C clock cycle. The advance of the P-C clock is shown by the cycle lights. The clock should always be stepped to T7 before returning the mode switch to RUN.

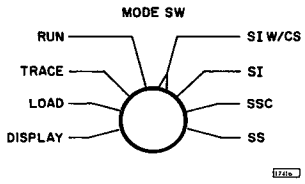

Figure 26. Console Mode Switch

RUN: Pressing START with the mode switch on RUN initiates normal program operation of the P-C.

TRACE: This position of the mode switch causes a trace interrupt after the execution of each instruction. The trace interrupt is a unique interrupt. It has no device status word, no interrupt level status word, and cannot be masked. The trace interrupt is the lowest priority customer interrupt. Once initiated, it is delayed by the occurrence of any other interrupt. It cannot occur while other interrupts are being serviced. When the trace interrupt occurs, the P-C executes the forced BSI and branches to the routine whose address is stored at /0009. (See "Interrupt.")

LOAD: Pressing START with the mode switch on LOAD causes the contents of the data entry switches to be stored at the address specified by the I-register. (The P-C must be in a stopped condition.) The I-register is incremented following each load operation caused by pressing START.

Pressing LOAD I with the mode switch on LOAD causes the contents of the data entry switches to be stored in the I-register of the P-C.

DISPLAY: Pressing START with the mode switch on DISPLAY causes the data at the I-register address to be displayed in the console B-register lights. The I-register is incremented after each display. Successive words are displayed with successive depressions of START.

TOGGLE SWITCHES

Console toggle switches are shown in Figure 27 and described in the following paragraphs.

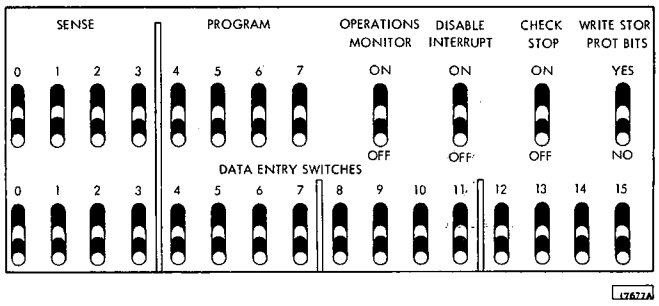

Figure 27. Console Toggle Switches

Sense and Program

The contents of these eight switches may be stored in bit positions 0 through 7 of the accumulator or a core storage location. An XIO with a function of read stores the contents of the sense and program switches at the core storage address specified by the IOCC. A function of sense device stores the switch data in the accumulator.

Operations Monitor

This switch is used to start the operations monitor. The off position disables the monitor.

Disable Interrupt

This switch is used to mask all interrupt levels, including internal. It is especially useful during program analysis when the operator wants to choose the time at which the program may be interrupted. The highest level interrupt on and unmasked is serviced when the switch is turned off.

The following switch limitations should be observed:

1. The switch should never be operated when the P-C is running; the switch should be turned on before an interrupt occurs.
2. The switch must not be turned on while doing a single memory cycle or single step operation of a forced BSI.
3. The switch must be off for proper execution of BOSC.

Check Stop

This switch, when on, causes the P-C to stop when an invalid operation code is detected, a parity error occurs, or a storage protect violation occurs. (These errors cause an internal interrupt if the check stop switch is off.) The stop occurs at the end of the core storage cycle in which the error is detected. The appropriate error light will be on. START must be pressed to continue operation of the next sequential instruction. No internal interrupt will occur.

It should be noted that although a channel address register check causes an internal interrupt, the interrupt does not stop the P-C, regardless of the position of the check stop switch.

Write Storage Protect Bits

This switch enables the writing or clearing of storage protect bits. (See "Store Status" instruction and "Clear Storage Functions," Figure 25.) A parity error may occur if the position of this switch is changed while the P-C is running.

Data Entry Switches

The contents of these 16 toggle switches can be stored by either manual or program control. See "Console Programming" for program control. The description of the load position under "Mode Switch" decribes manual control.

STATUS LIGHTS

These lights (Figure 28) show the status of various P-C functions and operations.

Arithmetic Control

This light (ARITH CTL) is on during arithmetic operations.

Shift Control

This light (SHIFT CTL) is on during shift operations.

Add

This light is on during add operations.

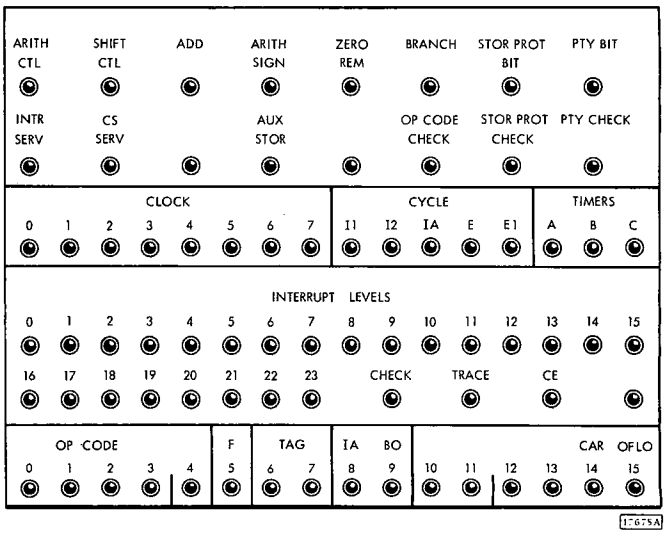

Figure 28. Console Status Indicators

Arithmetic Sign

This light (ARITH SIGN) is on when bit position 0 of the accumulator does not initially equal bit position 0 of the B-register.

Zero Remainder

This light (ZERO REM) is on when the accumulator contains a zero balance during a divide instruction.

Branch

This light is on during branch instructions.

Storage Protect Bit

This light (STOR PROT BIT) is on when the storage protect bit is on in a word transferred between the B-register and core storage.

Parity Bit

This light (PTY BIT) is on when the parity bit is on in a word transferred between the B-register and core storage.

Interrupt Service

This light (INTR SERV) is turned on when an interrupt-forced BSI instruction is being executed for the highest priority interrupt level that is on and not masked.

Cycle Steal Service

This light (SC SERV) is on during cycle steal operations for the highest priority data channel requiring service.

Auxiliary Storage

This light (AUX STOR) is on when CE storage (used for customer engineer programs and error logs) is being accessed.

When the system is executing instructions that access CE storage from main storage, the AUX STOR light turns on at T7 of the cycle preceding the execute cycle and turns off at the last T7 of the operation. When the system is running in a single storage cycle mode, the light will be on at the end of I2, or at the end of IA with indirect addressing, thus indicating that the next cycle will access CE storage. At the end of E-cycle, the light will be off, but the M-register will display the CE storage address.

Operation Code Check

This light is on when an invalid operation Op code is placed in the Op register. The Op code check light is turned off and the check light is turned on (internal interrupt) at the end of the cycle in which the error is detected. This allows the Op code check light to indicate any subsequent error.

Note that an Op code check causes an internal interrupt if the disable interrupt and check stop switches are off, or a check stop if the check stop switch is on.

Storage Protect Check

This light (STOR PROT CHECK) is turned on when an attempt is made to write in a read-only core storage location. The storage protect check light is turned off and the check light is turned on (internal interrupt) at the end of the cycle in which the error is detected. This allows the storage protect check light to indicate any subsequent error.

Note that a storage protect check causes an internal interrupt if the disable interrupt and check stop switches are off, or a check stop if the check stop switch is on.

Parity Check

This light (PTY CHECK) is turned on when a parity error (even number of bits on) is detected in the 18-bit word transfer between the B-register and core storage. The parity check light is turned off and the check light turned on (internal interrupt) at the end of the cycle in which the error is detected. This allows the parity check light to indicate any subsequent error.

Clock

These eight lights (0 through 7) show the advance of the basic P-C clock each time START is pressed and the mode switch is on SS (single stop). Normally, pressing START eight times with the mode switch on SS is equivalent to pressing START once with the mode switch on SSC (single storage cycle).

Cycle

These five indicators (I1, I2, IA, E, and E1) show the progress of an instruction that is being executed in single steps or single storage cycles; that is advanced by repeatedly pressing START with the mode switch on SSC or SS.

- I1 shows that a new instruction is being set up for execution. It is turned on at the beginning of all single word instructions and for the first word of all double word instructions.
- I2 shows that the second word of a double word instruction is being set up for execution.
- IA shows that the instruction being set up is a double word instruction that has an indirect address. The light is on while the indirectly addressed word is being read out of storage.
- E shows that the instruction set up during I-time has been defined by the Op code and is now being executed.
- E1 is turned on with the E light. Its on condition shows that instruction execution control circuitry has progressed to the E1 cycle point. E1 is turned off at the next clock 0 time. Instruction can then progress through E2 and E3 time. (There are no E2 and E3 console lights.)

Timers

These three lights (A, B, and C) show the status of their respective interval timers. An on condition indicates that the timer is in operation.

Interrupt Levels

An interrupt level light is on for each interrupt level requesting service or being serviced. Once on, an interrupt level light can be reset by either of two instructions:

1. A mask instruction that is executed before servicing of the interrupt begins. (The interrupt request is not lost but merely detained until the interrupt level is unmasked, at which time the light is turned back on.)
2. A branch out of interrupt (BOSC) is executed to complete servicing of the interrupt.

The last three interrupt level lights--customer engineer, trace, and check (internal interrupt)--cannot be masked. The CE interrupt can be initiated only from the CE panel or from a device operating in CE mode.

Operation Code

These five lights (0 through 4) display the Op code of each instruction.

Format (F)

This light is on when a two-word instruction is specified.

Tag

These two lights identify the index register or instruction register used in modification of the instruction address. The on condition of the indicators is shown by a 1.

Indicators 6	7	Register
0	0	I-Reg
0	1	XR-1
1	0	XR-2
1	1	XR-3

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Indirect Addressing

This light (IA) is on when the instruction contains this bit (bit 8), which usually indicates indirect addressing.

Branch Out

This light (BO) is on when there is a bit in position 9 of an instruction. When on in a BSC instruction, a branch out of interrupt (BOSC) is specified.

Carry and Overflow

These two lights are turned on individually when their respective conditions occur in the accumulator (A-register).

DATA FLOW DISPLAYS

Six rows of lights and two rotary switches (Figure 29) facilitate the display of data flow in the P-C.

Address Register

These 16 lights display the data in the storage address register (SAR) or the selected channel address register (CAR), depending on the position of the display address register switch. The selected register is displayed each time the P-C comes to a stop or wait condition. (The clock will be at 7.)

Display Address Register Switch

The 16-position rotary switch is used to select a CAR or SAR for display in the address register.

Permanent Register Displays: I, B, D, and A

The contents of these four registers are always displayed.

Data Register

These 16 lights display the contents of the Q-register, which is the A-register extension, the index register (XR1, XR2, or XR3), or the shift counter (SC), depending on the position of the display data register switch. The selected register is displayed each time the P-C comes to a stop or wait condition. (The clock will be at 7.)

Display Data Register Switch

This five-position rotary switch is used to select the Q-register, an index register, or the shift counter for display in the data register.

DISPLAY PROCEDURES

The following procedure may be used to display core storage data between the execution of single instructions:

1. With P-C in stop condition, position mode switch to SI (single instruction).
2. Press START successively to get program to desired point for data display.
3. Record address in I-register. (Because I-register is used in display mode, this recorded address is needed to return P-C to next instruction.)
4. Set address of core storage word to be displayed into data entry switches.
5. Position mode switch to LOAD.
6. Press LOAD I.

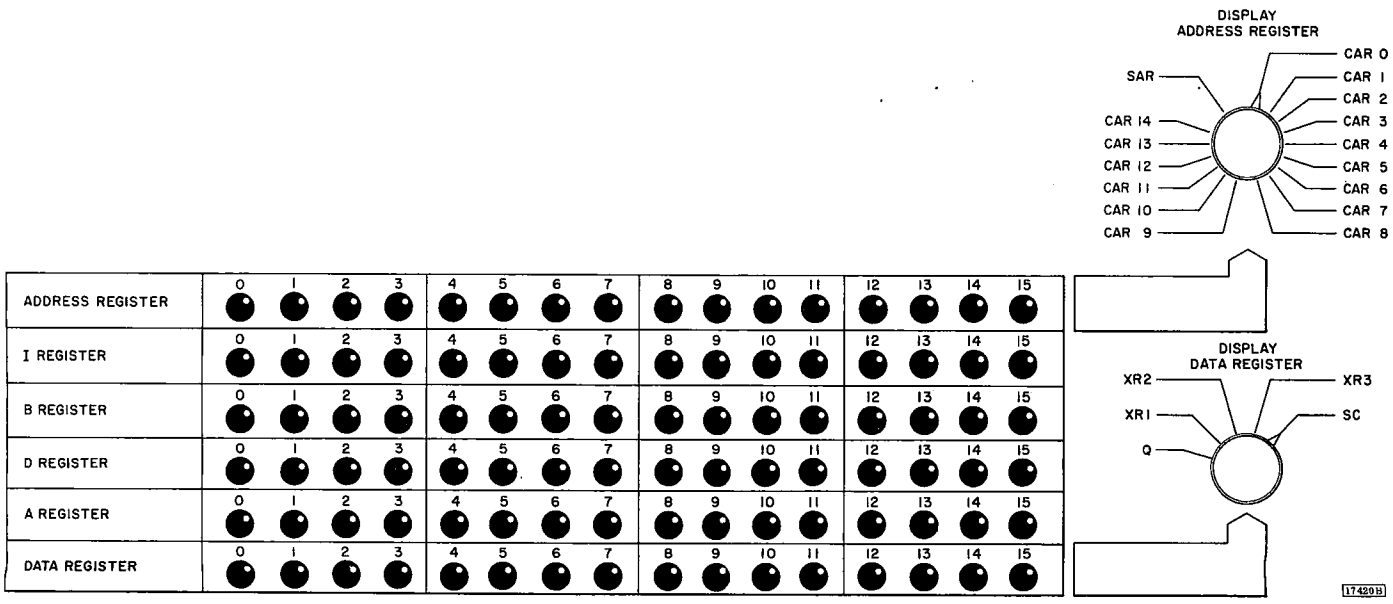


Figure 29. Console Data Flow Displays

7. Position mode switch to DISPLAY.
8. Press START. Selected word is now displayed in B-register indicators.
9. To display other core storage words, repeat steps 4 through 8.
10. To continue program:
    a. Set data entry switches to address recorded in step 3.
    b. Position mode switch to LOAD.
    c. Press LOAD I.
    d. Position mode switch to RUN.
    e. Press START.

To display core storage data between single core storage cycle operations:

1. With the P-C in a stop condition, position mode switch to SSC (single storage cycle).
2. Press START repeatedly until desired cycle in execution of instruction is reached.
3. Perform steps 3 through 10 of preceding single instruction execution procedure.

CONSOLE PROGRAMMING

Various features considered to be internal to the P-C can be programmed using the execute I/O (XIO) instruction. The input/output control command (IOCC) referenced by the XIO must have an area code of 00000, and modifier bits 8 through 10 must specify the particular feature as shown in the following illustration.

Feature/Register	Bits 8-10
Interval Timers	001
Console Data Entry Switches	010
Console Sense, Program Select, and CE Switches	011
Interrupt Mask Register	100
Programmed Interrupt	101
Console Interrupt	110
Operations Monitor	111

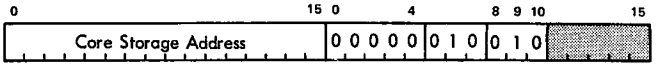
17398 A

These addresses are fixed for all 1800 systems.

Programming for the interval timers and operations monitor is described in their respective sections of this manual. Programming for the interrupt mask register and programmed interrupts is described in the "Interrupt" section of this manual. Programming for the remaining features is described in the following paragraphs.

Console IOCC's

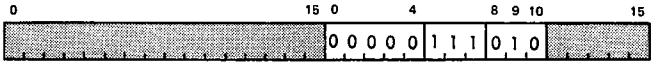
Read -- Data Entry Switches



17401 B

This command causes the status of the data entry switches to be read into the core storage location specified by the address word.

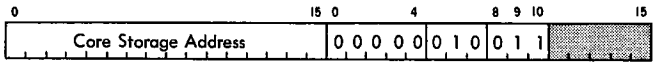
Sense Device -- Data Entry Switches



17400 A

This command causes the status of the data entry switches to be read into the accumulator.

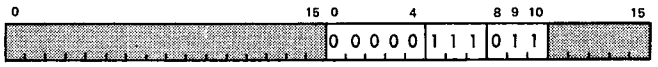
Read -- CE, Sense, and Program Switches



17403C

This command causes the status of the CE switches to be read into bit positions 8 through 15 and the status of the sense and program switches to be read into bit positions 0 through 7 of the core storage location specified by the address word.

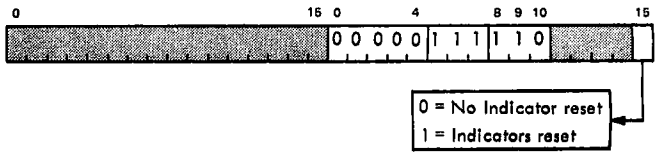
Sense Device -- CE, Sense, and Program Switches



17402 B

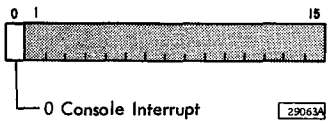
This command causes the status of the CE switches to read into bit positions 8 through 15 and the status of the sense and program switches to be read into bit positions 0 through 7 of the accumulator (A-register).

Sense Device -- Console Interrupt



17404 B

This command causes the console interrupt device status word (DSW) to be loaded into the accumulator. The DSW is shown in the following illustration.



Program Failure -- Restart

Program restart points should be written into programs to allow recovery or complete restart of the system. The programmer writing this recovery procedure must consider the nature of the process and the operational philosophy of the customer.

Industry, science, research, government -- all are faced with the need for collecting increasing amounts of data within decreasing time scales. Physical measurements must be monitored and quantified with greater speed and accuracy than ever before. The collection of analog data and its conversion for presentation to the digital processor-controller (P-C) are the functions of the analog input features.

A physical phenomenon is first sensed and converted to an analog electrical signal by sensors or transducers, such as thermocouples or strain gages. Electrical signals from sensors or transducers may be in the millivolt, volt, or milliampere range. Low voltage signals (less than 1 volt) are amplified to a level acceptable for conversion to digital form. All customer lines from transducers are terminated at the control system on screw-down terminals. The signals are also conditioned at the terminals, including the filtering of extraneous signals, known as noise.

Conversion of analog signals from a voltage level to digital information is accomplished by an analog-to-digital converter (ADC). Such converters are complex enough to permit analog signals from multiple sources to be converted by sharing one ADC. The necessary switching is accomplished by a multiplexer.

The data path from sensor or transducer to the P-C is shown in Figure 30.

ANALOG INPUT UNITS AND FEATURES

The analog input units and features provide modular packaged equipment used to convert voltage or current signals to digital values. The modules used to accomplish the conversions include analog-to-digital converters, multiplexers, amplifiers, and other signal conditioning equipment.

The units and features that accomplish the analog input function are briefly introduced below, followed by more detailed descriptions. A description of the operation of analog input and its relation to the P-C is given later in the "Programmed Control Modes" section.

As shown in Figure 31, input signals are routed through termination, signal conditioning elements, multiplexer switches, an amplifier (low level signals only), and into the ADC. The output of the ADC is presented to the P-C via data channel or direct program control operations.

1851 MULTIPLEXER TERMINAL, MODEL 1: This is a modular chassis that is mounted in an 1828 Enclosure. It provides up to 64 analog input multiplexer points (two-wire), with signal conditioning elements for each point. The chassis houses either solid state multiplexers or relay multiplexers. When relay multiplexers are installed, up to two differential amplifiers can be mounted in each terminal.

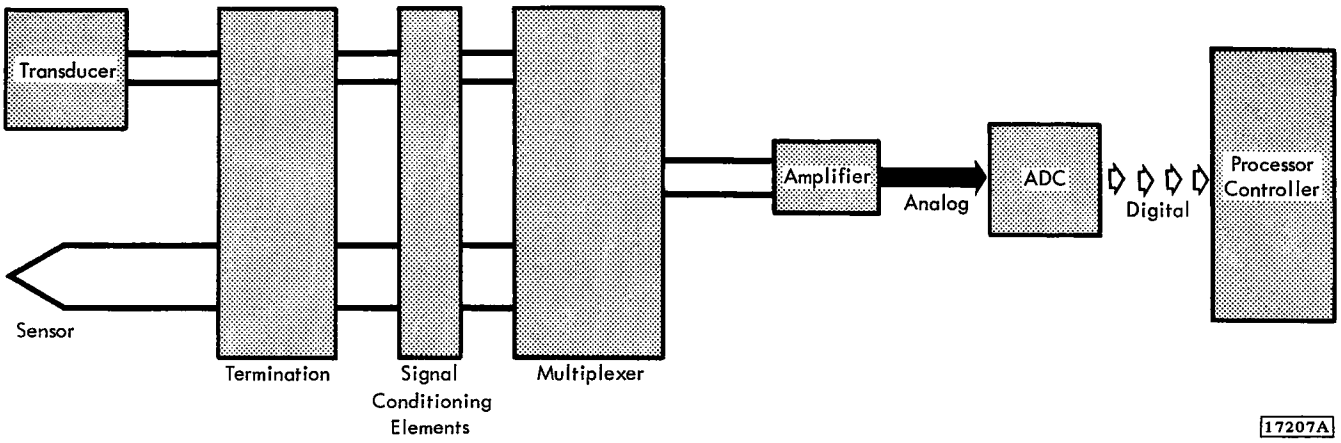


Figure 30. Analog Input Data Path

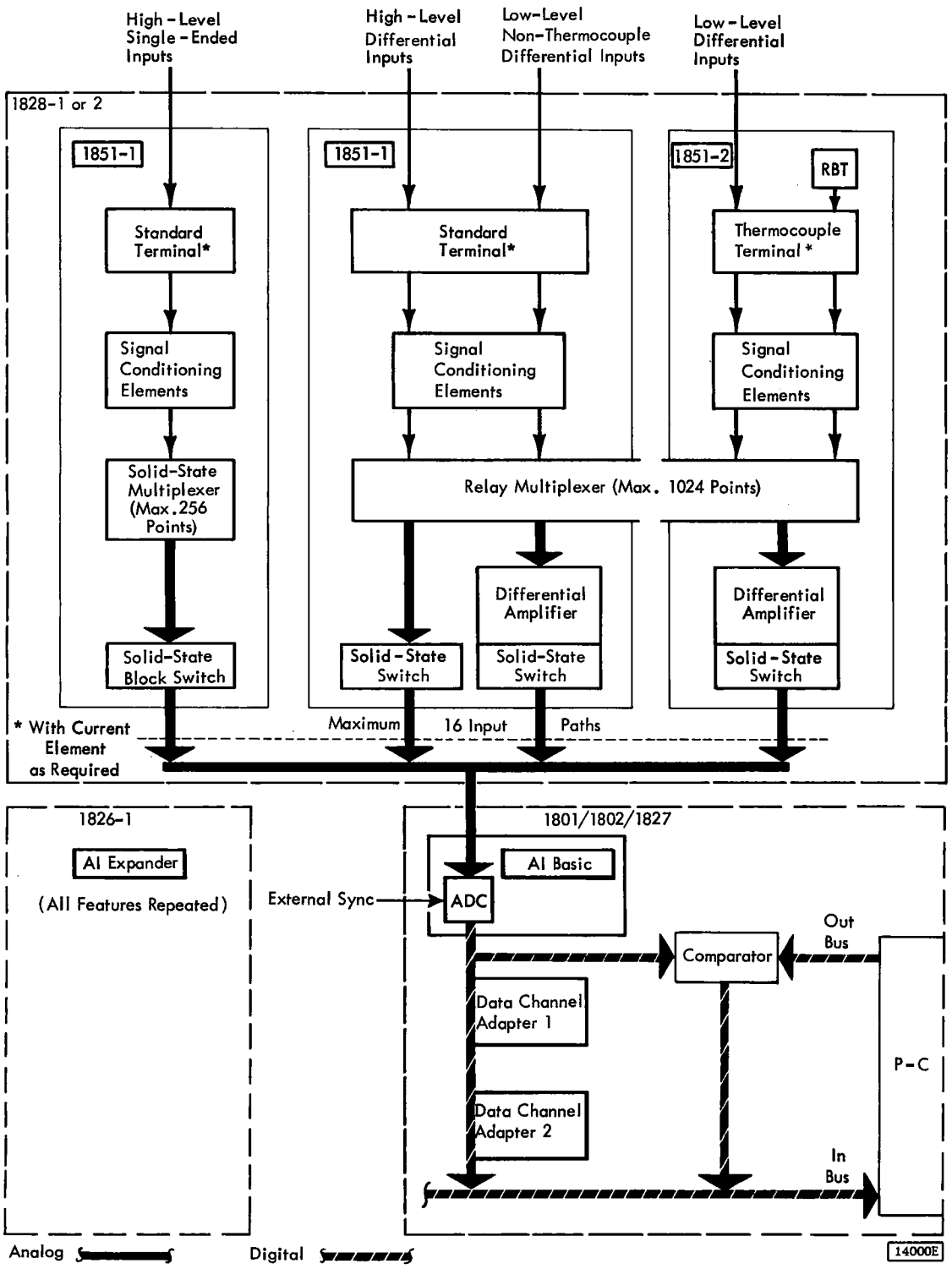


Figure 31. Analog Input Configuration

1851 MULTIPLEXER TERMINAL, MODEL 2: This terminal is similar to the model 1. However, a maximum of 62 multiplexer points is allowed, and a cold junction is provided for direct connection of thermocouples. A cold-junction temperature indicator device (resistance bulb thermometer) is included in the terminal.

MULTIPLEXER (RELAY): This multiplexer (Mpx/R) provides switching for both high-level differential inputs and low-level differential inputs, allowing all Mpx/R inputs to use a common ADC.

MULTIPLEXER (SOLID STATE): This multiplexer (Mpx/S) is a solid state, high-level single-ended multiplexer. Mps/S provides high-speed switching of analog input signals to allow use of a common ADC.

MULTIPLEXER OVERLAP: This feature allows overlap of solid state and relay multiplexing.

MPX /R CONTROL AND MPX/R CONTROL ADDITIONAL: These features provide the control circuitry necessary to operate the Mpx/R points. Each feature can control up to 256 points.

MPX/S CONTROL: Control circuitry to operate the Mpx/S points is provided by this feature.

DIFFERENTIAL AMPLIFIER: This is a time-shared amplifier which raises each low level signal to the ±5 volt level of the ADC. Up to 256 Mpx/R points can use the same amplifier. The differential amplifier may be assigned one of the following ranges: ±10 mV, ±20 mV, ±50 mV, ±100 mV, ±200 mV, or ±500 mV.

ADC MOD 1: This ADC converts analog signals (±5 volt range) to digital values (8, 11, or 14 bits plus sign).

ADC MOD 2: This ADC is similar to ADC Mod 1 but includes a sample-and-hold amplifier for increased conversion rates.

AI DATA CHANNEL ADAPTER 1: This adapter allows sequential reading of input points by means of data channel (cycle steal) operations with one XIO initialize read.

AI DATA CHANNEL ADAPTER 2: This adapter, in conjunction with adapter 1, allows random reading of input points via data channel (cycle steal) operations with one XIO initialize read and one XIO initialize write.

COMPARATOR: The comparator performs range checking on digital values developed by the ADC. The high and low limits are selectively obtained from the processor-controller for checking. When these values are determined to be out of limit, an interrupt informs the P-C. Only one P-C cycle is required for each value to be limit checked.

ANALOG INPUT EXPANDER: Allows a complete analog input system to be configured around the 1826 Data Adapter Unit. Thus, a second ADC or simply a remotely located ADC may be added to any 1800 system.

MULTIPLEXER/R AND MULTIPLEXER/S MAXIMUMS AND RANGES: Althrough the maximum number of Mpx/R points and Mpx/S points is 1,024 and 256, respectively, both maximums cannot be installed within the same system. The simultaneous maximums for each system are dependent upon the number of analog input ranges as shown in Figure 32.

IBM 1851 MULTIPLEXER TERMINAL

The 1851 Multiplexer Terminal is a modular chassis in which multiplexing and signal conditioning features can be mounted. The 1851 terminals are mounted in an 1828 Enclosure. Up to 19 terminals can be included for any one ADC in a system. Mpx/R and Mpx/S cannot be installed in the same 1851 terminal unit.

Two models of the multiplexer terminal are available. The model 1 provides facilities for up to 64 multiplexer points in groups of 16 points. Customer wires are terminated on screw-down terminals. The signal matching elements are available for each multiplexer terminal. Up to two differential amplifiers can also be mounted in each terminal.

The model 2 is modified to allow for thermocouple termination, cold junction thermal stabilization, and a resistance bulb thermometer (RBT) circuit. These elements are used to determine cold-junction temperature. Thus, thermocouple wires can be connected directly to the terminals, and the cold-junction temperature can be computed by the P-C.

The first two multiplexer addresses installed in a model 2 are used for the cold-junction signal measurement: 00 is RBT reference; 01 is RBT bridge output. These two signals should be read at intervals which are small compared with significant ambient temperature change intervals. Separate readings are required for each model 2.

Since the first two addresses are used for the cold junction, a maximum of 62 input points are

Number of Mpx/S Groups *	Mpx/R Points (Maximum) *	Number of Differential Amplifiers (Maximum)	Number of Low Level Ranges (Maximum)
0	256 HL +768 LL No HL +1024 LL	15 16	6 6
1	256 HL +768 LL No HL +1024 LL	14 15	6 6
2	256 HL +768 LL No HL +1024 LL	13 14	6 6
3	256 HL + 768 LL No HL +1024 LL	12 13	6 6
4	256 HL +768 LL No HL +1024 LL	11 12	6 6
5	256 HL +768 LL No HL +1024 LL	10 11	6 6
6	256 HL +768 LL No HL +1024 LL	9 10	6 6
7	256 HL +768 LL No HL +1024 LL	8 9	6 6
8	256 HL +768 LL No HL +1024 LL	7 8	6 6
9	256 HL +768 LL No HL +1024 LL	6 7	6 6
10	256 HL +768 LL No HL +1024 LL	5 6	5 6
11	256 HL +768 LL No HL +1024 LL	4 5	4 5
12	256 HL +768 LL No HL +1024 LL	3 4	3 4
13	256 HL +512 LL No HL +768 LL	2 3	2 3
14	256 HL +256 LL No HL +512 LL	1 2	1 2
15	256 HL + No LL No HL +256 LL	0 1	0 1
16	No HL + No LL	0	0

* Multiplexer/R input ranges are ± 10, ± 20, ± 50, ± 100, ± 200, and ± 500 millivolts for input to a differential amplifier, and -0.5 to +5.0 volts for direct input to the ADC. The only Multiplexer/S input range is ± 5.0 volts for direct input to the ADC. 17442B

Figure 32. Multiplexer Maximum Points and Ranges

available in a model 2 for external source signals. The first Mpx/R group has only 14 input points available for external source signals. The range for this group must be ±10, ±20, or ±50 millivolts.

All other functions of the model 2 are the same as those of model 1. Thus, nonthermocouple signals may be terminated in the model 2 if required by the system configuration.

MULTIPLEXER/R

The multiplexer/R (Mpx/R) feature provides for relay multiplexing of high or low level analog inputs at a maximum rate of 100 points per second. Input points are provided in groups of 16 each. Up to 16 groups can be combined to form the input to one differential amplifier, thus providing as many as 256 input points per amplifier.

Each amplifier has a fixed range. The full scale input range for any group of Mpx/R points depends on the range of the amplifier to which it is connected. Ranges available are: ±10 mV, ±20 mV, ±50 mV, ±100 mV, ±200 mV, and ±500 mV. High level inputs (-0.5 to +5.0 volts) do not require an amplifier.

The Mpx/R can operate with a maximum of 200 volts common mode (dc or peak-to-peak ac).

MULTIPLEXER/S

The multiplexer/S (Mpx/S) feature provides for solid-state multiplexing of high-level, single-ended (HLSE) analog inputs. Mpx/S is capable of multiplexing at rates higher than those attained with Mpx/R. The actual multiplexing rate is dependent upon the source amplifier, ADC, programming methods, etc. used in any particular system. Mpx/S points are mounted in the 1851 Multiplexer Terminal, Model 1, in groups of 16 points each and cannot be intermixed with Mpx/R points within a terminal. Mpx/S input voltage range is ±5 volts full scale.

Multiplexer Overlap

Several methods of overlapping Mpx/R and Mpx/S operations are possible.

Overlap Without Special Feature

In overlap operation, having a relay point selected inhibits solid-state operation from changing the ADC resolution. The resolution can be changed after the relay conversion is complete. It can also be changed if the solid-state operation is initiated during the 'relay end delay' period. Without the overlap special feature, overlapping can be accomplished by two methods:

1. Using direct program control mode of operation, the selection of a point in the relay multiplexer may be started. Then, while the relay point is being selected, a series of solid state point conversions may be performed.

   When relay multiplexing is complete, it obtains use of the ADC for conversion of the relay point. When conversion of the signal at the point is complete and the resultant data in the ADC register is available, an interrupt is

activated. Solid state and relay point interrupts are differentiated by programmed interrogation of the analog input device status word (DSW).

An interrupt resulting from completion of an input point conversion (either relay or solid state point) suspends selection of another point until the converted value has been read into core storage.

2. If a discrete conversion of a relay point is started under direct program control, a sequence of conversions of solid state points can be started using data channels. When relay multiplexing is complete, the multiplexer obtains use of the ADC for conversion of the relay point. When the resultant converted data is available in the ADC register, an interrupt is activated. This is the "direct program control conversion complete" interrupt utilized for discrete conversions under direct program control. If solid state conversions have not been completed when the relay multiplexer control captures the ADC, solid state conversions are continued as soon as the ADC register has been cleared. No further discrete conversions may be started until the solid state conversions are complete.

Overlap With Special Feature

With the multiplexer overlap special feature, another means of overlapping operations is possible. Under two-data-channel operation, relay addresses can be interleaved with solid state multiplexer addresses in the same address table. Both relay and solid state addresses are transferred to their respective controls by means of data channel operations. However, data from Mpx/R points is transferred to core storage under direct program control, whereas data from Mpx/S points is transferred by data channel operations.

When a relay address is received, it is latched by the Mpx/R control; then another data channel cycle is requested to obtain the next solid state multiplexer address from core storage. Random conversions of solid state multiplexer points proceed asynchronously by means of data channel operations until the relay multiplexer point is ready for conversion. When this occurs, the relay multiplexer takes control. The next point converted by the ADC is the relay point; an interrupt allows the P-C to transfer this value to core storage by means of an XIO read. The XIO read specifies the location at which the converted relay point data is stored. After the ADC has been read, conversions are continued under data channel control.

If another relay address is recognized before the first relay point has been converted, an interrupt occurs. This interrupt informs the P-C that a relay point was mislocated in the address table. The mislocated relay point will not be converted. A relay point cannot be the last word in a data table when the overlap special feature is used.

Efficient use of overlapping relay and solid state multiplexing depends upon correct placement of addresses in the multiplexer address data table. Enough solid state multiplexer addresses must be included between relay addresses to ensure that sufficient time is allowed for conversion of the first relay point. While one Mpx/R point is being selected, approximately 100 Mpx/S points can be converted with ADC mod 1, and 200 Mpx/S points with ADC mod 2.

SIGNAL CONDITIONING ELEMENTS

Signal conditioning elements listed below provide passive signal conditioning at the terminal for each analog input signal. For specifications and characteristics of each element, see 1800 Installation Manual -- Physical Planning, Order No. GA26-5922.

CURRENT ELEMENT: This element allows 4-20 ma current input signals to be converted into either the 0.1 to 0.5 volt range or the 1 to 5 volt range. Current elements can be installed with Mpx/S or Mpx/R. A current element cannot be used with a voltage element.

FILTER ELEMENT (MPX/R ONLY): This element is a low-pass passive filter to reject normal mode ac noise. Filter elements cannot be installed for use with Mpx/S.

VOLTAGE ELEMENT (MPX/S): This element provides 2:1 voltage attenuation. This element allows intermixing of 10 volt and 5 volt signals within the same Mpx/S group.

VOLTAGE ELEMENT (MPX/R): This element provides 2:1 voltage attenuation. For example, this allows intermixing of 100 millivolt signals and 50 millivolt signals in the same Mpx/R group. Voltage elements for Mpx/R provide the filtering function described for the filter element. A filter element cannot be installed on points with a voltage element.

CONNECTOR ELEMENT: This element is wired for straight-through connection with no signal conditioning.

CUSTOM ELEMENT: This element is available for customer mounting of special conditioning circuits to meet a particular requirement.

DIFFERENTIAL AMPLIFIER

This is a time-shared amplifier used in conjunction with the Mpx/R to raise analog signals to the ADC input level of ±5 volts.

Gains available are 500, 250, 100, 50, 25, and 10. These allow input voltage ranges of Mpx/R points to be specified for ±10, ±20, ±50, ±100, ±200 and ±500 millivolts.

A single amplifier can service up to 256 input points (16 blocks of 16 multiplexer relays). Up to two amplifiers can be mounted in one multiplexer terminal. Thus, multiple amplifiers can be used for voltage range changing in place of passive voltage elements.

ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADC provides the ability to convert bipolar analog signals (±5 volt signal range) to digital values. Two models are available: mod 1 and mod 2. Both models have program selectable resolutions of 8, 11, and 14 bits. The actual time required from start to completion of a conversion by either ADC depends on the number of output bits that are to be developed as follows: 8-bit resolution, 29 μs; 11-bit resolution, 36 μs; 14-bit resolution, 44 μs.

The ADC mod 1 and mod 2 differ in that the mod 1 includes a buffer amplifier and the mod 2 includes a sample-and-hold amplifier. When operating with a mod 1, the multiplexer holds the selected input point until conversion is completed. If Mpx/S is used with a mod 1, a 50 μs end delay is encountered after the conversion is completed before another point can be selected. Therefore, an additional 50 μs is required for each conversion with this configuration.

The sample-and-hold amplifier in the mod 2 allows the multiplexer to be released when the amplifier goes to hold mode at the start of the conversion cycle. If Mpx/S is used with a mod 2, no end delay is encountered after a conversion is completed before another point can be selected. This fact permits increased multiplexing and conversion rates. It should be noted that the sample-and-hold amplifier reverses the polarity of the input points. The programmer must consider this in his program.

In operation, conversion rates may vary up to 11,000 per second with an ADC mod 1, or up to 24,000 per second with an ADC mod 2, depending on the system configuration and programming methods used. These rates should not be considered as sustained system conversion rates. They are attainable only with the following system configuration and conditions after an operation has been initialized using a data table.

Configuration:

- 2 μs core storage.
- Data channel adapter 1 if operating in sequential mode.
- Data channel adapters 1 and 2 if operating in random mode.
- Multiplexer/S.

Conditions:

- Eight-bit resolution is used.
- External sync is not used.
- Comparator is not used.
- No other data channel operations are in progress.
- Processor-controller is in wait state during the data table operations.
- Data table chaining does not occur.

Any deviation from the preceding conditions results in reduced conversion rates.

Analog Input Calibration

The analog input calibration facility is housed in the 1828 Enclosure that is abutted to the 1801, 1802, or 1826 containing the analog basic.

Power is supplied to the calibration facility through the power switch on the front left side of the 1828.

The calibration facility provides the following dc reference voltages for calibration of analog input features.

±5 volts.	100 mV.
-5 volts.	50 mV.
500 mV.	20 mV.
200 mV.	10 mV.

Exact voltages are measured at the factory and are recorded (to five significant digits) on the reference unit.

A special high-level input point is selected by multiplexer address/13E8 (which is outside the

normal range of Mpx/S addresses) for ADC calibration only. The multiplexed calibration point can be addressed at any time by the program for an operational check of the ADC. The reference voltage to be addressed is selected by changing connections on a terminal strip. A customer engineer makes these changes.

Data Word

The data word developed in the ADC register is compatible with 1800 word format as shown in Figure 33. The data word allows for a sign plus 14-bit resolution. Program conversion of the value presented by the ADC should assume a position for the binary point. This position does not change when the format (14, 11, or 8 bit) is changed; only the number of significant bits in the ADC converted value changes. Negative numbers are in 2's complement form.

Figure 34 shows examples of maximum and overload positive values and maximum and overload negative values for all three word formats.

Buffer Amplifier

The buffer amplifier is a single-ended operational amplifier that is an integral part of the ADC mod 1.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
14-Bit Format	S	X	X	X	X	X	X	X	X	X	X	X	X	X	X	OL
11-Bit Format	S	X	X	X	X	X	X	X	X	X	X	X	1	0	0	OL
8 Bit Format	S	X	X	X	X	X	X	X	X	1	0	0	0	0	0	OL

NOTES:

1. S is the sign of the data: a 0-bit is positive; a 1-bit is negative.
2. The X's indicate that a 1- or 0-bit may appear to represent the converted value. In 8- and 11-bit formats, the 0's indicate that only a 0 will appear in these positions.
3. OL is overload indicator. If on, an overload condition is indicated; that is, the signal was outside the ±5 volt range. In this case, the other bits in the word should be ignored.
4. The 1-bit in bit position 9 of the 8-bit format and bit position 12 of the 11-bit format are provided for half-adjust of the quantizing error. Half-adjust of 14-bit format quantizing error is accomplished by ADC circuitry.

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Figure 33. ADC Word Format

Positive	Bit Weight (Powers of 2) S	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OL	Decimal Equivalent
14-Bit Maximum	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	+16382
14-Bit Overload	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+16383
11-Bit Maximum	0	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	+16372
11-Bit Overload	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	+16380
8-Bit Maximum	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	+16288
8-Bit Overload	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	+16352
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	Word Bit Position																

Negative	Bit Weight (Powers of 2) S	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OL	Decimal Equivalent
14-Bit Maximum	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	-16383
14-Bit Overload	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	-16384
11-Bit Maximum	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	-16372
11-Bit Overload	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	-16380
8-Bit Maximum	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-16288
8-Bit Overload	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	-16352
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
	Word Bit Position																

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Figure 34. ADC Maximum and Overload Values

The amplifier provides high-input-impedance buffering of the ADC on a time-shared basis for applications not requiring a time-shared sample-and-hold input characteristic.

Sample-and-Hold Amplifier

The sample-and-hold amplifier is a single-ended amplifier capable of providing a short aperture time for sampling high level analog signals and a high accuracy hold function. The sample-and-hold amplifier is an integral part of the ADC mod 2.

If 14-bit resolution is used with an ADC mod 2 which is located within the P-C, the P-C clock is stopped during the last portion of the sample period provided by the sample-and-hold amplifier. This reduces the possibility of noise being induced on the sample by the P-C. The period of time the P-C clock is stopped depends on core storage cycle time as follows:

Core Storage Cycle	Clock Stop Period
2 μs	1-3 μs
2.25 μs	0.75-3.00 μs
4 μs	1-5 μs

The clock stop period does not directly affect the ADC conversion rate. However, when considering overall system throughput, one should realize that each ADC conversion stops the P-C clock for the periods given.

The sample and hold amplifier reverses the polarity of the input points. This fact must be considered in writing the program.

External Sync

The operation of the ADC can be controlled by an external timing (sync) pulse.

When using Mpx/R, a ready signal is sent to the external device after the Mpx/R point has been addressed and the relay has settled. This ready signal indicates that the input point has been sampled and is being held for conversion until the external device signals with a sync pulse. When a sync pulse is received, conversion of the sample begins. The maximum time to hold a sample (ready signal sent to sync pulse received) and still maintain less than 0.01% error is 330 ms.

When using Mpx/S, a ready signal is sent to the external device after an Mpx/S address has been received, but before the point is actually selected and the input sampled. This ready signal indicates that the Mpx/S control is ready to sample the input. When a sync pulse is received, the Mpx/S input point is sampled and conversion begins. The actual conversion is started 10 μs after the sync pulse is received.

Input/output control command (IOCC) modifier bit 8 is used for external sync mode control in an XIO write or XIO initialize read. Modifier bit 8 being on enables external sync mode; modifier bit 8 being off terminates external sync mode.

It should be noted that external sync cannot be used while overlapping operations by means of the multiplexer overlap special feature.

COMPARATOR

The comparator performs selective checking on digital values converted by the ADC. A range-type check is made to confirm that converted values are within specified limits. The limits are obtained from the multiplexer address table in core storage whenever a check is required. (One core storage cycle delay allows both limits to be acquired.) An out-of-limits condition is signaled by an interrupt. Two analog input data channel adapter features are a prerequisite to this feature. The comparator is used only in data channel random mode as described under "Programmed Control Modes".

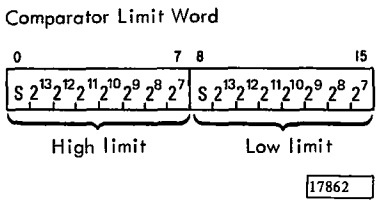
Operational Description

In converting many analog input source signals, it may be necessary to monitor each signal to ensure that the signal remains within specified bounds. Normally, a number of these signals are redundant and other signals need only be checked occasionally. To allow for flexibility of checking input signals, separate control is provided in the multiplexer address word to indicate when checking is to be performed by the comparator.

In order to perform a range comparison, both a high limit and low limit must be set. These limits are obtained from limit word in the multiplexer address table. It should be noted that limit words need not remain static. For example, when a particular high limit is exceeded, a single change will permit recognition of the return of the signal within the former limits. This is accomplished by substituting the high limit for the low limit and setting a new maximum high limit. In this case, the time interval in which the signal was out of limit is known if the interval timer is read after each limit is exceeded.

Limit Words

The high and low limit values are expressed in eight bits each (seven bits plus sign), enabling both the high and low limits to be stored in one 16-bit word. Negative numbers are expressed in 2's complement form. The format of the limit word is:



Limit words are interleaved in the multiplexer address table so that a limit word follows each address entry that is to be checked, as shown in Figure 35.

Comparator Control

Two bit positions (1 and 2) of the multiplexer address word are used to control comparator functions. When

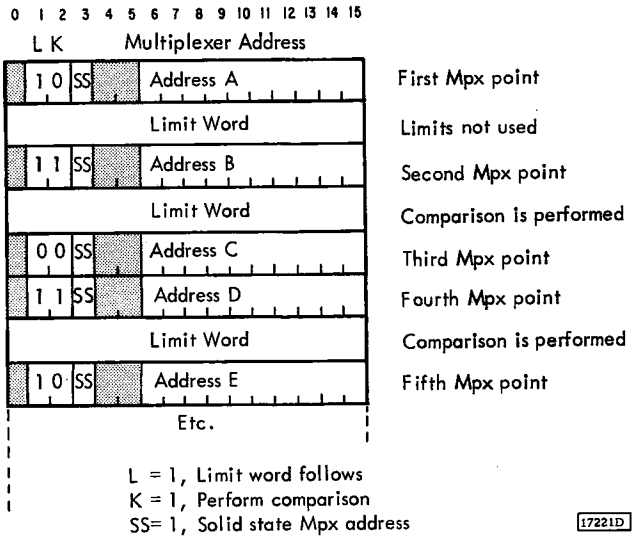


Figure 35. Multiplexer Address Table with Comparator Limit Words

bit position 1 (designated as L) is on, it indicates that the next word in the table is a limit word. When bit position 2 (designated as K) is on it indicates that a comparison is to be performed using the following limit word.

Figure 35 shows a sample multiplexer address table. The word count and scan control bits are obtained from the data table that receives the converted values. The chain address from the receive table is used to provide unique chaining. It should be noted that if the multiplexer overlap special feature is installed, a limit word cannot follow an Mpx/R address.

Comparison Cycle (L=1, K=1)

When the ADC register is filled with the value to be limit checked (seven high-order bits plus sign during conversion), the limit word is acquired from storage and the limit comparison is performed.

Out-of-Limits Conditions

When the comparator determines that an out-of-limits condition exists, the multiplexer point address and the type of condition involved are saved in the comparator. An interrupt unique to the comparator is activated to alert the P-C, and further comparisons are suppressed. The effect of this suppression is identical to that caused by the recognition of a 0 K-bit in the multiplexer address.

Comparison in step with multiplexing is automatically restarted when the comparator device status word (DSW) has been sensed and the interrupt indicator reset by an XIO sense device with reset. The out-of-limit conditions are:

- High out-of-limit, which occurs if the ADC value is equal to or greater than the high limit.
- Low out-of-limit, which occurs if the ADC value is less than the low limit.

ANALOG INPUT EXPANDER

This feature provides two principal advantages:

1. It doubles the capacity of the analog input features.
2. It allows the analog input features to be structured separate from the processor-controller.

The analog input expander is an 1826 Data Adapter Unit feature that provides the basic capability for attaching an ADC, comparator, multiplexer terminals, and so on. This second analog input system attaches to I/O control and data channels in a manner similar to that of the first analog input system. Thus the system conversion rates can be doubled, neglecting I/O interaction.

ANALOG INPUT ADDRESS ASSIGNMENT

There are 1,024 multiplexer addresses available for use with analog input. The first 256 addresses (0-255) are used by both Mpx/S and Mpx/R. Because these 256 addresses have a dual use, bit 3 of each multiplexer address word is used to specify which multiplexer is being addressed (Mpx/S or Mpx/R). When bit 3 is off, Mpx/R is addressed. When bit 3 is on, Mpx/S is addressed.

All Mpx/S groups are installed in the lowest numbered 1851's (1 through 4). Mpx/S is followed by Mpx/R in this sequence:

1. High level.
2. ±10 mV range.
3. ±20 mV range.
4. ±50 mV range.
5. ±100 mV range.
6. ±200 mV range.
7. ±500 mV range.

Addresses for each point within an 1851 are shown in Figure 36 for Mpx/S, Figure 37 for

Numbering within 1851		1851's with Multiplexer/S			
Group Number	Point Number	1st 1851	2nd 1851	3rd 1851	4th 1851
	00	00	64	128	192
	01	01	65	129	193
	02	02	66	130	194
	03	03	67	131	195
	04	04	68	132	196
	05	05	69	133	197
	06	06	70	134	198
0	07	07	71	135	199
	08	08	72	136	200
	09	09	73	137	201
	10	10	74	138	202
	11	11	75	139	203
	12	12	76	140	204
	13	13	77	141	205
	14	14	78	142	206
	15	15	79	143	207
	16	16	80	144	208
	17	17	81	145	209
	18	18	82	146	210
	19	19	83	147	211
	20	20	84	148	212
	21	21	85	149	213
	22	22	86	150	214
	23	23	87	151	215
1	24	24	88	152	216
	25	25	89	153	217
	26	26	90	154	218
	27	27	91	155	219
	28	28	92	156	220
	29	29	93	157	221
	30	30	94	158	222
	31	31	95	159	223
	32	32	96	160	224
	33	33	97	161	225
	34	34	98	162	226
	35	35	99	163	227
	36	36	100	164	228
	37	37	101	165	229
	38	38	102	166	230
2	39	39	103	167	231
	40	40	104	168	232
	41	41	105	169	233
	42	42	106	170	234
	43	43	107	171	235
	44	44	108	172	236
	45	45	109	173	237
	46	46	110	174	238
	47	47	111	175	239
	48	48	112	176	240
	49	49	113	177	241
	50	50	114	178	242
	51	51	115	179	243
	52	52	116	180	244
	53	53	117	181	245
	54	54	118	182	246
3	55	55	119	183	247
	56	56	120	184	248
	57	57	121	185	249
	58	58	122	186	250
	59	59	123	187	251
	60	60	124	188	252
	61	61	125	189	253
	62	62	126	190	254
	63	63	127	191	255

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Figure 36. Multiplexer/S Addresses

Mpx/R. Each 1851 ordered is assigned the 64 addresses shown in these two illustrations.

Mpx/S groups are installed in an 1851 in the following sequence: group 0, group 1, group 2, and group 3. For example, if two groups of Mpx/S are ordered, they are installed in group 0 and group 1. Addresses are assigned to each 1851, so that in the preceding example, 32 addresses are assigned to group 0 and 1, and 32 addresses are reserved for groups 2 and 3.

Addresses for 1851's containing Mpx/R (Mpx/S and Mpx/R are not installed in the same 1851) are assigned as shown in Figure 37. Mpx/R groups are installed in an 1851 in one of the following sequences, depending on system configuration:

1. 1851's containing all high-level inputs or all the same low-level range are installed in the following sequence: group 0, group 1, group 2, and group 3.
2. 1851's containing high-level inputs and one low-level input range (maximum two ranges per 1851) are installed in the following sequence: high-level starting with group 0 and ascending, low-level starting with group 3 and descending. For example, if one group of high-level and three groups of ±10 mV range are ordered for the same 1851, the one group of high level is installed in group 0 and the three groups of ±10 mV range are installed in groups 3, 2, and 1. An exception to this sequence occurs when the groups of high-level inputs are installed in an 1851 model 2. In this type of installation, points 00 and 01 are reserved for reference voltage and RBT, respectively. Therefore, high-level groups are installed starting with group 3 and descending, and the thermocouple inputs are installed starting with group 0 and ascending (opposite of the preceding example). An 1851 model 2 must have the ±10 mV, ±20 mV, or ±50 mV range specified for group 0.
3. 1851's containing two ranges of low-level inputs have the first range installed in ascending order starting with group 0. The second range is installed in descending order starting with group 3. For example, if two groups of ±10 mV range and two groups of ±20 mV range are ordered, the two groups of the ±10 mV range are installed in groups 0 and 1, and the two groups of ±20 mV range are installed in groups 3 and 2.

PROGRAMMED CONTROL MODES

This section describes the control modes for selection of analog input points, conversion of the

Numbering within 1851		1851's with Multiplexer/R															
Group Number	Point Number	1st 1851	2nd 1851	3rd 1851	4th 1851	5th 1851	6th 1851	7th 1851	8th 1851	9th 1851	10th 1851	11th 1851	12th 1851	13th 1851	14th 1851	15th 1851	16th 1851
	00	00	64	128	192	256	320	384	448	512	576	640	704	768	832	896	960
	01	01	65	129	193	257	321	385	449	513	577	641	705	769	833	897	961
	02	02	66	130	194	258	322	386	450	514	578	642	706	770	834	898	962
	03	03	67	131	195	259	323	387	451	515	579	643	707	771	835	899	963
	04	04	68	132	196	260	324	388	452	516	580	644	708	772	836	900	964
	05	05	69	133	197	261	325	389	453	517	581	645	709	773	837	901	965
	06	06	70	134	198	262	326	390	454	518	582	646	710	774	838	902	966
0	07	07	71	135	199	263	327	391	455	519	583	647	711	775	839	903	967
	08	08	72	136	200	264	328	392	456	520	584	648	712	776	840	904	968
	09	09	73	137	201	265	329	393	457	521	585	649	713	777	841	905	969
	10	10	74	138	202	266	330	394	458	522	586	650	714	778	842	906	970
	11	11	75	139	203	267	331	395	459	523	587	651	715	779	843	907	971
	12	12	76	140	204	268	332	396	460	524	588	652	716	780	844	908	972
	13	13	77	141	205	269	333	397	461	525	589	653	717	781	845	909	973
	14	14	78	142	206	270	334	398	462	526	590	654	718	782	846	910	974
	15	15	79	143	207	271	335	399	463	527	591	655	719	783	847	911	975
	16	16	80	144	208	272	336	400	464	528	592	656	720	784	848	912	976
	17	17	81	145	209	273	337	401	465	529	593	657	721	785	849	913	977
	18	18	82	146	210	274	338	402	466	530	594	658	722	786	850	914	978
	19	19	83	147	211	275	339	403	467	531	595	659	723	787	851	915	979
	20	20	84	148	212	276	340	404	468	532	596	660	724	788	852	916	980
	21	21	85	149	213	277	341	405	469	533	597	661	725	789	853	917	981
	22	22	86	150	214	278	342	406	470	534	598	662	726	790	854	918	982
	23	23	87	151	215	279	343	407	471	535	599	663	727	791	855	919	983
1	24	24	88	152	216	280	344	408	472	536	600	664	728	792	856	920	984
	25	25	89	153	217	281	345	409	473	537	601	665	729	793	857	921	985
	26	26	90	154	218	282	346	410	474	538	602	666	730	794	858	922	986
	27	27	91	155	219	283	347	411	475	539	603	667	731	795	859	923	987
	28	28	92	156	220	284	348	412	476	540	604	668	732	796	860	924	988
	29	29	93	157	221	285	349	413	477	541	605	669	733	797	861	925	989
	30	30	94	158	222	286	350	414	478	542	606	670	734	798	862	926	990
	31	31	95	159	223	287	351	415	479	543	607	671	735	799	863	927	991
	32	32	96	160	224	288	352	416	480	544	608	672	736	800	864	928	992
	33	33	97	161	225	289	353	417	481	545	609	673	737	801	865	929	993
	34	34	98	162	226	290	354	418	482	546	610	674	738	802	866	930	994
	35	35	99	163	227	291	355	419	483	547	611	675	739	803	867	931	995
	36	36	100	164	228	292	356	420	484	548	612	676	740	804	868	932	996
	37	37	101	165	229	293	357	421	485	549	613	677	741	805	869	933	997
	38	38	102	166	230	294	358	422	486	550	614	678	742	806	870	934	998
	39	39	103	167	231	295	359	423	487	551	615	679	743	807	871	935	999
2	40	40	104	168	232	296	360	424	488	552	616	680	744	808	872	936	1000
	41	41	105	169	233	297	361	425	489	553	617	681	745	809	873	937	1001
	42	42	106	170	234	298	362	426	490	554	618	682	746	810	874	938	1002
	43	43	107	171	235	299	363	427	491	555	619	683	747	811	875	939	1003
	44	44	108	172	236	300	364	428	492	556	620	684	748	812	876	940	1004
	45	45	109	173	237	301	365	429	493	557	621	685	749	813	877	941	1005
	46	46	110	174	238	302	366	430	494	558	622	686	750	814	878	942	1006
	47	47	111	175	239	303	367	431	495	559	623	687	751	815	879	943	1007
	48	48	112	176	240	304	368	432	496	560	624	688	752	816	880	944	1008
	49	49	113	177	241	305	369	433	497	561	625	689	753	817	881	945	1009
	50	50	114	178	242	306	370	434	498	562	626	690	754	818	882	946	1010
	51	51	115	179	243	307	371	435	499	563	627	691	755	819	883	947	1011
	52	52	116	180	244	308	372	436	500	564	628	692	756	820	884	948	1012
	53	53	117	181	245	309	373	437	501	565	629	693	757	821	885	949	1013
	54	54	118	182	246	310	374	438	502	566	630	694	758	822	886	950	1014
	55	55	119	183	247	311	375	439	503	567	631	695	759	823	887	951	1015
3	56	56	120	184	248	312	376	440	504	568	632	696	760	824	888	952	1016
	57	57	121	185	249	313	377	441	505	569	633	697	761	825	889	953	1017
	58	58	122	186	250	314	378	442	506	570	634	698	762	826	890	954	1018
	59	59	123	187	251	315	379	443	507	571	635	699	763	827	891	955	1019
	60	60	124	188	252	316	380	444	508	572	636	700	764	828	892	956	1020
	61	61	125	189	253	317	381	445	509	573	637	701	765	829	893	957	1021
	62	62	126	190	254	318	382	446	510	574	638	702	766	830	894	958	1022
	63	63	127	191	255	319	383	447	511	575	639	703	767	831	895	959	1023

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Figure 37. Multiplexer/R Addresses

selected analog signal to a digital value, and transfer of the digital value to the P-C.

Three basic control modes exist for input of analog data: (1) direct program control, (2) data channel sequential, and (3) data channel random. Essentially, direct program control mode requires execution of at least one execute I/O (XIO) instruction for each value that is read into the P-C. Data channel sequential mode uses one data channel and allows any number of groups of sequentially addressed values to be read into the P-C with execution of one XIO. Data channel random mode uses two data channels and allows each point to be addressed uniquely. Any number of groups of points may be addressed, converted, and read into the P-C with execution of two XIO's.

Direct Program Control

In the direct program control mode of operation, two XIO's are used. The first, an XIO write, addresses the multiplexer and selects the analog input point which is to be converted. Upon completion of multiplexing, an internal signal is sent to the ADC to start the point conversion. When the ADC has completed the conversion, an interrupt signal is sent from the ADC to the P-C. The P-C initiates a subroutine to determine the cause of the interrupt, if necessary, and provides the second XIO, an XIO read, to transfer the data to storage. This mode of converting data from analog signals to digital values in core storage is a discrete addressing method; that is, two XIO's result in the acquisition of data from one input point.

DIRECT PROGRAM CONTROL SEQUENTIAL: A special mode of direct program control can be used if analog points are to be converted in sequence. This mode requires only one write followed by a series of reads -- one for each point. Modifier bit 8 being on in the XIO read causes the multiplexer to add 1 to the address previously converted and then to perform the next cycle. (A cycle consists of selecting the analog input point, converting the selected analog signal, and initiating an interrupt to inform the P-C that the converted value is ready to be read into core storage.) Modifier bit 8 being off in an XIO read terminates the operation.

Data Channel Sequential

In this mode, which uses a single data channel, a sequence of analog input points is scanned, converted, and stored in core storage -- with only one XIO initialize read initiating the action.

The address field of the input/output control command (IOCC) contains the core storage address of a data table. The first word of the data table contains the word count and scan control bits for the data table. The word count is 1 greater than the number of input signals to be converted in the sequence. The scan control bits determine whether an interrupt is given and whether chaining or termination of the operation occurs when the word count reaches 0.

The initial multiplexer address is contained in the word following the word count and scan control bits in the data table. The data channel "writes" this multiplexer address word into the analog multiplexer address register (AMAR), thus initiating the selection of analog points and subsequent conversion to digital values. At the completion of each conversion, the converted data is read into sequential storage locations. After each transfer of data, the word count is decreased by 1, and the previous address is increased by 1. The new address causes the next sequential point to be selected. This operation continues until the word count reaches 0.

Figure 38 illustrates two data tables which are in core storage and could be used for chained sequential operation. The IOCC that initiates this

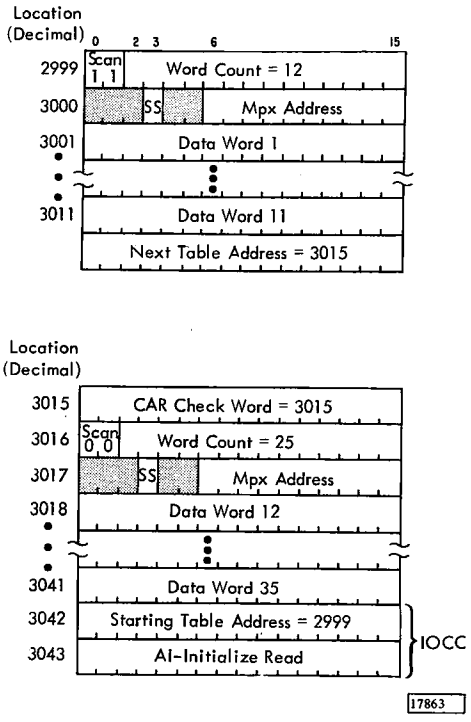


Figure 38. Analog Input Data Tables, Chained Sequential Mode

analog input operation is located in storage locations 3042 and 3043. The IOCC initializes the multiplexer and ADC and then places the address of the word count (the first word in the table) into the channel address register (CAR) of the data channel. In this example, the word count is located in storage location 2999.

The ADC now requests a data channel cycle to place the word count into the word count register. In this example, the word count is 12. CAR is increased by 1 so that now CAR contains the address 3000. On the next data channel cycle, the initial multiplexer address is transferred from location 3000 to the AMAR. When multiplexing is complete, a signal is sent to the ADC to start conversion. At the completion of conversion, the ADC register contains a digital value and a data channel cycle is requested. CAR (now containing address 3001) addresses core storage, and the digital value in the ADC output register is transferred to location 3001.

The preceding procedure is repeated and continues until the word count reaches 0. At this time, the scan control bits are monitored and it is discovered that they indicate continued scanning (11). When continuous scan is indicated, the data channel takes four cycles to initialize the I/O device for the next data table. The first cycle transfers the word following the first data table to CAR. (This word contains the core-storage location of the next table.) The second cycle addresses core storage and transfers the contents of the first word of the next data table to the B-register. A CAR check is then made. The third cycle transfers the word count and scan control bits from the second word of this data table to their respective registers in the I/O device. The fourth cycle transfers the multiplexer address from the third word of the data table to the AMAR. Data transfers then resume by means of data channel operations.

When the word count again reaches 0, the scan control bits indicate that the operation is to be terminated and an interrupt generated. The operation is now terminated. A new XIO is required to initiate further operations.

Data Channel Random

In this mode of operation, the multiplexer addresses are transferred on one data channel, and the ADC data is transferred on a second data channel. The operation is initiated with two XIO's. The first, an XIO initialize read, performs two functions: (1) sets up the controls for transferring converted data from the ADC to storage on one channel, and (2) loads the scan control register and word count register for the operation. (The word count is equal to the number of converted values to be stored.) The second, an XIO initialize write, initiates the transfer of multiplexer addresses from core storage to the analog multiplexer address register on the other data channel.

When the first analog input point has been selected, the ADC is started. At the completion of the first conversion, a data channel cycle transfers the converted data to the data table in core storage. Alternate data channel cycle requests bring in the multiplexer addresses on one channel and transfer the converted data to storage on the other channel. This operation continues until the word count is decremented to 0. When this occurs, the scan control bits are interrogated to determine whether an interrupt is to be given and whether the operation is to continue or terminate.

Figures 39 and 40 illustrate multiplexer address and ADC storage tables that are to perform a random addressing operation. An XIO initialize read referencing location 3524 initiates ADC action. An XIO initialize write referencing location 3122 initiates multiplexing.

In this example (Figures 39 and 40), 119 points are being read and converted in a random sequence. The two ADC tables are chained together, while the multiplexer table is chained to itself. The scan control bits cause an interrupt at the end of each ADC table. The number of multiplexing addresses set up in the multiplexer address table must equal the word count set up in the ADC table. Comparator limit words, if used, are not included in the word count.

Systems with two data channels may convert values while operating in random mode. Modifier bit 10

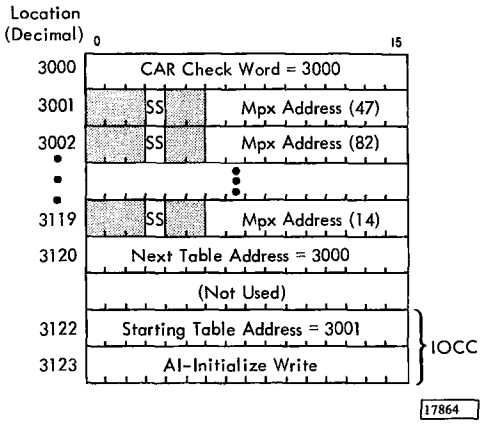


Figure 39. Multiplexer Address Table, Random Mode

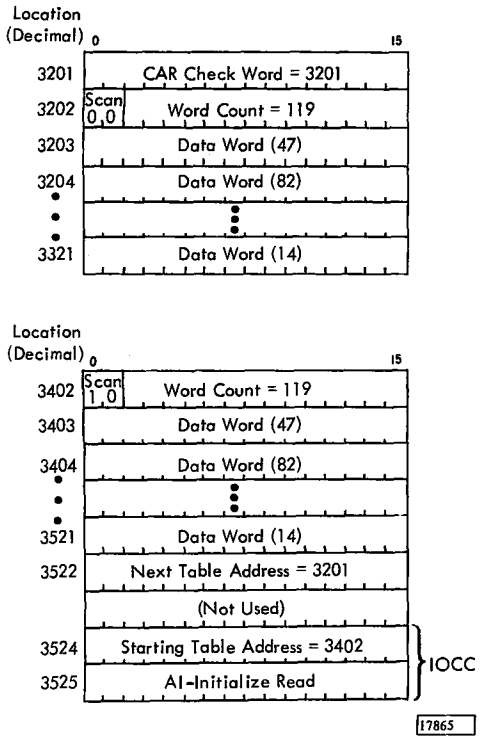


Figure 40. ADC Table, Chained Random Mode

being on in the XIO initialize read specifies random mode; modifier bit 10 being off specifies sequential mode.

If overlap special feature is used, the ADC word count is equal to the number of solid state points. Because relay points are read by direct program control, they are not stored in the ADC storage table.

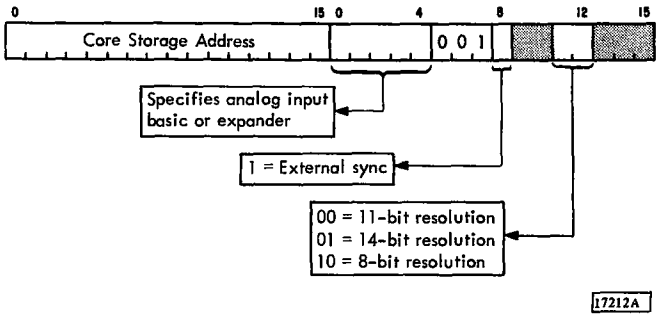
ANALOG INPUT PROGRAMMING

Analog input operates under direct program control or data channel control for data transfer and utilizes the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO must have an area code of 01010 to address analog input basic or 10000 to address analog input expander. The following IOCC's provide operation and control of analog input features.

Analog Input IOCC's

Write

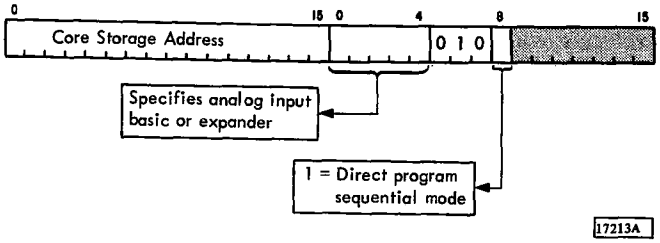


This command causes the multiplexer address located at the core storage location specified by the IOCC address field to be sent to the analog multiplex address register. After the multiplex point is selected and converted, a DPC (direct program control) conversion complete interrupt is given. This interrupt indicates that the converted value is ready to be read into core storage.

An XIO read or an XIO blast reset instruction must be executed for every XIO write instruction given. Failure to do this will cause the relay conversion circuit to remain on for DPC relay operations, or the DPC solid state busy circuit to remain on for solid-state operations.

The functions of modifier bits that further define the command are shown in the preceding illustration.

Read

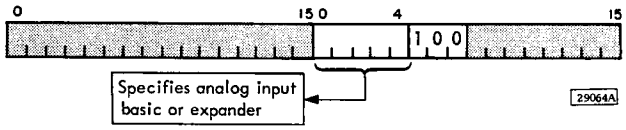


This command causes the converted data in the ADC to be read into the core storage location specified by the IOCC address field. If modifier bit 8 is off, the operation is considered complete after the data is

read. If modifier bit 8 is on, the analog multiplex address register is increased by 1 and the next sequential multiplex point is selected and converted. After this multiplex point is converted, a DPC (direct program control) conversion complete interrupt is given. This interrupt indicates that the converted value is ready to be read into core storage by another XIO read. This sequential operation continues until an XIO read with modifier bit 8 off is given.

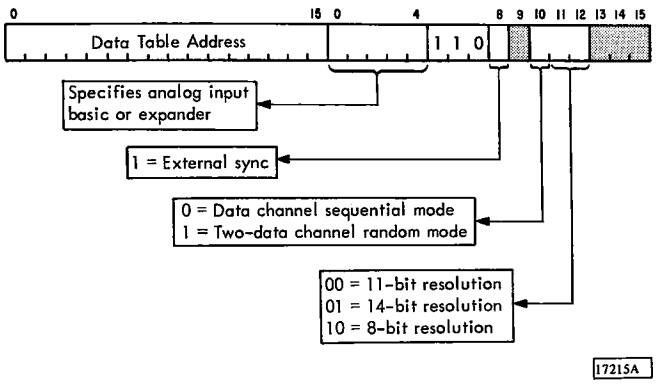
An XIO read performed before a conversion complete interrupt may result in a data parity error. The ADC data word is stored in memory regardless of whether the parity is good.

Control



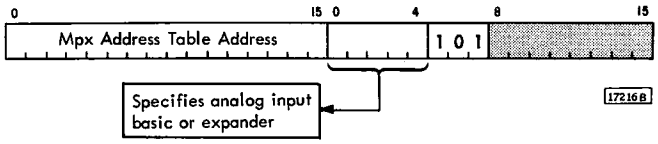
This command (blast reset) can be used to immediately halt analog input operation. All ADC basic controls and registers, the multiplexer, and the comparator are reset by execution of this command. If an I/O operation is in progress, it is terminated and the analog input is released. Analog input is thus made available for another XIO.

Initialize Read



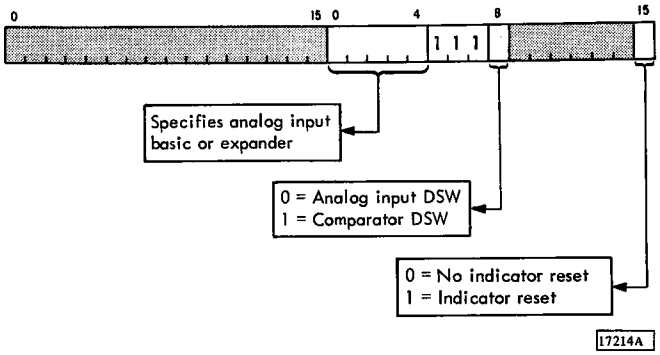
This command initializes the analog input and data channel in preparation for transferring converted data from the ADC to core storage. The analog input may be initialized to one of two modes: data channel sequential or data channel random. Analog input operations for these two modes are described under "Data Channel Sequential" and "Data Channel Random".

Initialize Write



This command initiates the transfer of multiplexer addresses from the address table specified by the address field to the analog multiplexer address register. This command is used only in two data channel random mode. Operation with this mode is described under "Data Channel Random".

Sense Device



This command causes the device status word (DSW) specified by modifier bit 8 to be read into the accumulator (A). If modifier bit 8 is off, the analog input DSW (Figure 41) is read. If modifier bit 8 is on, the comparator DSW (Figure 42) is read.

Modifier bit 15 controls the reset of the program resettable indicators in the DSW read. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset.

Analog Input DSW Interrupt Indicators

All analog input basic interrupts are combined into one interrupt signal. This signal is assigned to an interrupt level and an interrupt level status word (ILSW) bit position.

All analog input expander interrupts are combined into one interrupt signal. This signal is assigned to the same interrupt level as analog input basic, but to a different ILSW bit position. Analog input and comparator interrupts may be assigned to the same interrupt level if desired.

Figure 41 shows the format of the analog input DSW and defines the indicators that cause interrupts. Program resettable indicators are also defined.

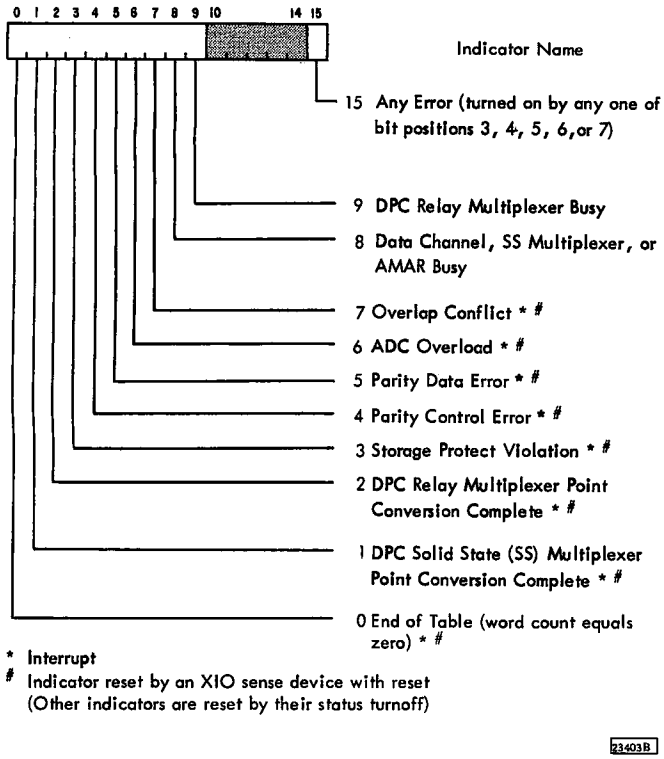


Figure 41. Analog Input Device Status Word

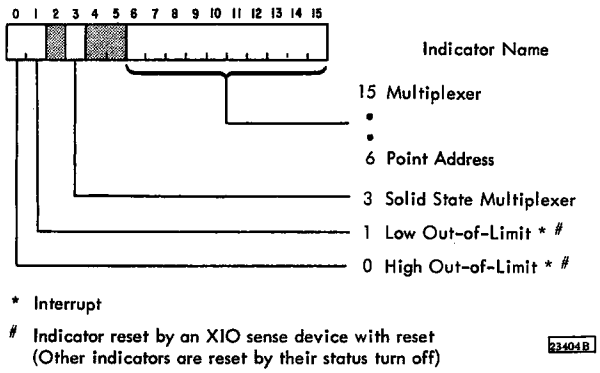


Figure 42. Comparator Device Status Word

END OF TABLE: This indicator turns on, causing an interrupt, when the word count is decreased to 0 during data channel operations in which the scan control bits have specified an end-of-table interrupt.

DPC SS CONVERSION COMPLETE: During direct program control (DPC) operation, this indicator turns on when a solid state (SS) multiplex point conversion is complete. The indicator turning on causes an interrupt to notify the program that the converted data is ready to be transferred to core storage.

DPC RELAY CONVERSION COMPLETE: During direct program control (DPC) operation, this indicator turns on when a relay multiplex point conversion is complete. The indicator turning on causes an interrupt to notify the program that the converted data is ready to be transferred to core storage.

STORAGE PROTECT VIOLATION: This indicator turns on, causing an interrupt, if an attempt is made to store converted ADC data in a protected core storage location. If this occurs, all analog input operations are halted.

PARITY CONTROL ERROR: This indicator turns on, causing an interrupt, when a transmission parity error is detected during a control cycle. It is also turned on when a transmission or P-C parity error is detected during loading of the word counter, loading of the AMAR, or loading and checking of the CAR while chaining to another table. Analog input operations are halted.

PARITY DATA ERROR: This indicator turns on, causing an interrupt, if a parity error is detected when a multiplexer address or converted data is transferred between the P-C and analog input interface.

ADC OVERLOAD: This indicator turns on, causing an interrupt, if the input to the ADC exceeds the range of the ADC.

OVERLAP CONFLICT: During two data channel overlap operation, this indicator turns on if a second relay point is addressed before the first relay point has been converted. Overlap conflict turning on causes an interrupt.

Analog Input DSW Noninterrupt Indicators

Figure 41 shows the format of the analog input DSW and defines the noninterrupt indicators. Program resettable indicators are also defined.

DATA CHANNEL, SS MULTIPLEXER, OR AMAR BUSY: This indicator reflects the combined status of these three busy conditions:

1. Data channel busy turns on at the beginning of a data channel operation (relay or solid state) and remains on until the word count for the last data table is decreased to 0 (no chaining specified).
2. SS (solid state) multiplexer busy turns on when the solid state multiplexer is addressed. The indicator remains on until reset by an XIO read with modifier bit 8 off (read sequential not specified).

3. AMAR (analog multiplexer address register) busy is on while the AMAR is being used. This interval begins when an address is loaded into AMAR (or increased during sequential operation) and ends when the address is transferred to the multiplexer to select the input point.

A new XIO initialize read or XIO write cannot be initiated while the data channel, SS multiplexer, or AMAR busy indicator is on. Both of these instructions are ignored, and no indication is given to the program.

DPC RELAY BUSY: This indicator turns on when a relay multiplexer is addressed by an XIO write, or when a relay multiplexer is sequenced by an XIO read specifying sequential addressing. The indicator is turned off 800 μs after the relay conversion is completed unless another relay conversion is initiated before the end of the 800 μs period. A new relay point can be initiated after the DPC relay conversion complete interrupt has been serviced. The SS multiplexer can be used in overlap mode while this indicator is on.

Comparator DSW Interrupt Indicators

All comparator interrupts in analog input basic are combined into one interrupt signal. This signal is assigned to an interrupt level and an interrupt level status word (ILSW) bit position.

All comparator interrupts in analog input expander are combined into one interrupt signal. This signal is assigned to the same interrupt level as the comparator in analog input basic, but to a different ILSW bit position. Analog input and comparator interrupts may be assigned to the same interrupt level if desired.

Figure 42 shows the format of the comparator DSW and defines the indicators that cause interrupts. Program resettable indicators are also defined.

HIGH OUT-OF-LIMIT: This indicator turns on, causing an interrupt, when the comparator detects an ADC reading equal to or above the high limit specified.

LOW OUT-OF-LIMIT: This indicator turns on, causing an interrupt, when the comparator detects an ADC reading below the low limit specified.

Comparator DSW Noninterrupt Indicators

Figure 42 shows the comparator DSW format and defines the noninterrupt indicators. Program resettable indicators are also defined.

SOLID STATE MULTIPLEXER: This indicator is on when the multiplexer point address in DSW bits 6 through 15 is a solid state multiplexer point address.

MULTIPLEXER POINT ADDRESS: These bits identify the multiplexer point that caused an out-of-limit condition.

ANALOG INPUT EXECUTION TIMES

The following are typical times required for reading a series of analog input points. Note that the times are shown for the three core storage cycle times. In these examples, ADC conversion time is for 14-bit resolution. Eleven or 8-bit resolution is 8 or 15 μs per point faster, respectively. The following items should be considered when using these examples in determining system conversion rates:

- Time is not included for program instruction execution other than the instructions required to initiate and perform the analog input operations. It is assumed that the P-C is in a wait state at all other times. If instruction execution continues while conversions are being made, one core storage cycle should be added to each point converted.
- If the comparator is used, one core storage cycle must be added for each point in which a comparison is performed.
- If external sync is used, the elapsed time between 'ready' and the sync signal must be added to each point using external sync.
- Time is not included for any data channel (cycle steal) delay that may be encountered if other data channel operations are in progress during conversions. The exact delay depends on: (1) the priority of the data channel(s) assigned to analog input, and (2) the number of other data channel operations being performed.

Direct Program Control Operations

Multiplexer/R -- ADC Mod 1

Per Point	2 μs	2.25 μs	4 μs
XIO write	0.010 ms	0.011 ms	0.020 ms
Mpx relay	9.947	9.947	9.947
ADC conv.	0.044	0.044	0.044
Interrupt	0.110	0.124	0.220
XIO read	0.010	0.011	0.020
	10.121 ms	10.137 ms	10.241 ms

Multiplexer/S -- ADC Mod 1

Per Point	2 μs	2.25 μs	4 μs
XIO write	10.0 μs	11.3 μs	20.0 μs
Mpx/S and buffer amp.	10.0	10.0	10.0
ADC conv.	44.0	44.0	44.0
Interrupt	110.0	123.8	220.0
XIO read	10.0	11.3	20.0
	184.0 μs	200.4 μs	314.0 μs

Multiplexer/S -- ADC Mod 2

Per Point	2 μs	2.25 μs	4 μs
XIO write	10.0 μs	11.3 μs	20.0 μs
Mpx/S and S & H amp.	10.0	10.0	10.0
ADC conv.	44.0	44.0	44.0
Interrupt	110.0	123.8	220.0
XIO read	10.0	11.3	20.0
	184.0 μs	200.4 μs	314.0 μs

Data Channel Operations

One Data Channel -- Mpx/S -- ADC Mod 1

Initialize	2 μs	2.25 μs	4 μs
XIO initialize read	8.0 μs	9.0 μs	16.0 μs
Cycle steal (CS) word count	4.0	4.5	8.0
CS initial Mpx addr.	2.0	2.3	4.0
	14.0 μs	15.8 μs	28.0 μs

Per Point	2 μs	2.25 μs	4 μs
Mpx/S and buffer amp.	10.0	10.0	10.0
ADC conv.	44.0	44.0	44.0
ADC end delay	50.0	50.0	50.0
CS read data	2.5	3.1	5.0
	106.5 μs	107.1 μs	109.0 μs

Chaining	2 μs	2.25 μs	4 μs
CS new addr.	4.0 μs	4.5 μs	8.0 μs
CS CAR check	4.0	4.5	8.0
CS word count	4.0	4.5	8.0
CS Mpx addr.	4.0	4.5	8.0
	16.0 μs	18.0 μs	32.0 μs

One Data Channel -- Mpx/S -- ADC Mod 2

Initialize and chaining times are the same as those for the preceding "One Data Channel -- Mpx/S -- ADC Mod 1".

Per Point	2 μs	2.25 μs	4 μs
Mpx/S and S & H amp.	10.0 μs	10.0 μs	10.0 μs
ADC conv.	44.0	44.0	44.0
CS read data	2.5	3.1	5.0
	56.5 μs	57.1 μs	59.0 μs

Two Data Channel -- Mpx/S -- ADC Mod 1

Initialize	2 μs	2.25 μs	4 μs
XIO initialize read	8.0 μs	9.0 μs	16.0 μs
XIO initialize write	8.0	9.0	16.0
CS word count	4.0	4.5	8.0
CS Mpx addr.	2.0	2.3	4.0
	22.0 μs	24.8 μs	44.0 μs

Per Point	2 μs	2.25 μs	4 μs
Mpx/S and S & H amp.	10.0 μs	10.0 μs	10.0 μs
ADC conv.	44.0	44.0	44.0
ADC end delay	50.0	50.0	50.0
CS read data	2.5	3.1	5.0
	106.5 μs	107.1 μs	109.0 μs

Chaining	2 μs	2.25 μs	4 μs
CS new addr.	2.0 μs	2.3 μs	4.0 μs
CS CAR check	4.0	4.5	8.0
CS new addr.	4.0	4.5	8.0
CS CAR check	4.0	4.5	8.0
CS word count	4.0	4.5	8.0
CS Mpx addr.	4.0	4.5	8.0
	22.0 μs	24.8 μs	44.0 μs

Two Data Channels - - Mpx/S - - ADC Mod 2

Initialize and chaining times are the same as those for the preceding "Two Data Channels -- Mpx/S -- ADC Mod 1".

Per Point	2 μs	2.25 μs	4 μs
Mpx/S and S & H amp.	10.0 μs	10.0 μs	10.0 μs
ADC conv.	44.0	44.0	44.0
CS read data	2.5	3.1	5.0
	56.5 μs	57.1 μs	59.0 μs

THERMOCOUPLE OPERATION

A thermocouple is a device used for measuring temperatures. It produces a voltage that is directly and almost linearly proportional to the difference in temperature between the measuring junction (hot junction) and the reference junction (cold junction).

Several thermocouple types, employing different combinations of metal, are available. With an appropriate choice of thermocouple, temperatures as high as 9,000°F or as low as -450°F can be measured.

Converting Thermocouple Signals

The conversion of a thermocouple signal to a meaningful and accurate temperature value is performed as a part of the 1800 program. The following factors are used by the 1800 program to accomplish thermocouple signal conversion.

- Thermocouple calibration data.
- Resistance bulb thermometer (RBT) bridge output.
- RBT reference voltage output.
- RBT operating characteristics.
- Thermocouple signal.

Because of the interrelationship of these factors, care must be taken in correlating the measured signal to the actual temperature it represents.

Each process thermocouple is connected to the 1800 via an 1851 Multiplexer Terminal, Model 2. The thermocouple measuring (hot) junction is located in the process area (tank, furnace, and so on) where temperature sensing is desired, and the thermocouple reference (cold) junction is located in the 1851 Multiplexer Terminal, Model 2. The resistance bulb thermometer (RBT) and the reference voltage are also located in the 1851 model 2. Thus, the 1851 model 2 provides thermal stability for the reference junctions, a means of determining the temperature of the reference junction, and terminations for thermocouple signals.

The reference junction terminations are extended to signal conditioning elements in the 1851. From this point, the multiplexer selectively connects these signals to the ADC to be converted to a digital value.

Thermocouple Calibration Data

Figure 43 illustrates the operating curve of an iron-constantan (type J) thermocouple. A manufacturer's thermocouple calibration graph normally shows only one curve at a stated reference (cold junction) temperature. However, Figure 43 includes two curves (0°C and 25°C) to show the influence of the cold junction temperature. It also includes a straight line as an aid to judging linearity.

For complete and more accurate data about a specific thermocouple, refer to the calibration data available from the thermocouple manufacturer, or refer to calibration data available from a testing laboratory.

Resistance Bulb Thermometer

Essentially, an RBT is a wire-wound resistor whose electrical resistance varies with temperature. The RBT supplied with the 1851 model 2 provides a means of determining the reference junction temperature within the 1851 model 2.

The RBT resistor is electrically connected to a precision reference voltage and a Wheatstone bridge (balanced circuit). A temperature variation causes a change in resistance and a consequent imbalance of the bridge circuit. The voltage

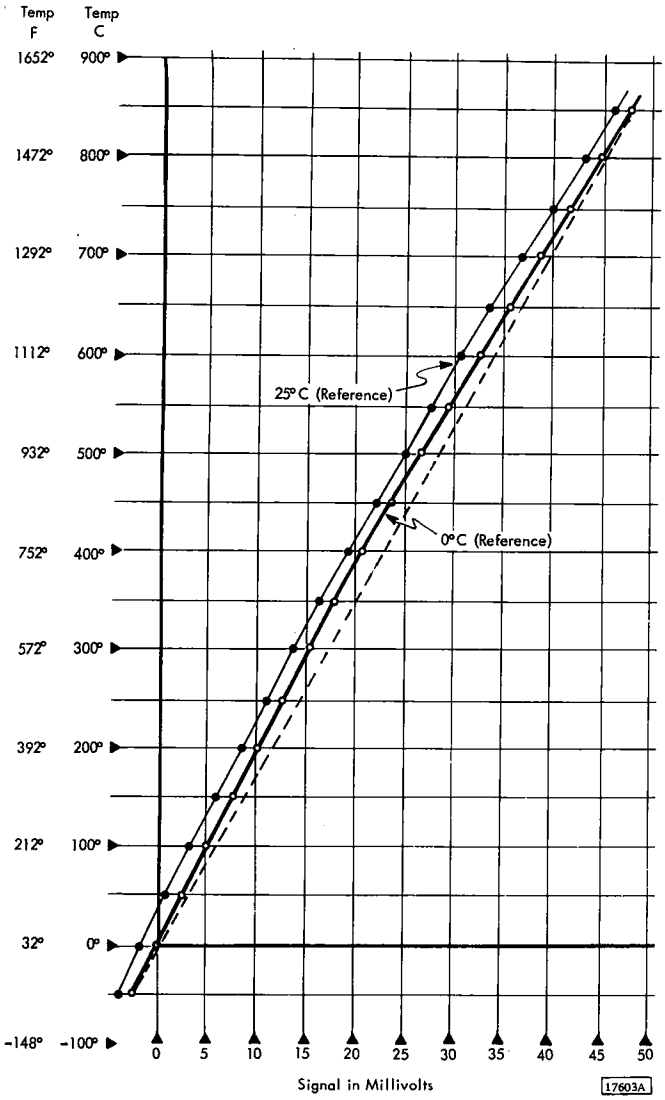


Figure 43. Iron-Constantan Thermocouple Chart

produced by this imbalance is called the RBT bridge output. This output and the reference voltage are made available to the 1800 program, which then interprets the two values. Thus, thermocouple signals are compensated for reference junction temperature changes.

The RBT circuit outputs are made available at the first and second address terminals within the 1851 model 2. (See Figure 37 for the Mpx/R address that will select points 00 and 01 within the 1851 model 2 being used). When point 01 (within an 1851 model 2) is selected by the multiplexer, the RBT bridge output is converted by the ADC to a digital value. When point 00 (within an 1851 model 2) is selected, the reference voltage is converted by the ADC to a digital value.

RBT Operating Characteristics

The RBT circuit supplied with the 1851 model 2 has the following characteristics.

Range		Reference Output			RBT Bridge Output		
		65°C	25°C	5°C	65°C	25°C	5°C
10 mV	Maximum	4.90 mV	4.63 mV	4.58 mV	10.00 mV	3.37 mV	0.12 mV
	Minimum	3.78 mV	3.70 mV	3.64 mV	7.91 mV	2.48 mV	-0.10 mV
20 mV	Maximum	9.58 mV	9.10 mV	9.01 mV	20.00 mV	6.63 mV	0.24 mV
	Minimum	7.47 mV	7.33 mV	7.21 mV	16.05 mV	4.90 mV	-0.19 mV
50 mV	Maximum	24.03 mV	23.16 mV	23.02 mV	50.01 mV	16.87 mV	0.61 mV
	Minimum	18.94 mV	18.71 mV	18.79 mV	39.58 mV	12.52 mV	-0.50 mV

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The preceding millivolt values are converted to a digital value by the ADC, and they are converted to the corresponding temperature by one of the following formulas.

$$T_{rbt}\,(^{\circ}F) = 51.876\ \frac{V_{rbt}}{V_r} + 41.0$$

$$T_{rbt}\,(^{\circ}C) = 28.82\ \frac{V_{rbt}}{V_r} + 5.0$$

Where:

T_{rbt} = RBT Temperature

V_{rbt} = ADC reading (Q value) for the RBT bridge output

V_r = = ADC reading (Q value) for the reference output

The values 51.876 and 41.0 (Fahrenheit) and 28.82 and 5.0 (Celsius) are constants for the RBT supplied with the thermocouple block. T_{rbt} can be computed in degrees Celsius and converted to degrees Fahrenheit with the following formula.

$$T_{rbt}\,(^{\circ}F) = \frac{9}{5}\ (\ T_{rbt}\ \text{in}\ ^{\circ}C\ ) + 32$$

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Thermocouple signals of up to ±50 mV can be terminated in the first Mpx/R group of an 1851 model 2. However, when the multiplexer (under control of the 1800 program) connects a thermocouple signal to the ADC, the millivolt signal is converted to a digital value between 00000 and ±16383. The 1800 program must compute a temperature that corresponds to the ADC value.

Thermocouple Conversion Accuracy

Accuracy of thermocouple signal conversion depends on many factors. Some of these factors are:

1. Accuracy of measurement of the reference (cold) junction temperature.

   The resistance bulb thermometer (RBT) circuit supplied with an 1851 model 2 provides two outputs (RBT reference and RBT bridge output). These two outputs, when converted by the ADC to a digital value and used in the proper formula, indicate the temperature of the reference (cold) junction within ±2°F.
2. Accuracy of thermocouples may vary from ±1-1/2°F to ±10°F, depending on the type of thermocouple used. For more specific information, refer to the manufacturer's specifications for the thermocouple being used.
3. Thermocouple measurement accuracy is largely dependent on the proper installation of the thermocouple.
4. Heat distribution within the medium being measured is another factor that affects the accuracy of the temperature measurement.

Thermocouple Conversion Example

The remainder of this section shows an example of thermocouple conversion. Three points should be stressed about the conversion procedure which follows:

1. It is recognized that there are other means, such as curve fitting, to convert thermocouple signals.
2. The following example is valid only when the RBT supplied with the 1851 model 2 is used.
3. Each thermocouple type must be separately correlated because their curves and operating ranges are different.

The following assumptions are made for the thermocouple conversion example.

- The thermocouple signal range is plus or minus 50 mV (amplifier gain of 100).
- The thermocouple is installed (hot junction) in a process area with a temperature region of 800°C.
- RBT temperature is 24.6°C (room temperature).
- Thermocouple calibration data is based on a 0°C reference curve (0°C curve in Figure 43).
- ADC value when reading the thermocouple signal is 15132.
- ADC value when reading RBT bridge output is 5182.
- ADC value when reading reference output is 7620.
- All numeric values in the example are base 10.
- The sample problem is presented immediately after each formula.

Converting Thermocouple Characteristics

For a computer conversion procedure, the thermocouple operating curve is considered as being formed of a series of short straight line segments. This segmentation is necessary because the millivolt output is not completely linear in relation to measured temperatures. This nonlinear relationship is most pronounced at the upper end of the thermocouple temperature range. Smaller segments provide closer approximation within each segment.

Study the manufacturer's calibration data (curve or table) to determine the number of segments or divisions that must be made to obtain the desired degree of accuracy. For example, the iron-constantan (type J) thermocouple curve shown in Figure 43 covers a temperature range of -50°C to +850°C. This range may be divided into nine segments as follows:

-50°C to +50°C
+50°C to +150°C
+150°C to +250°C
+250°C to +350°C
+350°C to +450°C
+450°C to +550°C
+550°C to +650°C
+650°C to +750°C
+750°C to +850°C

In order to correlate this operational curve to an actual temperature by a computer program, several intermediate values must be determined. Determination of these intermediate values (steps 1 through 5 of the following procedure) must be done once for each thermocouple type in the system.

1. The size of signal (in millivolts) required to produce an ADC digital value of one bit.

$$K_{adc} = 0.3051758 \text{ mV}$$

Where:

K_{adc} = Value of one ADC register bit

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2. Determine the ADC reading (Q value) that will be developed in the ADC register for each point used in the segmentation of the manufacturer's calibration curve. (See the 0°C reference curve in Figure 43.)

$$Q = \frac{V_t \times G}{K_{adc}}$$

Where:

Q = ADC digital value
V_t = Voltage in the thermocouple circuit (each point used is calculated separately)
G = Gain of the differential amplifier
K_{adc} = Determined previously

For example:

$$Q\ (-50^\circ C) = \frac{-2.42 \times 100}{0.3051758} = -793$$

$$Q\ (+50^\circ C) = \frac{2.58 \times 100}{0.3051758} = 845$$

$$Q\ (+750^\circ C) = \frac{42.32 \times 100}{0.3051758} = 13{,}867$$

$$Q\ (+850^\circ C) = \frac{48.73 \times 100}{0.3051758} = 15{,}968$$

29167

3. Determine the slope (A) of each segment of the calibration curve.

$$A = \frac{\Delta \text{degrees}}{\Delta Q}$$

Where:

Both Δ degrees and Δ Q are the difference in the extremes of each segment.
Q values were obtained in a previous step.
A has a dimension of degrees per digit.

For example:

$$A\ (-50^\circ C \text{ to } +50^\circ C \text{ Segment}) = \frac{100}{1638} = 0.0610$$

$$A\ (+750^\circ C \text{ to } +850^\circ C \text{ Segment}) = \frac{100}{2101} = 0.0476$$

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4. Determine the temperature axis (Y-axis) intercept point (B) for each segment. This is the point where a line extended from the segment at the same slope would cross the Y-axis.

$$T = A \times Q + B$$

or

$$B = T - A \times Q$$

Where:

A and Q values were obtained previously
B has a dimension of degrees
T is temperature in degrees corresponding to the same end point of the segment as the lower of the Q values

For example:

$$B\ (-50^\circ C \text{ to } +50^\circ C \text{ Segment}) = -50 - (0.0610 \times -793)$$
$$= -50 - (-48.37)$$
$$= -1.63$$

$$B\ (+750^\circ C \text{ to } +850^\circ C \text{ Segment}) = 750 - (0.0476 \times 13{,}867)$$
$$= 750 - (660)$$
$$= 90$$

29169A

5. Determine constants C and D for the segment that includes 25°C (the segment that includes the approximate RBT temperature).

$$C = \frac{1}{A}$$

$$D = -\frac{B}{A}$$

Where:

Constants C and D define this segment (-50° to +50°C) relative to the signal axis (x - axis)

C has a dimension of digits per degree
D has a dimension of digits

For example:

$$C = \frac{1}{0.0610} = 16.4$$

$$D = -\frac{-1.63}{0.0610} = 26.7$$

29170A

The A, B, C, D, and Q values can now be stored in the 1800 core storage to be used by the program when the thermocouple signal is read. The preceding steps provide a "program image" of the thermocouple curve. Each thermocouple type used in a system must be similarly defined and correlated.

Determining Cold Junction Temperature

The cold-junction temperature must be determined as often as indicated by (1) 1851 model 2 ambient air temperature changes, and (2) the accuracy of the measurement desired. The following steps (6 through 8) are required to determine the RBT temperature and adjust it for the effects of the calibration curve at the RBT temperature.

6. The 1800 program must read the RBT bridge output and the reference output as described in the section for resistance bulb thermometer.
7. Using the ADC readings for the RBT bridge output and reference voltage, compute the temperature indicated by the RBT.

$$T_{rbt}\,(^{\circ}C) = 28.82\ \frac{V_{rbt}}{V_r}\ +5.0$$

Where:

T_{rbt} = RBT temperature
V_{rbt} = ADC reading for RBT bridge output
V_r = ADC reading for reference voltage
28.82 and 5.0 are constants

For example:

$$T_{rbt}\,(^{\circ}C) = 28.82\ (\frac{5182}{7620}) + 5.0$$
$$= 28.82\,(0.68) + 5.0$$
$$= 24.6^{\circ}\,C$$

29171

8. Adjust the RBT temperature for the effects of the calibration curve slope at the RBT temperature.

$$R_{rbt} = C\,(T_{rbt}) + D$$

Where:

R_{rbt} = Adjusted Q value of T_{rbt}
C and D were obtained previously
T_{rbt} was obtained previously

For example:

$$R_{rbt} = 16.4\,(24.6) + 26.7$$
$$= 403.4 + 26.7$$
$$= 430$$

29172A

Determining Thermocouple Temperature

The following steps are performed for each thermocouple signal selected by the multiplexer.

9. The multiplexer, under control of the 1800 program, connects the thermocouple signal to the ADC for conversion to a digital value (Q value). To adjust the Q value for the effects of the cold-junction temperature, use the following formula.

$$R_{tc} = V_{tc} + R_{rbt}$$

Where:

R_{tc} = Adjusted Q value for the thermocouple signal
V_{tc} = ADC reading (Q value) for the thermocouple signal
R_{rbt} was obtained previously

For example:

$$R_{tc} = 15{,}132 + 430$$
$$= 15{,}562$$

29173A

10. The previous step establishes the correct segment of the calibration curve to be used in the determination of thermocouple temperature. The 1800 program must use the adjusted Q value for the thermocouple signal to determine which of the A and B values (previously stored in core storage) are to be used in the final step to determine actual thermocouple measuring junction temperature. Use the following formula to complete the computation of thermocouple temperature.

$$T_{tc} = A\,(R_{tc}) + B$$

Where:

T_{tc} = Thermocouple measuring (hot) junction temperature
A and B = The values corresponding to the segment (750° to 850°) that includes the Q value from the previous step.
R_{tc} was obtained previously

For example:

$$T_{tc} = 0.0476 \times 15{,}562 + 90$$
$$= 830.7^{\circ}\,C$$

29174A

Digital Input

Digital input features enable the processor-controller (P-C) to accept real-time digital information in a digital format. The modular design of the features permit individual system tailoring for specific types and quantities of digital input data, such as:

- Contact sense.
- Voltage level sense.
- Contact interrupt.
- Voltage level interrupt.
- Digital voltmeters.
- Special analog-to-digital converters.
- Turbine flowmeters.
- Shaft encoders.
- Electronic registers, including telemetry.
- Mechanical counters.
- Electronic counters.
- Rotary switches from operator panels.
- Sense switches from operator panels.
- Pulse tachometers.
- Frequency meters.
- Watt-hour meters.
- Vibration detectors.
- Weighing devices.

Digital input is brought into the system in 16-bit groups. The format may be in any form. For example:

- Unrelated bits from contact or voltage levels.
- Binary numbers.
- Binary-coded-decimal digits.
- Decimal digits.
- Gray code digits.

Any mixture of digital formats can be handled. Conversion from one base to another can be easily and quickly implemented by the program. Data input is under direct program control or data channel control. In direct program control, one instruction is used to bring 16 bits of data into core storage. With a data channel, one instruction initiates an operation that brings many 16-bit groups of data into core storage (one group per core storage cycle). The number of groups read (sequentially, randomly, or single address) and synchronization of the P-C to the input data are handled automatically.

Interrupt conditions from the process are a type of digital input. These process interrupts are brought into the P-C in 16-bit groups, with up to four priority levels of interrupt and four interrupt conditions per level for each 16-bit group.

High-speed 8-bit or 16-bit binary electronic pulse counters are available as special features. Counters are read into core storage as digital input groups, 16 bits at a time (two 8-bit counters or one 16-bit counter).

As shown in Figure 44, the combined capacity of the digital input and pulse counter features is 1,024 bits, as follows:

Digital Input
8 adapter x 8 digital input groups
x 16 bits per group = 1,024.

Pulse Counter
8 adapter x 128 pulse counter bits per adapter (pulse counters can be 8-bit or 16-bit counters) = 1,024.

Any combination of these adapters, digital input groups, and pulse counters may be used within the capacity of 1,024 bits.

The capacity of the process interrupt feature is 24 priority levels or 384 bits, as follows:

8 adapter x 3 process interrupt groups
(24 levels)
x 16 bits per group = 384

Control for digital input features is provided by digital input basic, which is supplied with the basic P-C. Digital input basic provides timing control, checking control, and an interface to the P-C for all digital input features.

The 1826 Data Adapter Unit provides housing for digital input points. The following units and features may be added to the system to provide digital input functions. For specifications, see 1800 Installation Manual - Physical Planning, Order No. GA26-5922.

DATA CHANNEL ADAPTER

This feature adapts digital input basic to a data channel and provides the controls necessary to enable digital input via data channel (cycle steal) operations. A word counter and scan control

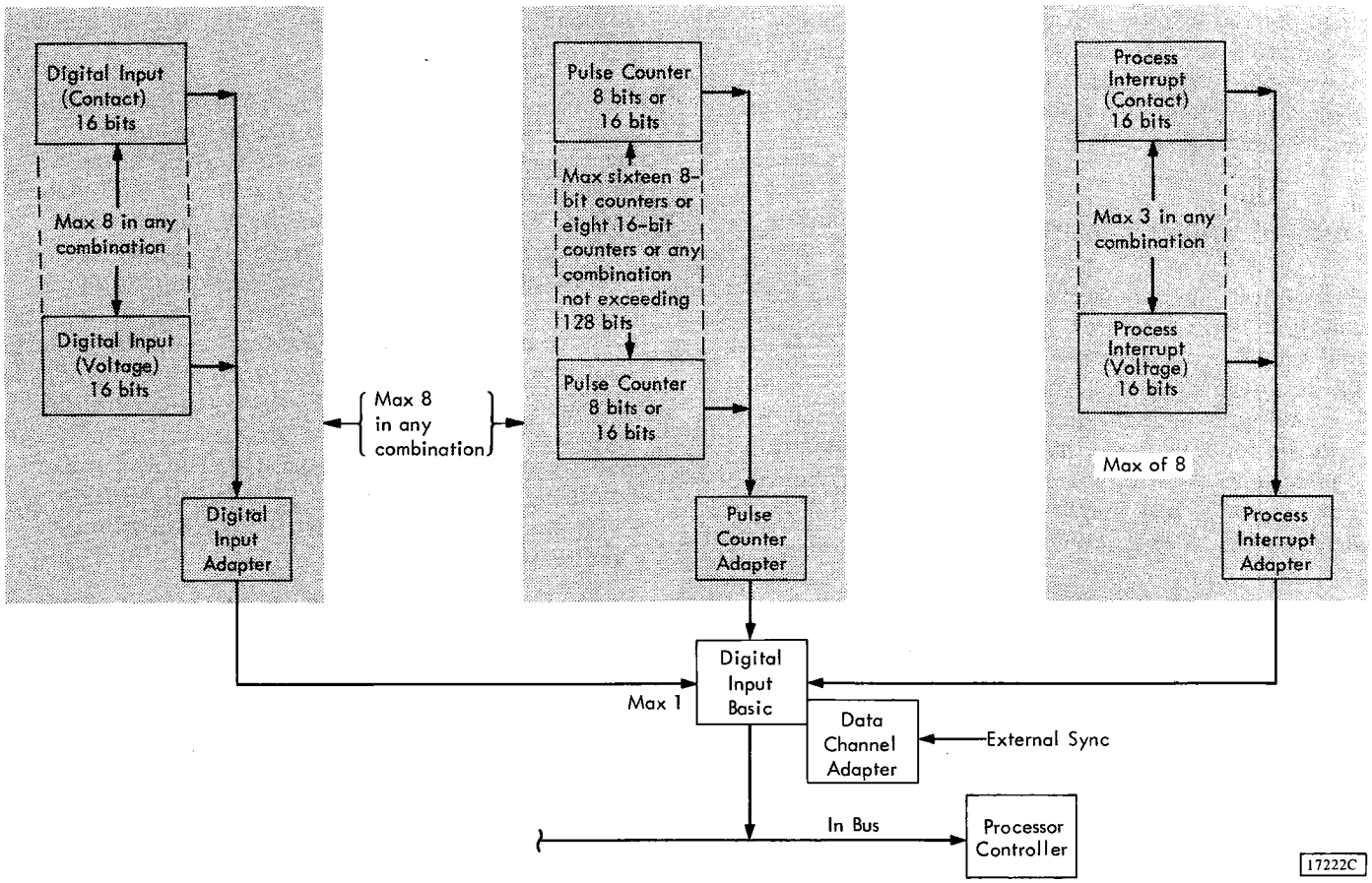


Figure 44. Digital Input Configuration

circuits are provided for counting the number of data transfers and specifying the action to be taken after the last word has been transferred to a data table in core storage.

The data channel adapter also provides controls which permit each data transfer to core storage from digital input to be controlled by an external timing (sync) pulse. Therefore, digital input operations can be performed with or without external sync.

Operation With External Sync

External sync operation is initiated by an XIO initialize read with modifier bit 8 on. After digital input basic has received a digital input group address from core storage through data channel operation, a ready signal is sent to the external timing device. The ready signal indicates that the addressed digital input group is ready to be read. When the external device receives the ready signal and has data to be read, it transfers the data to the addressed digital input group and sends a sync pulse to the data channel adapter. The sync pulse initiates a data channel (cycle steal) operation, which causes the data to be read and transferred to a data table in core storage.

The ready and sync exchange will continue and the digital input feature will be interlocked until the word count is decreased to 0; however, the P-C program can continue to run while the digital input feature is interlocked.

Operation Without External Sync

Digital input operation without external sync is initiated by an XIO initialize read with modifier bit 8 off. Digital input group addresses are transferred to digital input basic, and input data read are transferred to core storage by data channel (cycle steal) operations. The speed of this digital input read operation is at the maximum rate of the data channel (core storage cycle) unless a higher priority data channel request is honored. Once started, a digital input

read operation without external sync continues to completion by means of continuous data channel operations. Therefore, the P-C is essentially locked out from program execution until the digital input read operation is completed.

DIGITAL INPUT ADAPTER

The digital input adapter is a prerequisite for contact type digital input or voltage type digital input and provides control facilities for up to eight 16-bit digital input groups.

As many as eight digital input adapters may be ordered for a system, thus providing facilities for a maximum of 64 digital input groups. Any logical grouping of 16 bits may be used to form a digital input group. For example:

Sixteen bits of status information.
Four 4-bit BCD digits.
One 10-bit coded decimal digit and 6 bits of status.
One 16-bit binary number.

Sixteen screw-down terminals (0 through 15) are provided for termination of each input group signal wires; two wires are used for each bit. Terminal positions 0 through 15 correspond to P-C word bit positions 0 through 15 respectively when the input group is read.

A digital input channel can be created for process operator consoles or other low speed devices by using the electronic "contact" operate digital output feature to select various devices for input via a single 16-bit digital input group. Process operator console input devices and cabling are available on a Request for Price Quotation (RPQ) basis.

Digital Input Points

Two types of digital input points can be ordered in modular groups of 16. One type operates in conjunction with a customer supplied process contact and is called digital input (contact). The other type senses the level of voltage supplied from customer devices and is called digital input (voltage). In conjunction with the second (voltage) type of input, a high-speed digital input feature is available. In any case, all 16 input points of a digital input group must be of the same type.

DIGITAL INPUT (CONTACT): Contact input enables the P-C to read the status of process contacts. When a contact input group is read, each closed contact causes a 1-bit to be placed in the corresponding P-C word bit position, and each open contact causes a 0-bit to be placed in the corresponding P-C word bit poisition. Read speeds of up to 500,000 words per second are possible on a 2 μs system when using a data channel and no external sync. However, repetitive reading of the same group cannot be performed at this rate and still reliably sense a change in the input status. This restriction is caused by recovery delay of the input noise filter located at each digital input point. See IBM 1800 Installation Manual -- Physical Planning, Order No. GA26-5922 for specifications.

DIGITAL INPUT (VOLTAGE): Voltage input enables the P-C to read voltage levels from external devices. When a voltage input group is read, each positive input causes a 1-bit to be placed in the corresponding P-C word bit position, and each negative input causes a 0-bit to be placed in the corresponding P-C word bit position. Read speeds up to 500,000 words per second are possible on a 2 μs system when using a data channel and no external sync. However, repetitive reading of the same group cannot be performed at this rate and still reliably sense a change in the input status. This restriction is caused by recovery delay of the input noise filter located at each digital input point. See IBM 1800 Installation Manual -- Physical Planning, Order No. GA26-5922 for specifications.

HIGH-SPEED DIGITAL INPUT (VOLTAGE): High-speed input enables high repetitive reading speeds (up to 100,000 words per second) for input from digital registers. For example, telemetry registers may be coupled to one or more high-speed input groups. (The number of input groups depends on the register size and number coding.) Conversion of the various number bases is accomplished through programming.

High-speed telemetry receiver registers may be read without a data channel by using an external interrupt for synchronization. They may also be read using data channel operations synchronized by an external sync signal.

PULSE COUNTER ADAPTER

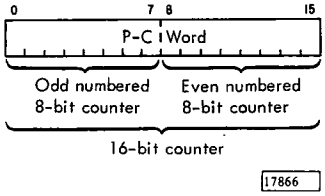
The pulse counter adapter provides control facilities for up to sixteen 8-bit pulse counters or eight 16-bit pulse counters. As many as eight pulse counter adapters may be ordered for a system, thus providing facilities for a maximum of 64 sixteen-bit or 128 eight-bit pulse counters.

Pulse Counter

The pulse counter accepts discrete pulses as input information and advances one count for each pulse received. Pulses can be accumulated at rates up to 5,000 per second.

The input pulse signal is connected via two-wire screw-down terminals at the individual counter terminal.

The pulse counter may be an 8 or 16-bit counter. The counters are read into the P-C in the format shown in the following illustration.



Two 8-bit counters (or one 16-bit counter) are read from one address. The counters are reset to zero when read.

PROCESS INTERRUPT ADAPTER

The process interrupt adapter is a prerequisite for contact type process interrupt or voltage type process interrupt and provides control facilities for up to 48 interrupt points. As many as 8 process interrupt adapters may be ordered for a system, thus providing facilities for a maximum of 384 process interrupt points.

Process Interrupt Points

Two types of process interrupt points can be ordered in modular groups of 16. The first type operates in conjunction with a customer supplied contact and is called process interrupt (contact). The second type senses the level of voltage supplied from a customer device and is called process interrupt (voltage).

An interrupt condition is generated by an off-to-on transition of an input signal and is stored in an indicator until serviced. The signal causing an interrupt cannot interrupt again until it has been serviced and the signal has completed another off-on cycle.

PROCESS INTERRUPT (CONTACT): Contact interrupt permits an interrupt to be generated by the changing status of an external contact. Sensing voltage for the contact is supplied by the 1800. Closing of the external contact causes an interrupt to be generated.

PROCESS INTERRUPT (VOLTAGE): Voltage interrupt permits an interrupt to be generated by a changing voltage level supplied by a customer device. An interrupt is generated when the input voltage changes from negative to positive (0 to 1).

DIGITAL INPUT ADDRESS ASSIGNMENT

Each 16-bit group of digital input, each 16 bits of pulse counter input, and each 16-bit group of process interrupt is assigned a specific address so that it can be selected by the program.

Digital and Pulse Counter Input Addresses

Digital input devices and pulse counters are assigned addresses from 64 through 127. This group of 64 addresses is shared by both digital input devices and pulse counters. Because each digital input adapter and pulse counter adapter uses eight addresses, the total number of digital input and pulse counter adapters cannot exceed eight, in any combination. For example, if 4 digital input adapters (32 addresses) are ordered, a maximum of 4 pulse counter adapters (32 addresses) can be ordered.

If digital input is ordered, address 64 is assigned to the first digital input group of the first digital input adapter. Address 65 is assigned to the second digital input group of the first digital input adapter. This sequence of assignment continues through address 127, which is assigned to the last digital input group of the eighth digital input adapter (Figure 45).

If pulse counters are ordered, address 127 is assigned to counters 0 and 1 (8-bit counters) or to counter 0 (16-bit counter) in the first pulse counter adapter. (There are two 8-bit counters or one 16-bit counter per address.) Address 126 is assigned to counters 2 and 3 (8-bit counters) or to counter 2 (16-bit counter) in the first pulse counter adapter. This sequence of assignment continues through

Digital Inputs		Decimal- Address	Pulse Counters	
Adapter	Group No. (16 pts. ea.)		Counter No. (2/Addr.) *	Adapter
First	0	64	15-14	Eighth
	1	65	13-12	
	2	66	11-10	
	3	67	9-8	
	4	68	7-6	
	5	69	5-4	
	6	70	3-2	
	7	71	1-0	
Second	0	72	15-14	Seventh
	1	73	13-12	
	2	74	11-10	
	3	75	9-8	
	4	76	7-6	
	5	77	5-4	
	6	78	3-2	
	7	79	1-0	
Third	0	80	15-14	Sixth
	1	81	13-12	
	2	82	11-10	
	3	83	9-8	
	4	84	7-6	
	5	85	5-4	
	6	86	3-2	
	7	87	1-0	
Fourth	0	88	15-14	Fifth
	1	89	13-12	
	2	90	11-10	
	3	91	9-8	
	4	92	7-6	
	5	93	5-4	
	6	94	3-2	
	7	95	1-0	
Fifth	0	96	15-14	Fourth
	1	97	13-12	
	2	98	11-10	
	3	99	9-8	
	4	100	7-6	
	5	101	5-4	
	6	102	3-2	
	7	103	1-0	
Sixth	0	104	15-14	Third
	1	105	13-12	
	2	106	11-10	
	3	107	9-8	
	4	108	7-6	
	5	109	5-4	
	6	110	3-2	
	7	111	1-0	
Seventh	0	112	15-14	Second
	1	113	13-12	
	2	114	11-10	
	3	115	9-8	
	4	116	7-6	
	5	117	5-4	
	6	118	3-2	
	7	119	1-0	
Eighth	0	120	15-14	First
	1	121	13-12	
	2	122	11-10	
	3	123	9-8	
	4	124	7-6	
	5	125	5-4	
	6	126	3-2	
	7	127	1-0	

*Sixteen-bit counters use even numbers (one counter number per address).

29066 B

Figure 45. Digital and Pulse Counter Input Addresses

address 64, which is assigned to counters 14 and 15 (8-bit counters) or to counter 14 (16-bit counter) in the eighth pulse counter adapter. (See Figure 45.)

Each digital input and pulse counter adapter ordered is assigned eight addresses in the manner given in the preceding paragraphs. If an adapter is ordered but is not completely populated (for example, only four groups of points are ordered for an adapter), the remainder of the eight addresses for that adapter are not available to be used in another adapter.

Process Interrupt Addresses

Input from process interrupt points is accepted via process interrupt status words (PISW's). Each PISW consists of 16 bit positions to which 16 process interrupt points may be assigned. (Assignment of process interrupt points to PISW's is described in the "Interrupt" section.)

Each PISW has its own unique address. Twenty-four PISW's (1 through 24) are available and are assigned addresses 2 through 25, respectively.

PROGRAMMED CONTROL MODES

This section describes the control modes that are available for selection and transfer of digital input data to the P-C.

Four basic modes for input of digital data are available: (1) direct program control, (2) data channel sequential, (3) data channel single address, and (4) data channel random.

Direct Program Control

Using direct program control mode of operation, one execute I/O (XIO) is used to read one input group and transfer the data to the P-C. The address of the input group is specified in the modifier field of the input/output control command (IOCC) referenced by the XIO.

An input group may be read into the accumulator or core storage. An XIO sense device reads the addressed input group into the accumulator while an XIO read transfers data to the core storage location specified by the IOCC address word.

Data Channel Sequential

Using data channel sequential mode of operation, a sequence of input groups can be read into core

storage with one XIO initialize read to initiate the action. The input/output control command (IOCC) address word contains the core storage address of a data table. The first word of the table contains the scan control bits and word count for the operation. The word count is 1 more than the number of input groups to be read. The scan control bits determine whether an interrupt is given and whether chaining or termination of the operation occurs when the word count reaches 0.

The word following the word count and scan control bits in the data table contains the initial input group address for this data table. The data channel "writes" this address into digital input basic, which then initiates reading of the input group. After the input group is read, the data is transferred by the data channel to the next sequential core storage word in the data table. Upon completion of each data transfer, the word count is decreased by 1 and the input group address is increased by 1. The new address causes the next sequential input group to be read.

This operation continues until the word count reaches 0. At this time, the scan control bits are monitored. If continuous scanning is indicated, the data channel takes four cycles to initialize for the next data table. The first cycle transfers the word following the first data table to the channel address register (CAR). This word contains the address of the next data table. The second cycle reads the first word of the next data table to the B-register. A CAR check is then made. The third cycle transfers the word count and scan control bits to digital input basic. The fourth cycle transfers the initial input group address for this data table to digital input basic. Data transfers then resume by means of data channel operations.

Figure 46 shows two data tables which could be used for chained sequential operation. In this example, the IOCC initiating the operation is at locations 3042 and 3043.

Data channel sequential mode may be used with or without external sync.

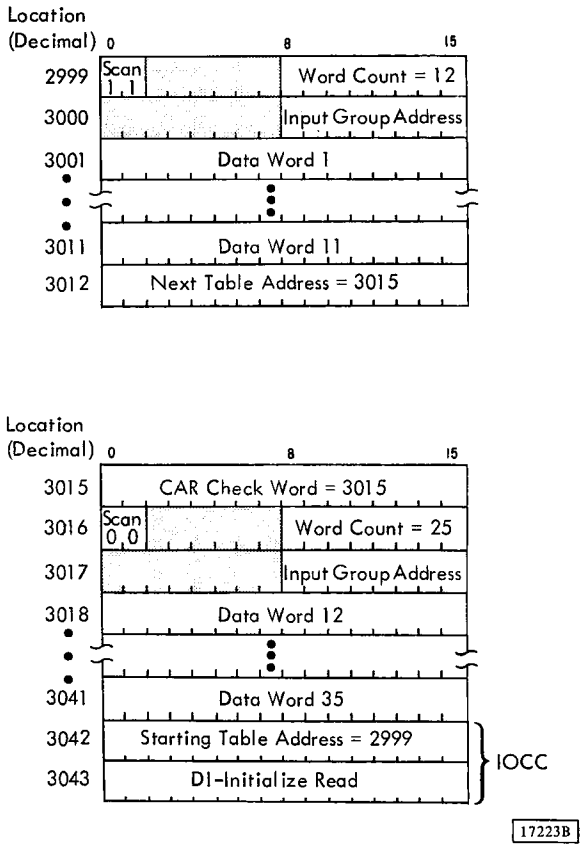


Figure 46. Digital Input Data Tables, Chained Sequential Mode

Data Channel Single Address

Data channel single address mode of operation is identical to data channel sequential mode of operation except that the initial input group address is not increased after each data transfer. Therefore, the same input group is read repeatedly. The data is placed in sequential words of the data table until the word count reaches 0.

Data channel single address mode may be used with or without external sync.

Data Channel Random

Using data channel random mode of operation, input groups can be read at random into core storage with one XIO initialize read to initiate the action. The input/output control command (IOCC) address word contains the core storage address of the data table. The first word of the table contains the scan control bits and word count for the operation. The word count is twice the number of input groups to be read.

The word following the word count and scan control bits in the data table is an input group address. The data channel "writes" this address into digital input basic, which then initiates reading of the input group. After the input group is read, the data is transferred by the data channel to the next sequential core storage word in the data table. The data channel then "writes"

the next input group address (contained in the word following the data stored) into digital input basic, which then initiates reading of the input group.

This operation continues until the word count (which is decreased by 1 for each address written and for each data word stored) reaches 0. At this time the scan control bits are monitored. If continuous scanning is indicated, the data channel takes four cycles to initialize for the next data table as described under "Data Channel Sequential".

Figure 47 shows two data tables which could be used for chained random operation. In this example, the IOCC initiating the operation is at locations 3114 and 3115.

Data channel random mode may be used with or without external sync.

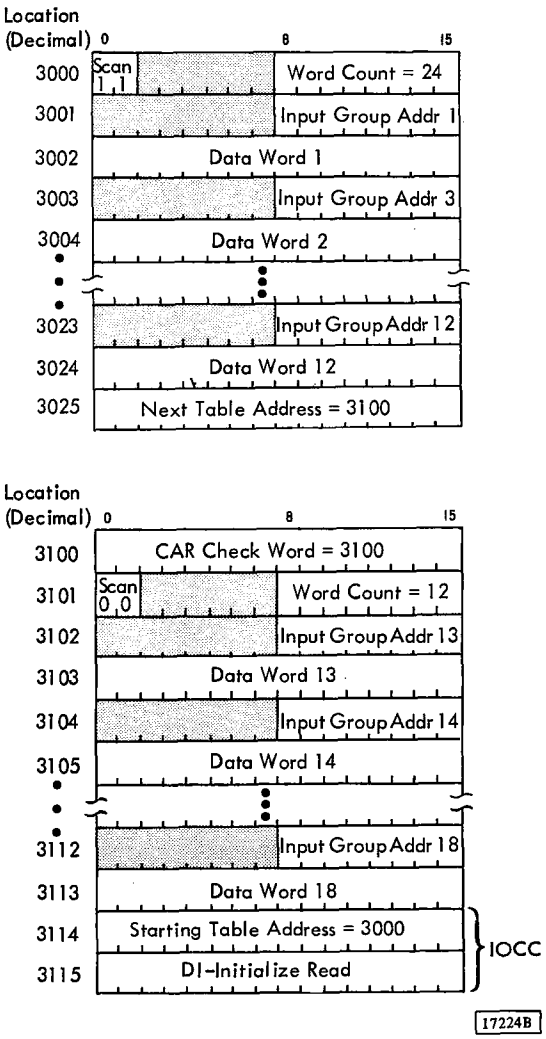


Figure 47. Digital Input Data Tables, Chained Random Mode

Overlap of Operations

Some digital input operations can be overlapped. This overlap is accomplished by using direct program control to read or sense the device status word or process interrupt status words during data channel operations with digital input groups. However, this overlap can occur only during data channel operations with external sync. Otherwise, the digital input operation is completed by means of the data channel before any P-C instructions can be executed. The following points should be considered when programming such an overlap.

- An XIO initialize read terminates the data channel operation in progress and sets command reject.
- An XIO read specifying a digital input group address (64 through 127) sets command reject and is not executed.
- An XIO read specifying a process interrupt status word address (2 through 25) sets command reject, but is executed correctly.
- A parity error causing an internal interrupt as an XIO is being executed terminates the data channel operation in progress.

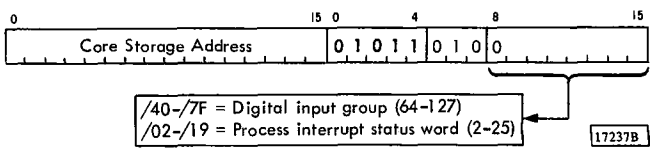
DIGITAL INPUT PROGRAMMING

Digital input features operate under direct program control or data channel control for data transfer and utilize the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO must have an area code of 01011 to address digital input features. The following IOCC's provide operation and control of digital input features.

Digital Input IOCC'S

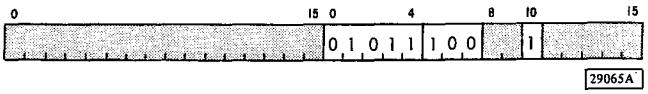
Read



This command causes the digital input group or process interrupt status word (PISW) specified by

modifier bits 8 through 15 to be read into the core storage location specified by the IOCC address word.

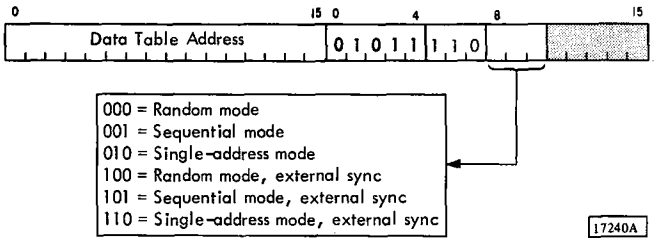
Control



This command (blast reset) can be used to immediately halt any digital input operation using external sync. All basic digital input controls and registers are reset by this command. If a digital input operation with external sync is in progress, it is terminated. As a result, digital input basic and the data channel are released for the next XIO.

During a digital input operation using a data channel and not external sync, a blast reset cannot be performed until the operation is completed because the P-C is locked out from instruction execution.

Initialize Read



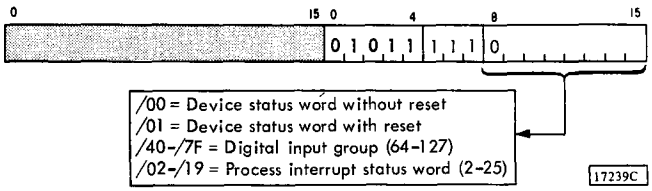
This command initializes digital input basic and the data channel in preparation for transfer of data from digital input groups to core storage. Digital input basic may be initialized to one of three modes. Operation under each mode is described under "Data Channel Sequential", "Data Channel Single Address", and "Data Channel Random".

External sync may be specified with any of the three modes of operation. It should be noted that without external sync, digital input groups are read at the maximum rate of the data channel (core storage cycle time) unless a higher priority data channel request is honored. However, timing restrictions due to filtering and customer load should be observed.

Caution should be used when chaining data tables without external sync. A digital input operation without external sync locks out the P-C until the operation is complete. Chaining data tables increases the amount of data that can be transferred by a single digital input operation; therefore, it can increase the amount of time the P-C is locked out.

Process interrupt status words (PISW's) cannot be read with this command. If a PISW is addressed, the data read for that group will be blank.

Sense Device



This command causes the digital input device status word (DSW), the digital input group, or the process interrupt status word (PISW) addressed by modifier bits 8 through 15 to be read into the accumulator.

Digital Input DSW Interrupt Indicators

Figure 48 shows the format of the digital input DSW and defines the indicators that cause interrupts. Program resettable indicators are also defined.

PARITY ERROR: This indicator turns on, causing an interrupt, if even parity is detected during data transfer to or from core storage, or if a P-C parity error is detected while chaining from one table to another in a digital input operation. A parity error terminates the operation.

STORAGE PROTECT VIOLATION: This indicator turns on, causing an interrupt, if an attempt is made to store data into a storage-protected location. This error terminates the operation.

DI (DIGITAL INPUT) SCAN COMPLETE: This indicator turns on, causing an interrupt, when the word count is decreased to 0 during data channel operations and the scan control bits specify an interrupt.

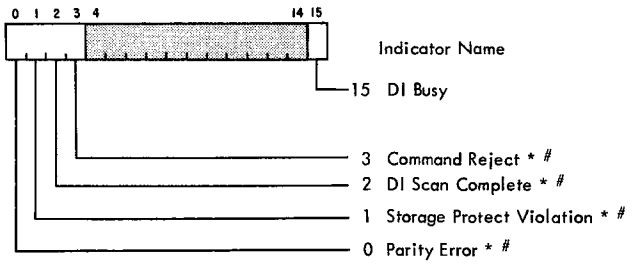
COMMAND REJECT: This indicator turns on, causing an interrupt, if an XIO read or XIO initialize read is given while the DI busy indicator is on. If an XIO read addresses a process interrupt

status word (PISW), the PISW is read correctly even though command reject is turned on.

Digital Input DSW Noninterrupt Indicators

Figure 48 shows the format of the digital input DSW and defines the noninterrupt and program resettable indicators.

DI (DIGITAL INPUT) BUSY: This indicator is on during digital input data channel operations and is off when the data channel is not busy. An XIO read or XIO initialize read given while DI busy is on causes a command reject interrupt. If an XIO read addresses a PISW, the PISW is read correctly even though command reject is turned on.



* Interrupt
\# Indicator reset by an XIO sense device with reset
(Other indicator reset by its status turnoff)

23406A

Figure 48. Digital Input Device Status Word

Digital and analog output features provide versatile control capability for the 1800 system. They enable the processor-controller (P-C) to control the many types of auxiliary devices required in a data acquisition or control system. Equipment such as set point positioners, displays, trend recorders, motor operated valves, and telemetry can be controlled by the P-C. The control outputs available are:

- Electronic "contact" operate.
- Pulse output.
- High-speed digital register output.
- High-speed analog voltage output.

Pulse chaining and pulse-duration outputs may be accomplished by programming.

Digital output (electronic "contact" operate, pulse output, and register output) is in modular groups of 16 points each. One 16-bit output register is provided for each digital output. Analog voltage output is developed from 10-bit or 13-bit digital data, depending on the model of digital-to-analog converter (DAC) used.

Both digital and analog output operations can be performed via direct program control or data channel control. With data channel control, digital and analog output operations can be synchronized by a sync pulse supplied by an external device.

Digital and analog output basic is supplied with the basic processor-controller and provides the controls and checking circuits necessary for operation of digital and analog output features.

System capacity of digital and analog output points depends on the combination of points installed. Selection begins with the digital output and analog output controls (Figure 49). A maximum of eight controls, in any combination, can be ordered for a system.

Seven digital output controls are available. One may be located within the 1801 and controls as many as eight 16-bit output registers through two digital output adapters. The six additional digital output controls are located in 1826 Data Adapter Units. Each of these controls accomodates as many as 16 output registers through four digital output adapters. (See Figure 49.) If the maximum number of digital output points is desired, all seven digital output controls are installed, thus providing 26 digital output adapters. Each adapter accumulates four 16-bit registers, giving a total of 104 registers (1,664 bits). Installation of the maximum digital output points eliminates the possibility of analog output points.

Eight analog output controls are available and are located in 1856 Analog Output Terminals. If the maximum number of analog output points is desired, all eight analog output controls are installed. Each control accomodates as many as eight digital-to-analog converters (DAC's), with a maximum of 16 output points. (See Figure 49.) (Each DAC provides one or two analog output points, depending on the model.) Thus, a maximum of 128 analog output points can be installed. Installation of the maximum analog output points eliminates the possibility of any digital output points. Installation of single point DAC's (mods 1 or 3) reduces the maximum of 128 analog output points by one for each DAC mod 1 or 3 installed.

DATA CHANNEL ADAPTER

This feature adapts digital and analog output basic to a data channel. In so doing, it provides the necessary controls for digital and analog output by means of data channel (cycle steal) operations. A word counter and scan control circuits are provided. These count the number of data transfers and specify the action to be taken after the last word in a core storage data table has been transferred to a digital output group or analog output point.

The data channel adapter also permits data transfers from core storage to digital and analog output points to be controlled by an external timing (sync) pulse.

Operation With External Sync

External sync operation is initiated by an execute I/O (XIO) initialize write with modifier bit 8 on. This causes the addressed digital output group or analog output point to be loaded with a data word from a

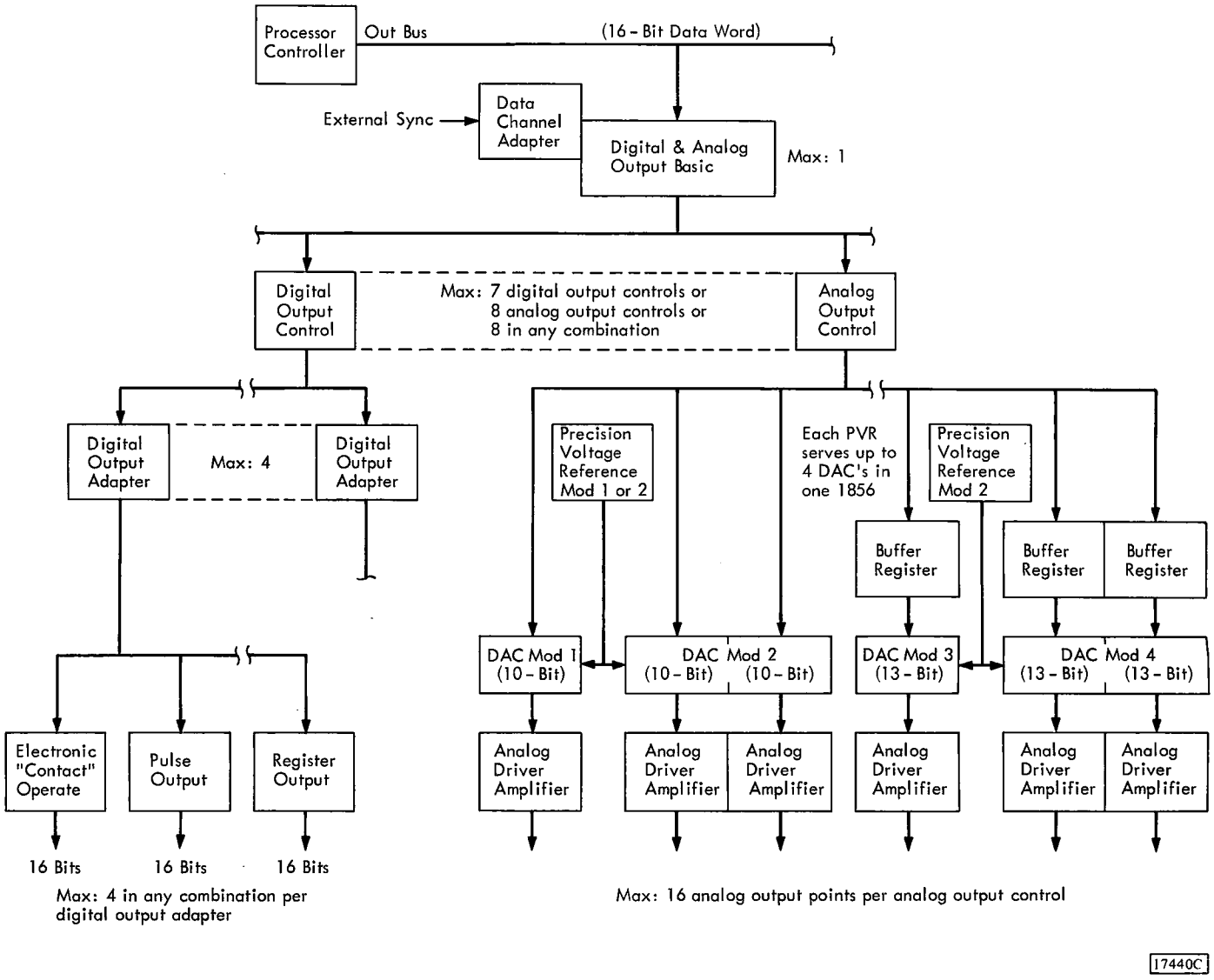


Figure 49. Digital-Analog Output Configuration

core storage data table. (The address and data word are transferred by data channel operations.) After the data word has been loaded, a ready signal indicating that data is available is sent to the external timing device. When the external device receives the ready signal, it reads the data and then sends a sync pulse to the data channel adapter. This sync pulse resets the ready signal and indicates that the external device is ready to receive more data. This indication initiates the loading of another data word by data channel operations. After this loading, a ready signal is again sent to the external device.

The ready and sync exchange continue, and the digital and analog output feature are interlocked until the word count is decreased to 0. However, the P-C program can continue to run while the digital and analog output feature is interlocked. When the word count reaches 0, the addressed output will have been loaded with the last word of the data table. A scan complete interrupt is then given if specified by the scan control bits. However, digital and analog output basic remain busy until an external sync pulse is received for the last word.

Operation Without External Sync

Operation without external sync is initiated by an XIO initialize write with modifier bit 8 off. Digital or analog output addresses are transferred to digi-

tal and analog output basic. Data words are transferred to the addressed output by means of data channel (cycle steal) operations.

The operation proceeds at the maximum rate of the data channel (core storage cycle time) unless a higher priority data channel request is honored. Once started, a digital or analog output operation without external sync continues to completion by means of continuous data channel operations. Therefore, the P-C is essentially locked out from program execution until the operation is completed.

DIGITAL OUTPUT POINTS

Three types of digital output points are available: electronic "contact" operate, pulse output, and register output. For physical planning specifications see IBM 1800 Installation Manual -- Physical Planning, Order No. GA26-5922.

Electronic "Contact" Operate

This type of digital output is used to operate alarms, console lights, and console displays as well as process equipment such as relays, solenoid valves, and dc motors. Electronic "contact" operate is available in modular groups of 16 points up to the system limit of 104 groups. The 16 points of a group are set by a data transfer from core storage to the 16-bit register for the group. Once set, the information in the output register remains until changed by another data transfer to that group.

A data bit of 1 corresponds to closed (conducting); a data bit of 0 corresponds to open (nonconducting). The 16 output points (0 through 15) correspond to core storage word bit positions 0 through 15, respectively.

Process operator console output devices such as lights, digital displays, and other low speed devices can be operated by using a single electronic "contact" operate group as an output channel to the devices. Process operator console devices and cabling are available on a Request for Price Quotation (RPQ) basis.

Pulse Output

This type of digital output is used primarily to provide pulse trains for operation of devices such as electronic latches, set point positioners, and other stepping motor devices. Pulse output is available in modular groups of 16 points up to the system limit of 104 groups. The 16 points of a group are set by a data transfer from core storage to the 16-bit register for the group.

A data bit of 1 corresponds to closed (conducting); a data bit of 0 corresponds to open (nonconducting). The 16 output points (0 through 15) correspond to core storage word bit positions 0 through 15, respectively. Pulse output is similar to electronic "contact" operate except for duration of the contact closure.

The 16 output points of each group are immediately set to their respective conditions (open or closed) when the output register for each group is loaded. Output points in all groups are simultaneously reset (opened) by the timeout of a 3-ms timer. The timer is started by using a separate XIO control. In this manner, pulse chains are accomplished by programming.

The effective duration of the contact closure can be increased by loading the 16-bit register before the 3-ms timer is started. Likewise, this duration can be decreased by loading the register after the timer is started.

Register Output

This type of digital output is used in register-to-register transfer applications, such as transferring data from the P-C to telemetry registers. Register output is available in modular groups of 16 points each up to the system limit of 104 groups. The 16 points of a group are set by data transfer from core storage to the 16-bit output register for the group. The 16 output points (0 through 15) correspond to core storage word bit positions 0 through 15, respectively.

Once set, the information in the output register remains until changed by another data transfer.

IBM 1856 ANALOG OUTPUT TERMINAL

The 1856 Analog Output Terminal is a modular chasis in which analog output control and digital-to-analog converters (DAC's) are housed. The 1856 is mounted in an 1828 Enclosure. Up to sixteen 1856's can be installed in an 1800 system.

Two models of the 1856 exist. Model 1 provides housing and power for as many as four DAC's and one analog output control. The analog output control operates as many as eight DAC's. Model 2 provides housing and power for as many as four DAC's, but does not contain an analog output control. The DAC's in a model 2 are controlled by analog output control in the model 1. Therefore, a model 1 is required for each model 2.

DIGITAL-TO-ANALOG CONVERTER (DAC)

The digital-to-analog converter (DAC) develops analog voltage output from digital input values. A precision reference voltage is required to supply the

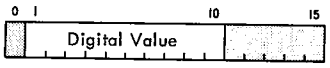
DAC reference voltage used in developing the analog output voltage. The DAC contains a register used to hold the digital value being converted. This output register is loaded by a data transfer from core storage. As the register is loaded, the DAC converts the digital value and provides the corresponding analog output voltage. The output remains until the register is changed by another data transfer. During data transfer from core storage, the output register is force loaded to minimize DAC switching transients. Force load means that the register goes directly from the previous value to the new value without being reset to 0 in between.

Four DAC mods (1, 2, 3, and 4) are available to provide two basic types of analog voltage output.

DAC Mod 1 and Mod 2

DAC's mod 1 and mod 2 provide unipolar analog voltage output from ten-bit digital input. This analog voltage output is suitable for operating analog controllers, strip chart recorders, and other displays. The mod 1 provides one analog output point. Therefore, a maximum system configuration populated with mod 1 DAC's provides 64 analog output points. The mod 2 has two separate digital-to-analog converters in one housing and two analog output points. A maximum system configuration populated with mod 2 DAC's provides 128 analog output points.

The format of the ten-bit digital data sent from core storage for conversion is:



10-Bit Resolution Format

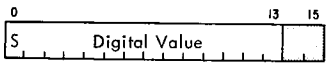
17878

DAC Mod 3 and Mod 4

DAC's mod 3 and mod 4 provide bipolar analog voltage output suitable for hybrid systems. This output is obtained from digital input consisting of 13 bits plus sign. Negative digital input values are handled in 2's complement form.

Mod 3 provides one analog output point. Therefore, a maximum system configuration populated with mod 2 DAC's provides 64 analog output points. Mod 4 has two separate digital-to-analog converters in one housing and two analog output points. A maximum system configuration populated with mod 4 DAC's provides 128 analog output points.

The format of the 13-bit (plus sign) digital data sent from core storage for conversion is:



13-Bit Resolution Format

17879

It is frequently a requirement in hybrid computing and often an advantage in other applications to furnish output at several analog output points simultaneously. By using an optional buffer register for each of these analog output points, the buffers can be preloaded as data is received from the P-C. After the buffers are loaded, an execute I/O (XIO) control with modifier bit 9 on is executed, causing all DAC registers to be simultaneously loaded directly from their buffer registers.

Precision Voltage Reference

The precision voltage reference (PVR) feature is required to supply the DAC reference voltage. Each feature can supply up to eight analog output points and is available in two models.

The mod 1 precision voltage reference is used with mod 1 or mod 2 DAC's to provide ten-bit resolution unipolar analog output. The mod 2 precision voltage reference is normally used with mod 3 or mod 4 DAC's to provide 13-bit resolution bipolar analog output. The mod 2 precision voltage reference may be used with mod 1 or mod 2 DAC's when it is desired to mix the two kinds of output in a single 1856 Analog Output Terminal. However, it is more economical to use the mod 1 for each full group of eight ten-bit resolution unipolar output points.

Analog Output Driver Amplifier

The analog output driver amplifier is an optional feature that can be installed on each analog output point. This amplifier provides a ±10 volt analog output signal and permits operation of an analog output point with a wide range of load impedances. The output impedance of the DAC's is 10,000 ohms. To match loads differing greatly from this value, an analog output driver amplifier with an output impedance of less than 0.6 ohm may be used. The analog output driver amplifier may also be used to increase the DAC output from its normal 5 volts to 10 volts.

DIGITAL AND ANALOG OUTPUT ADDRESSING

Digital and analog output points share a group of addresses. The decimal range of addresses is 0 through 127.

As shown in Figure 50, each digital output control ordered is assigned 16 addresses beginning with address 127 for the first group of 16 points. Address

Decimal - Address (Modifiers)				Analog Output			
Digital Output				DAC Mod		DAC No. within 1856	1856
Digital Output Control	Digital Output Adapter	Group No. (16 points each)		2 or 4 Output	1 or 3 Output		
Addresses 00 - 15 not available for digital output			00	1st	1st	1	1st (Model 1)
			01	2nd			
			02	1st	1st	2	
			03	2nd			
			04	1st	1st	3	
			05	2nd			
			06	1st	1st	4	
			07	2nd			
			08	1st	1st	1	2nd (Model 2)
			09	2nd			
			10	1st	1st	2	
			11	2nd			
			12	1st	1st	3	
			13	2nd			
			14	1st	1st	4	
			15	2nd			
*7	28	3	16	1st	1st	1	3rd (Model 1)
		2	17	2nd			
		1	18	1st	1st	2	
		0	19	2nd			
	27	3	20	1st	1st	3	
		2	21	2nd			
		1	22	1st	1st	4	
		0	23	2nd			
	26	3	24	1st	1st	1	4th (Model 2)
		2	25	2nd			
		1	26	1st	1st	2	
		0	27	2nd			
	25	3	28	1st	1st	3	
		2	29	2nd			
		1	30	1st	1st	4	
		0	31	2nd			
6	24	3	32	1st	1st	1	5th (Model 1)
		2	33	2nd			
		1	34	1st	1st	2	
		0	35	2nd			
	23	3	36	1st	1st	3	
		2	37	2nd			
		1	38	1st	1st	4	
		0	39	2nd			
	22	3	40	1st	1st	1	6th (Model 2)
		2	41	2nd			
		1	42	1st	1st	2	
		0	43	2nd			
	21	3	44	1st	1st	3	
		2	45	2nd			
		1	46	1st	1st	4	
		0	47	2nd			
5	20	3	48	1st	1st	1	7th (Model 1)
		2	49	2nd			
		1	50	1st	1st	2	
		0	51	2nd			
	19	3	52	1st	1st	3	
		2	53	2nd			
		1	54	1st	1st	4	
		0	55	2nd			
	18	3	56	1st	1st	1	8th (Model 2)
		2	57	2nd			
		1	58	1st	1st	2	
		0	59	2nd			
	17	3	60	1st	1st	3	
		2	61	2nd			
		1	62	1st	1st	4	
		0	63	2nd			

Decimal - Address (Modifiers)				Analog Output			
Digital Output				DAC Mod		DAC No. within 1856	1856
Digital Output Control	Digital Output Adapter	Group No. (16 points each)		2 or 4 Output	1 or 3 Output		
4	16	3	64	1st	1st	1	9th (Model 1)
		2	65	2nd			
		1	66	1st	1st	2	
		0	67	2nd			
	15	3	68	1st	1st	3	
		2	69	2nd			
		1	70	1st	1st	4	
		0	71	2nd			
	14	3	72	1st	1st	1	10th (Model 2)
		2	73	2nd			
		1	74	1st	1st	2	
		0	75	2nd			
	13	3	76	1st	1st	3	
		2	77	2nd			
		1	78	1st	1st	4	
		0	79	2nd			
3	12	3	80	1st	1st	1	11th (Model 1)
		2	81	2nd			
		1	82	1st	1st	2	
		0	83	2nd			
	11	3	84	1st	1st	3	
		2	85	2nd			
		1	86	1st	1st	4	
		0	87	2nd			
	10	3	88	1st	1st	1	12th (Model 2)
		2	89	2nd			
		1	90	1st	1st	2	
		0	91	2nd			
	9	3	92	1st	1st	3	
		2	93	2nd			
		1	94	1st	1st	4	
		0	95	2nd			
2	8	3	96	1st	1st	1	13th (Model 1)
		2	97	2nd			
		1	98	1st	1st	2	
		0	99	2nd			
	7	3	100	1st	1st	3	
		2	101	2nd			
		1	102	1st	1st	4	
		0	103	2nd			
	6	3	104	1st	1st	1	14th (Model 2)
		2	105	2nd			
		1	106	1st	1st	2	
		0	107	2nd			
	5	3	108	1st	1st	3	
		2	109	2nd			
		1	110	1st	1st	4	
		0	111	2nd			
1	**4	3	112	1st	1st	1	15th (Model 1)
		2	113	2nd			
		1	114	1st	1st	2	
		0	115	2nd			
	**3	3	116	1st	1st	3	
		2	117	2nd			
		1	118	1st	1st	4	
		0	119	2nd			
	2	3	120	1st	1st	1	16th (Model 2)
		2	121	2nd			
		1	122	1st	1st	2	
		0	123	2nd			
	1	3	124	1st	1st	3	
		2	125	2nd			
		1	126	1st	1st	4	
		0	127	2nd			

29067 B

* Not available when the first digital output control is in 1826.

** Not available when the first digital output control is in 1801.

Figure 50. Digital and Analog Output Addresses

126 is assigned to the second group of 16 points. This sequence of assignment continues through address 16, which is assigned to the last group of 16 points (in the seventh digital output control).

The first and all odd numbered 1856 Analog Output Terminals ordered must be mod 1. The second and all even numbered 1856's must be mod 2. Each 1856 mod 1 supplies controls and addressing for the next higher numbered 1856 mod 2. Sixteen addresses are assigned for each 1856 mod 1 ordered. Eight addresses are designated for the mod 1, and another eight are designated for the next higher numbered mod 2. If the mod 2 is not ordered, the addresses designated for it are not available for use by digital output groups.

As shown in Figure 50, addresses 00 through 15 are assigned to the first 1856 mod 1 and its corresponding mod 2; addresses 16 through 31 are assigned to the second 1856 mod 1 and its corresponding mod 2. This sequence of assignment continues through addresses 112 through 127, which are assigned to the eighth 1856 mod 1 and its corresponding 1856 mod 2.

PROGRAMMED CONTROL MODES

This section describes the control modes available for digital and analog output operation. These basic control modes are available: (1) direct program control, (2) data channel single address, and (3) data channel random.

Direct Program Control

Using direct program control mode of operation, one execute I/O (XIO) write is used to transfer one word of data from core storage to a digital output group or analog output point. The address of the digital output group or analog output point is specified in the modifier field of the write input/output control command (IOCC). The core storage address of the data word is specified by the address word of the write IOCC.

XIO control may be used with direct program control to reset all pulse output registers simultaneously. This feature is useful in generating pulse trains and for transmitting pulse duration signals to many devices simultaneously. XIO control is also used to transfer the contents of all optional buffer registers to their respective DAC's, thereby permitting simultaneous analog output over a group of points.

Data Channel Single Address

In data channel single address mode of operation, a series of data words can be transferred from core storage to one digital output group or analog output point -- with only one XIO initialize write initiating the action. The input/output control command (IOCC) address word contains the core storage address of a data table. The first word of the table contains the scan control bits and word count for the operation. The word count is 1 more than the number of data words to be transferred.

The word following the word count and scan control bits in the data table contains the digital output group or analog output point address for this data table. The data channel "writes" this address into digital and analog output basic. Once the address has been transferred, data word transfer to the addressed digital output group or analog output point proceeds by means of data channel (cycle steal) operation. If external sync is not specified, data words are transferred to the output group or point at the maximum rate of the data channel (core storage cycle time) unless a higher-priority data channel request is honored.

The data word transfer operation continues until the word count is decreased to 0. At this time, the scan control bits are monitored. If continuous scanning is indicated, the data channel takes four cycles to initialize for the next data table. The first cycle transfers the word following the first data table to the channel address register (CAR). This word contains the address of the next data table. The second cycle reads the first word of the next data table to the B-register. A CAR check is then made. The third cycle transfers the word count and scan control bits to digital and analog output basic. The fourth cycle transfers the digital output group or analog output point address for this data table to digital and analog output basic. Data word transfers then resume by means of data channel operations.

Figure 51 shows two data tables which could be used for chained single address operation. In this example, the IOCC initiating the operation is at locations 3042 and 3043.

Data Channel Random

In data channel random mode of operation, digital output groups or analog output points can be addressed randomly and a data word sent to each addressed group or point -- with only one XIO initialize write initiating the action. The input/output

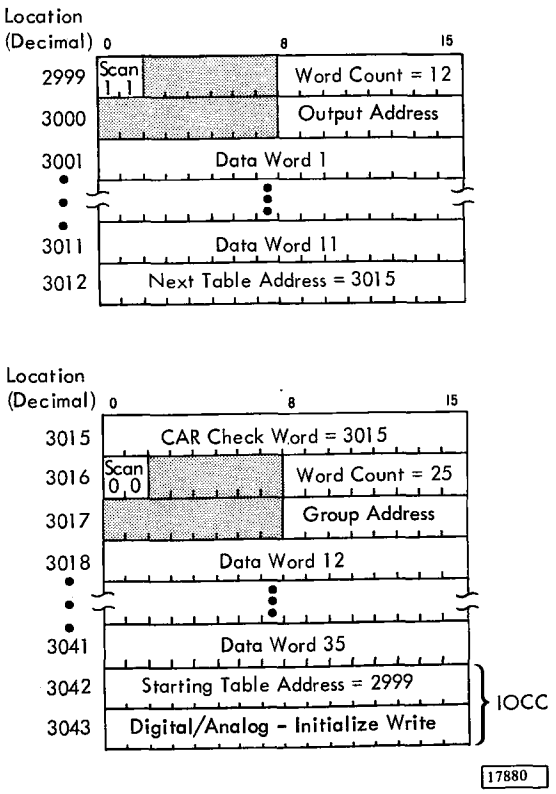


Figure 51. Digital/Analog Output Data Tables, Chained Single Address Mode

control command (IOCC) address word contains the address of a data table. The first word of the data table contains the scan control bits and word count for the operation. The word count is twice the number of data words to be transferred.

The word following the scan control bits and word count in the data table is a digital output group or analog output point address. The data channel "writes" this address into digital and analog output basic. After the address has been transferred, the data channel transfers the data word following the address in the data table to the addressed output group or point.

This operation continues, alternately transferring addresses and data until the word count (which is decreased by 1 for each address and each data word transferred) reaches 0. At this time, the scan control bits are monitored. If continuous scanning is indicated, the data channel takes four cycles to initialize for the next data table as described under "Data Channel Single Address".

If external sync is not specified, data transfer with this mode of operation is at the maximum rate of the data channel (core storage cycle time) unless a higher-priority data channel request is honored.

Figure 52 shows two data tables that could be used for chain random operation. In this example, the IOCC initiating the operation is at locations 3114 and 3115.

DIGITAL AND ANALOG OUTPUT PROGRAMMING

Digital and analog output features operate under direct program control or data channel control for data transfer. They utilize the execute I/O (XIO) instruction.

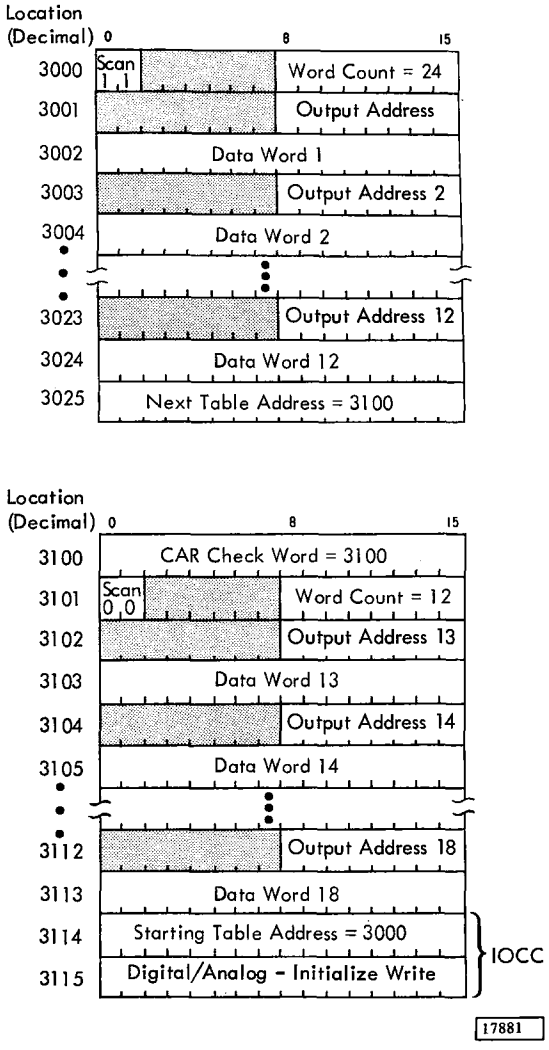
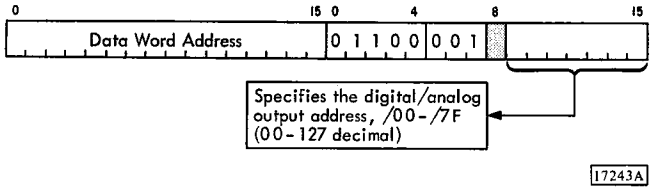


Figure 52. Digital/Analog Output Data Tables, Chained Random Mode

The input/output control command (IOCC) referenced by an XIO must have an area code of 01100 to address digital and analog output features. The following IOCC's provide operation and control of digital and analog output features.

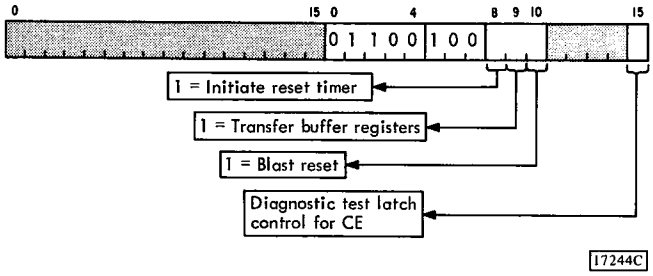
Digital and Analog Output IOCC's

Write



This command causes the data word in the core storage location specified by the IOCC address word to be transferred to the digital output group or analog output point specified by modifier bits 9 through 15.

Control



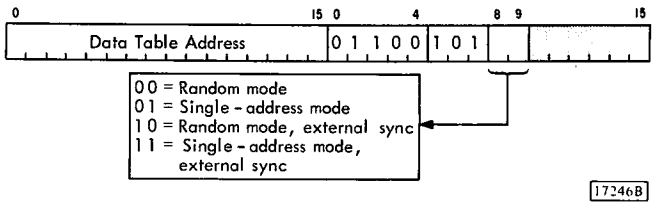
This command may be used to perform the three functions indicated in the preceding illustration, and described next.

INITIATE RESET TIMER: This function starts the 3-ms pulse output timer. When the 3-ms time period expires, all pulse output points are reset. This function is used in conjunction with pulse output points to provide pulse trains and pulse-duration signals.

TRANSFER BUFFER REGISTERS: This function is used in conjunction with analog output points having the optional buffer register features. The contents of all buffer registers are simultaneously transferred to their respective digital-to-analog converters by this function.

BLAST RESET: This function can be used to immediately halt any digital or analog output operations using external sync. All basic digital and analog output controls are reset by this command. (Digital output and analog output registers are not reset.) If a digital or analog output operation with external sync is in progress, it is terminated thus making digital and analog output basic and the data channel available for another XIO.

Initialize Write

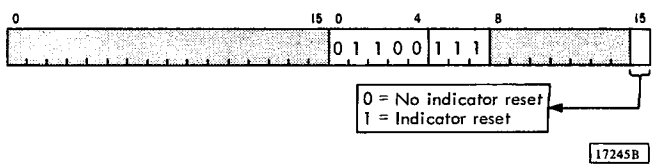


This command initializes digital and analog input basic and the data channel. This initialization prepares for the transfer of data words from core storage to digital/analog output points. Digital and analog output basic may be initialized to one of two modes. Operation under each mode is described under "Data Channel Single Address" and "Data Channel Random".

External sync may be specified with either mode. Without external sync, digital or analog output occurs at the maximum rate of the data channel (core storage cycle time) unless a higher-priority data channel request is honored. The actual output data rate to customer devices must be limited, if necessary, to the device characteristics and the repetition rate allowed by the devices to the same output or to single outputs. The rate can be controlled either by external sync operation or by programming.

Caution should be used when chaining data tables without external sync. A digital or analog output operation without external sync locks out the P-C until the operation is complete. Chaining data tables increases the amount of data that can be transferred by a single output operation; therefore, it can increase the amount of time the P-C is locked out.

Sense Device



This command causes the digital and analog output device status word (DSW) to be read into the accumulator.

Modifier bit 15 controls reset of the DSW indicators that can be reset by the program. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset.

Digital/Analog Output DSW Interrupt Indicators

Figure 53 shows the format of the digital and analog output DSW and defines the indicators that cause interrupts. Program resettable indicators are also defined.

PARITY ERROR: This indicator turns on, causing an interrupt, if even parity is detected during data transfer to or from core storage, or if a P-C parity error is detected while chaining from one table to another during a digital or analog output operation. A parity error terminates the operation.

DAO (DIGITAL/ANALOG OUTPUT) SCAN COMPLETE: This indicator turns on, causing an interrupt, when the word count is decreased to 0 during data channel operations and the scan control bits specify an interrupt.

COMMAND REJECT: This indicator turns on, causing an interrupt, if an XIO write or XIO initialize write is given while the DAO busy indicator is on.

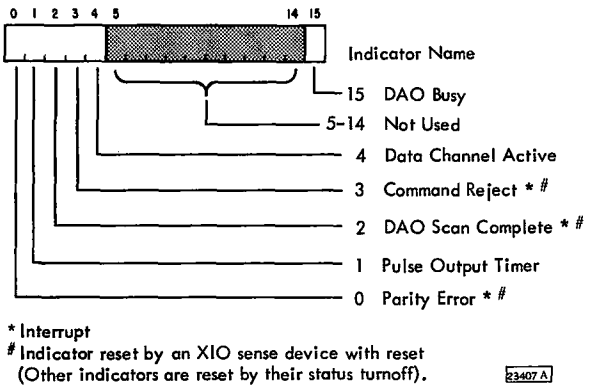


Figure 53. Digital/Analog Output Device Status Word

Digital/Analog Output DSW Noninterrupt Indicators

Figure 53 shows the format of the digital and analog output DSW and defines the noninterrupt and program resettable indicators.

PULSE OUTPUT TIMER: This indicator is on whenever the pulse output timer is on.

DATA CHANNEL ACTIVE: This indicator is on when the data channel is busy during a digital or analog output operation. The indicator turns off when the data channel is released from the operation (last word of last data table has been transferred). In external sync operations, the data channel is released after the last word is transferred, but before the last external sync pulse is received. Therefore, data channel active turns off but DAO busy remains on until the last external sync pulse is received. In operations without external sync, data channel active and DAO busy turn off at the same time.

DAO (DIGITAL/ANALOG OUTPUT) BUSY: This indicator turns on when digital/analog output is in use on a data channel. It is turned off by either of two conditions: (1) in an operation without external sync, the last word of the last data table has been transferred, or (2) in an operation with external sync, the sync pulse acknowledging receipt of the last data word of the last table has been received. DAO busy and data channel active turn off at the same time in operations without external sync.

IBM 1053 Printer and IBM 1816 Printer-Keyboard

The IBM 1053 Printer (Figure 54) provides printed output for the 1800 system.

The IBM 1816 Printer-Keyboard (Figure 55) provides console keyboard entry and console printer output. The printer portion of the 1816 is physically and functionally the same as the 1053. Therefore, the printer description and programming are the same for the two units.

Any one of three maximum configurations of 1053's and 1816's can be attached to the system:

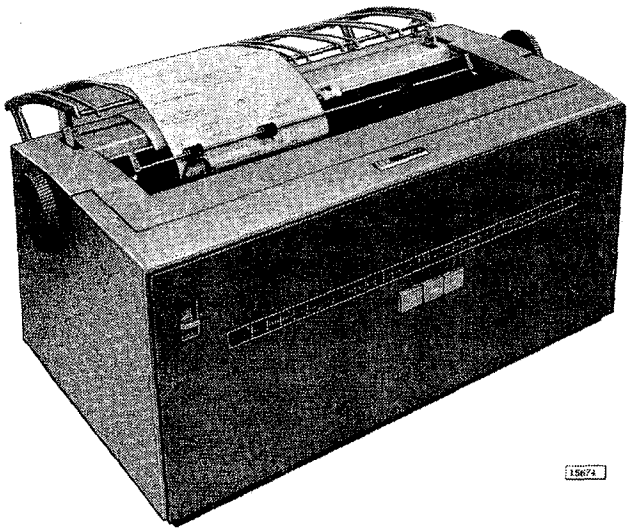


Figure 54. IBM 1053 Printer

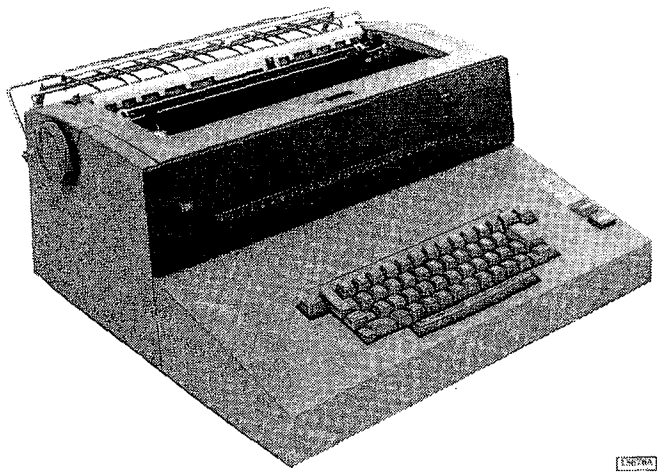


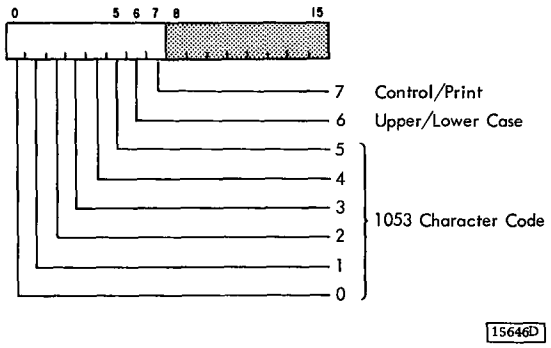
Figure 55. IBM 1816 Printer-Keyboard

(1) six 1053's and two 1816's, (2) seven 1053's and one 1816, or (3) eight 1053's.

PRINTER FUNCTIONAL DESCRIPTION

The printer (1053/1816) operates under direct program control and provides output at a maximum rate of 14.8 characters per second. Data and control characters (space, tabulate, and so on) are sent to the printer by means of the XIO write instruction. Because data and control characters are sent to the printer in the same manner, a message to be printed contains a mixture of both of these types of characters. These characters are in a certain sequence -- the one necessary to give the desired formatted output.

The character format within a core storage word to be transmitted to the printer is:



Each word transferred to the printer contains one data or control character. The control characters provide a means of programming print line format. For example, the carrier return control character is used at the end of a print line to return the carrier to the left margin. If a carrier return is not given, data will in some cases be overprinted in the last column of the print line until a carrier return is given. Therefore a carrier return should be given at the end of each print line.

All printers can operate in overlapped mode; that is, each one can print a different message at the same time, or they can all print the same message simultaneously from the same instruction.

Printer Character Coding

Data to be printed by the printer is converted to typewriter character code by the program. Figure 56

						Lower Case		Upper Case		
B0	B1	B2	B3	B4	B5	B6=0	Hexadecimal	B6=1	Hexadecimal	B7
0	0	1	1	1	1	a	3C	A	3E	0
0	0	0	1	1	0	b	18	B	1A	0
0	0	0	1	1	1	c	1C	C	1E	0
0	0	1	1	0	0	d	30	D	32	0
0	0	1	1	0	1	e	34	E	36	0
0	0	0	1	0	0	f	10	F	12	0
0	0	0	1	0	1	g	14	G	16	0
0	0	1	0	0	1	h	24	H	26	0
0	0	1	0	0	0	i	20	I	22	0
0	1	1	1	1	1	j	7C	J	7E	0
0	1	0	1	1	0	k	58	K	5A	0
0	1	0	1	1	1	l	5C	L	5E	0
0	1	1	1	0	0	m	70	M	72	0
0	1	1	1	0	1	n	74	N	76	0
0	1	0	1	0	0	o	50	O	52	0
0	1	0	1	0	1	p	54	P	56	0
0	1	1	0	0	1	q	64	Q	66	0
0	1	1	0	0	0	r	60	R	62	0
1	0	0	1	1	0	s	98	S	9A	0
1	0	0	1	1	1	t	9C	T	9E	0
1	0	1	1	0	0	u	B0	U	B2	0
1	0	1	1	0	1	v	B4	V	B6	0
1	0	0	1	0	0	w	90	W	92	0
1	0	0	1	0	1	x	94	X	96	0
1	0	1	0	0	1	y	A4	Y	A6	0
1	0	1	0	0	0	z	A0	Z	A2	0
1	1	1	1	1	1	1	FC	(	FE	0
1	1	0	1	1	0	2	D8	+	DA	0
1	1	0	1	1	1	3	DC	<	DE	0
1	1	1	1	0	0	4	F0	¬	F2	0
1	1	1	1	0	1	5	F4	)	F6	0
1	1	0	1	0	0	6	D0	;	D2	0
1	1	0	1	0	1	7	D4	*	D6	0
1	1	1	0	0	1	8	E4	'	E6	0
1	1	1	0	0	0	9	E0	"	E2	0
1	1	0	0	0	1	0	C4	|	C6	0
1	1	0	0	0	0	#	C0	=	C2	0
1	0	1	1	1	1	/	BC	_	BE	0
1	0	0	0	0	1	-	84	?	86	0
1	0	0	0	0	0	,	80	:	82	0
0	1	0	0	0	1	&	44	>	46	0
0	1	0	0	0	0	$	40	!	42	0
0	0	0	0	0	1	@	04	%	06	0
0	0	0	0	0	0	.	00	¢	02	0

Chart is for 952 print element. The 969 element is normally shipped with machine and has all capitals.

25198B

Figure 56. 1053/1816 Printer Character Codes

shows the characters that can be printed by the print element designed for use with the 1800 system, and their respective codes.

Bit position 6 of the character code determines whether the character is uppercase shift or lowercase shift. The printer shifts only when instructed to do so, and it remains in the most recently specified case until instructed to shift again. This fact can be very important. For example, the numeric characters 0 through 9 are lowercase shift. Therefore, when the output data is alphameric, the alphabetic characters should all be lowercase to avoid shifting. Each shift would add 60 to 70 ms to the print time.

In Figure 56, note that bit position 7 is off for all data characters. When bit 7 is on in an output character, the character is interpreted as a control character. Control character codes and their respective functions are shown in Figure 57.

PRINTER PROGRAMMING

The printers operate under direct program control, utilizing the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO must have area and modifier bit combinations as shown in the following illustration to address a specific printer.

Area Code	Modifier Bits			
	11	12	13	14
00001	4th Printer	3rd Printer	2nd Printer	1st Printer
01111	8th Printer	7th Printer	6th Printer	5th Printer

May be 1816 or 1053

17867

Printers 1 and 5 may be either 1816's or 1053's. Printers 2 through 4 and 6 through 8 are 1053's.

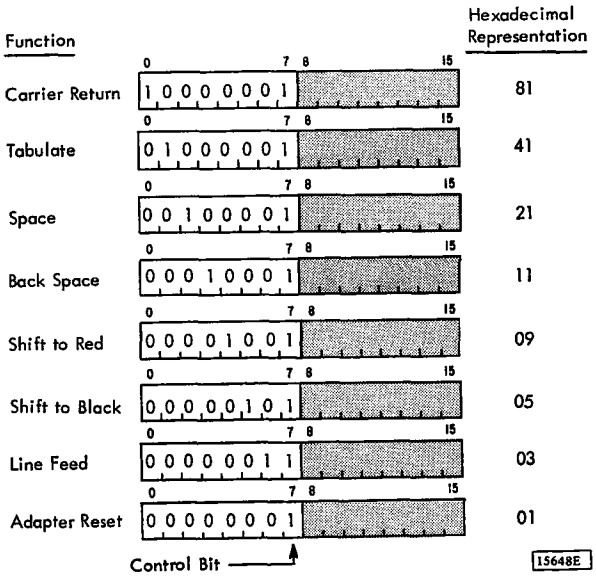
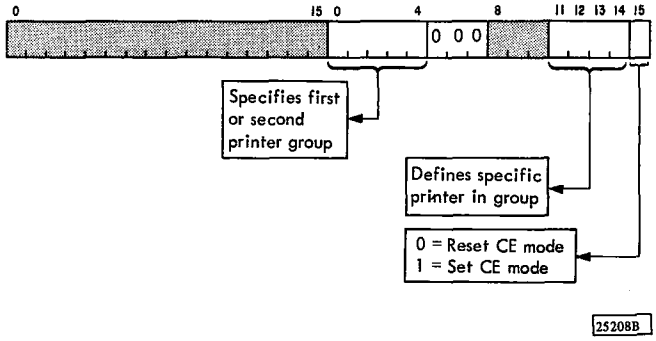


Figure 57. 1053/1816 Control Character Codes

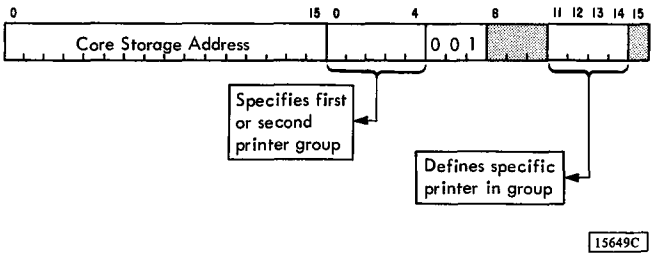
1053/1816 Printer IOCC's

CE Mode



This command places the specified printers (and keyboard if 1816 is specified) in CE mode if modifier bit 15 is on, or removes them from CE mode if modifier bit 15 is off. More than one printer may be specified at a time. If no printer is specified, the command performs as a no-op.

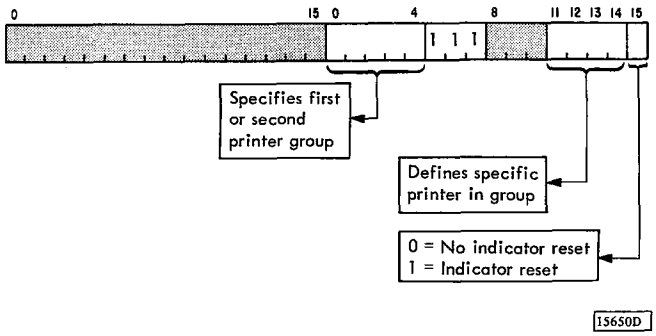
Write



This command causes the word at the core storage location specified by the IOCC address word to be sent to the specified printer for printing or control.

If more than one printer is specified, all those addressed will print the same data or perform the same control function simultaneously. If no printer is specified the command performs as a no-op.

Sense Device



This command causes the device status word (DSW) of the specified printer to be placed in the accumulator (A). If more than one printer is specified, the DSW's for the specified printers are ORed together and then placed in the accumulator.

Modifier bit 15 controls reset of the program resettable indicators in the selected printers. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset.

There is one DSW for each 1053 (Figure 58), and one for each 1816 (Figure 61). It should be noted that if an 1816 is specified, the indicator bits for the console keyboard are also ORed into the DSW. Therefore, the DSW in the accumulator will appear as shown in Figure 61.

1053 DSW Interrupt Indicators

Only one interrupt indicator is associated with each printer. All printers within a group of four (1 through 4, or 5 through 8) must be assigned to the same priority interrupt level. Furthermore, each printer within the group must have its DSW interrupt indicator assigned to a unique bit position in the interrupt level status word. Figure 58 shows the format of the 1053 DSW and defines the interrupt indicators. Program resettable indicators are also defined.

PRINTER SERVICE RESPONSE: This indicator turns on, causing an interrupt, each time a printer has completely printed the character or performed the control function sent by the last XIO write.

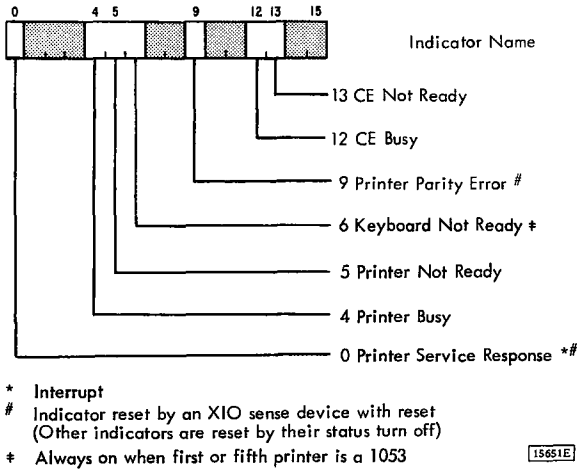


Figure 58. 1053 Device Status Word

The printer service response must be turned off by a sense DSW with reset after the print operation is completed and before another print operation is initiated.

1053 DSW Noninterrupt Indicators

Figure 58 shows the 1053 DSW format and defines noninterrupt and program resettable indicators.

PRINTER BUSY: When on, this indicator shows that the printer is in the process of printing a character or performing a control function and should not be given another XIO write. This indicator turns on at the time data is sent to the printer and remains on until the printer has completed the action required.

Whenever printer busy is on, printer not ready is also on.

PRINTER NOT READY: When off, this indicator shows that the printer is properly loaded with forms, has dc power, is not in CE mode, and is not busy.

Usually, the program must determine that printer not ready (or CE not ready) is off before an XIO write is given.

Note: If an XIO write is given while a printer is busy and/or not ready, loss of information or repetitive print of the last character transmitted will occur. No indication of the information loss will be given.

One exception to the preceding rule is an XIO write with an adapter reset control character. This control character causes a blast reset to the adapter. If printer not ready is a result of a busy condition, the busy condition is reset and the printer becomes available for another XIO operation. If printer not ready is a result of a condition other than busy, the adapter reset control character performs no useful function.

If printer not ready is tested and found to be on, printer busy should then be tested. If printer busy is off, operator intervention is required unless the printer is in CE mode. However, printer not ready on with printer busy on indicates that the printer has not completed the function specified by the previous XIO. If a malfunction prevents completion of an operation, the printer and adapter are locked in a busy and not ready condition. To clear this condition, an XIO write with an adapter reset control character is required. However, the program must ensure that enough time is allowed for the previous operation to be completed before a reset is given. Otherwise, an operation may be prematurely terminated. Carrier return is the worst-case operation; it may require as much as 2 seconds for completion.

PRINTER PARITY ERROR: This indicator is turned on when a parity error is detected in the character received from the P-C.

CE BUSY: When the printer is in CE mode, this indicator is used in place of the printer busy indicator. All conditions defined in the printer busy status are applicable to this indicator in CE mode only. Programs utilizing CE mode use this indicator instead of the printer busy indicator.

CE NOT READY: When the printer is in CE mode, this indicator is used in place of both the keyboard not ready and the printer not ready indicators. All conditions defined for both indicators are applicable to this indicator in CE mode only. Programs utilizing the CE mode use this indicator instead of printer not ready or keyboard not ready indicators.

KEYBOARD FUNCTIONAL DESCRIPTION

The input speed of the 1816 Printer-Keyboard is 20 characters per second, but is usually limited by the speed of the operator. The keyboard operates under direct program control.

When a key is struck by the operator, the keyboard emits a coded character representing the key, and a keyboard service response interrupt is generated. The keyboard service response interrupt signals the program that a character is ready to be read into core storage. A subsequent XIO read transfers the character into core storage.

Keyboard entries are not printed automatically. The P-C must be programmed to provide output on the printer for each keyboard entry. Conversion from the keyboard input character code to the printer output character code must also be accomplished by the program.

Keyboard Character Coding

Keyboard input character codes, as they appear in core storage, are related to IBM card code. Figure 59 shows the various characters, their hexadecimal codes, the corresponding card codes, and the bit formats in core storage.

Keyboard Functional Keys

The arrangement of the various keyboard keys is shown in Figure 60. The power on switch (not shown in Figure 60) located on the 1816 front panel should be left on at all times for printer operation.

REST KBD (Restore Keyboard): This key allows the operator to restore the keys if they should become interlocked. System reset from the P-C console also restores the keyboard.

KBD REQ (Keyboard Request): This key causes an interrupt in the P-C.

EOF (End of Field): When the P-C responds to this key, a word containing only a 12-bit is placed in core storage. Analysis of this word allows the program to determine that no further characters are to be sent in this message.

ER FLD (Erase Field): When the P-C responds to this key, a word containing only a 14-bit is placed in core storage. Analysis of this word allows the program to determine that the message being entered is to be deleted and replaced by a corrected message.

ER CHR (Erase Character): When the P-C responds to this key, a word containing only a 13-bit is placed in core storage. Analysis of this word allows the program to determine that the last character received is to be replaced by the next character to be entered.

Key	Hex	Keyboard Entry or Card Image Bits															IBM Card Code
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
*	4220	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	11,8,4
/	3000	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0,1
0	2000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0800	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	2
3	0400	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	3
4	0200	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	4
5	0100	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	5
6	0080	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	6
7	0040	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	7
8	0020	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	8
9	0010	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	9
$	4420	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	11,8,3
.	8420	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	12,8,3
,	2420	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0,8,3
EOF	0008	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	None
ER CHR	0004	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	None
ER FLD	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	None
=	00A0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	6,8
'	0120	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	5,8
(	8120	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	12,5,8
)	4120	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	11,5,8
+	80A0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	12,8,6
-	4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11
A	9000	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12,1
B	8800	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	12,2
C	8400	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	12,3
D	8200	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	12,4
E	8100	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	12,5
F	8080	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	12,6
G	8040	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	12,7
H	8020	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	12,8
I	8010	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	12,9
J	5000	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	11,1
K	4800	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11,2
L	4400	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	11,3
M	4200	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	11,4
N	4100	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	11,5
O	4080	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	11,6
P	4040	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	11,7
Q	4020	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	11,8
R	4010	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	11,9
S	2800	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0,2
T	2400	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0,3
U	2200	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0,4
V	2100	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0,5
W	2080	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0,6
X	2040	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0,7
Y	2020	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0,8
Z	2010	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0,9
Space	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
¢	8820	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	12,8,2
<	8220	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	12,8,4
|	8060	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	12,8,7
&	8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	12
!	4820	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	11,8,2
;	40A0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	11,8,6
¬	4060	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	11,8,7
%	2220	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0,8,4
_	2120	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0,8,5
>	20A0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0,8,6
?	2060	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0,8,7
:	0820	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	8,2
#	0420	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	8,3
@	0220	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	8,4
"	0060	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	8,7
0-8-2	2820	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0,8,2

27278A

Figure 59. 1816 Keyboard Input Codes

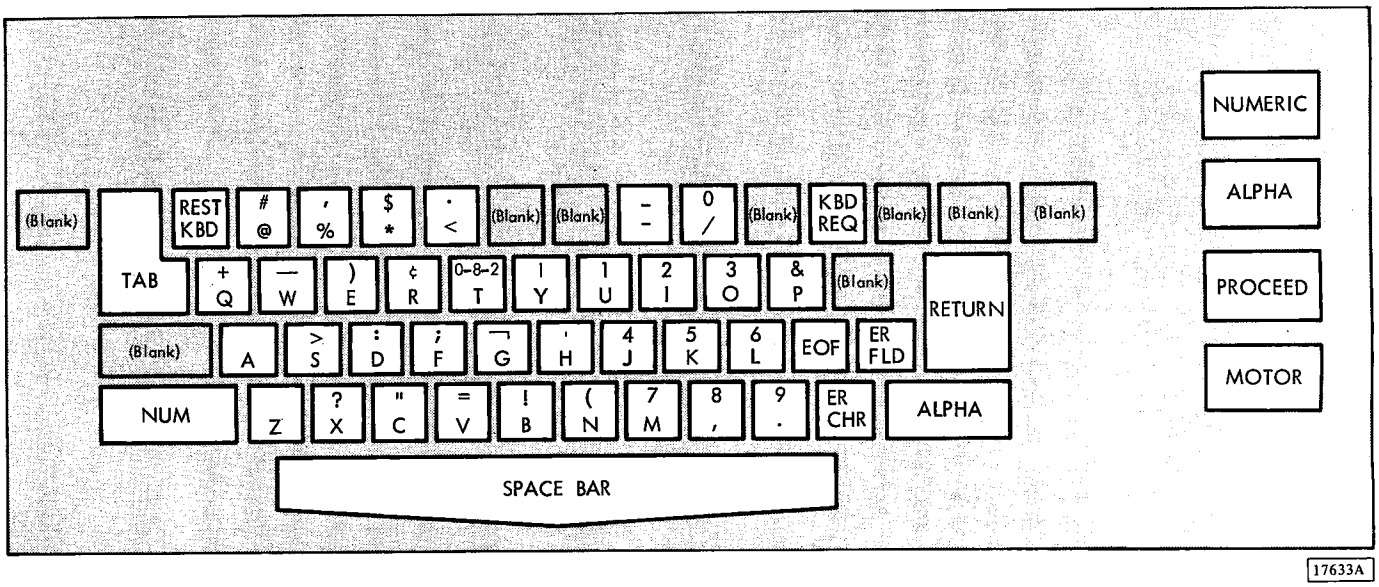


Figure 60. 1816 Keyboard

NUM (Numeric): This key places the keyboard in the numeric (uppercase shift) mode. The keyboard remains in this mode until changed. If the numbers or symbols which appear on the top portion of the keys are desired, the keyboard must be placed in numeric mode.

ALPHA (Alphabetic): This key places the keyboard in the alphabetic (lowercase shift) mode. The keyboard remains in this mode until changed. If the letters or symbols that appear on the bottom portion of the keys are desired, the keyboard must be placed in alphabetic mode.

Keyboard Lights

PROCEED: This light comes on when the P-C has performed an XIO control placing the keyboard in proceed status. This light goes off 25 ms after a key is pressed (at which time keyboard service response interrupt is given) or when an XIO read is performed.

ALPHA (alphabetic): When on, this light indicates that the keyboard is in alphabetic mode (lowercase shift).

NUMERIC: When on, this light indicates that the keyboard is in numeric mode (uppercase shift).

Operating Example

The following procedure describes a typical use of the keyboard.

1. Press REST KBD to restore the keyboard.
2. Press KBD REQ. The key locks down, the keyboard is interlocked and after 25 ms, keyboard request interrupt is set.
3. The program is interrupted. An XIO sense device reads the DSW into the accumulator, where it is interrogated and the keyboard request bit is found on. (XIO sense device uses modifier bit 15 to turn off the interrupt request.)
4. The program issues an XIO control. The proceed light turns on, the keyboard is restored, and the DSW keyboard not ready indicator turns on.
5. Press any character key. The key locks down and the keyboard is interlocked. After 25 ms, the proceed light turns off, a keyboard service response interrupt is set, and the DSW keyboard not ready indicator turns off.
6. The program is interrupted. An XIO sense device reads the DSW into the accumulator, where it is interrogated and the keyboard service response bit is found on. (XIO sense device uses modifier bit 15 to turn off the interrupt request.)
7. The program issues an XIO read to read the character into core storage. If a parity

error is detected, the program may read again.

8. Steps 4 through 7 are repeated until the message is complete, as indicated by pressing EOF.

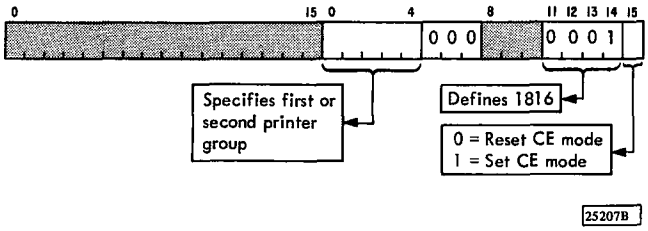
KEYBOARD PROGRAMMING

The 1861's operate under direct program control, utilizing the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO addresses the 1816's using the same principle as 1053 printer addressing. For example, an area code of 00001 with modifier bit 14 on addresses the 1816 in printer position 1. Similarly, an area code of 01111 with modifier bit 14 on addresses the 1816 in printer position 5.

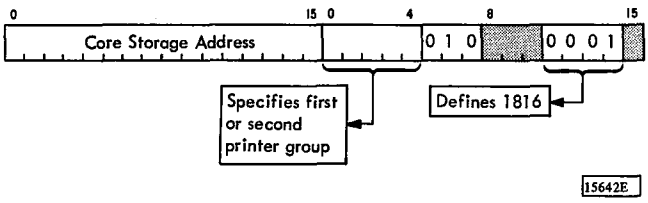
1816 Keyboard IOCC's

CE Mode



This command places the 1816 in CE mode if modifier bit 15 is on, or removes the 1816 from CE mode if modifier bit 15 is off.

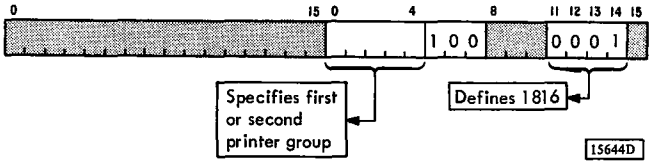
Read



This command causes a single keyboard input character to be read into the core storage location specified by the IOCC address word. It also turns off the proceed light.

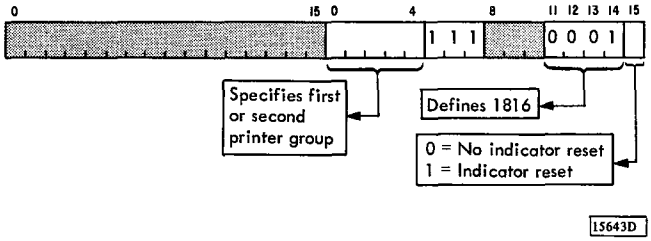
The character can be reread if desired.

Control



This command places the keyboard in proceed status so that a character can be entered. It also turns on the proceed light and restores the keyboard.

Sense Device



This command causes the device status word (DSW) of the 1816 to be placed in the accumulator (A). The DSW is shown in Figure 61.

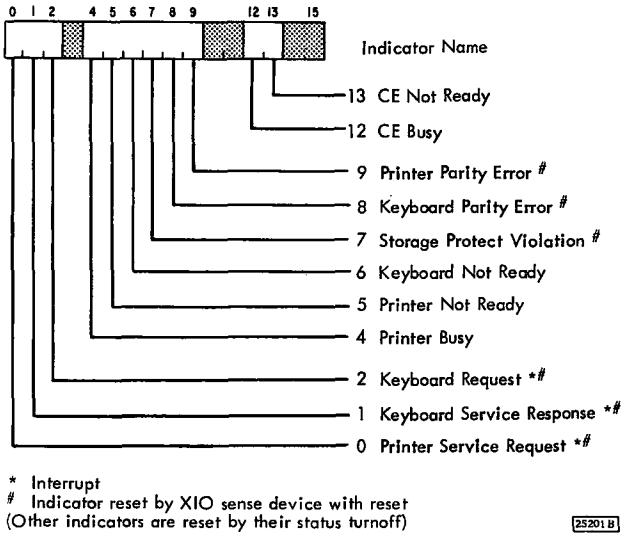


Figure 61. 1816 Device Status Word

Modifier bit 15 controls reset of the program resettable indicators in the DSW. If modifier bit 15 is on, the indicators are reset. (Any 1816 printer indicators that are on will be reset at the same time.) If modifier bit 15 is off, the indicators are not reset.

1816 DSW Interrupt Indicators

Three interrupt indicators are associated with the 1816: one for the printer and two for the keyboard. All three indicators are ORed together as a single interrupt. This single interrupt is assigned to a priority interrupt level and a unique interrupt level status word bit. The format of the 1816 DSW is shown in Figure 61 and interrupt and program resettable indicators are defined.

PRINTER SERVICE RESPONSE: This indicator turns on, causing an interrupt, each time the printer has printed the character or performed the control function sent by the last XIO write.

The printer service response must be turned off by a sense DSW with reset after the print operation is completed and before another print operation is initiated.

KEYBOARD SERVICE RESPONSE: This indicator turns on, causing an interrupt, when a character key on the keyboard is pressed. This interrupt indicates that a character is ready to be read into core storage.

KEYBOARD REQUEST: This indicator turns on, causing an interrupt, when KBD REQ is pressed.

1816 DSW Noninterrupt Indicators

Figure 61 shows the format of the 1816 DSW and defines noninterrupt and program resettable indicators.

PRINTER BUSY: When on, this indicator shows that the printer is in the process of printing a character or performing a control function, and should not be given another XIO write. This indicator turns on when data is sent to the printer and remains on until the printer has completed the action required.

Whenever printer busy is on, printer not ready is also on.

PRINTER NOT READY: When off, this indicator shows that the printer is properly loaded with forms, has dc power, is not in CE mode, and is not busy.

Usually, the program must determine that printer not ready (or CE not ready) is off before an XIO write is given.

Note: If an XIO write is given while a printer is busy and/or not ready, loss of information or repetitive print of the last character transmitted will occur. No indication of the information loss will be given.

One exception to the preceding rule is an XIO write with an adapter reset control character. This control character causes a blast reset to the adapter. If printer not ready is a result of a busy condition, the busy condition is reset and the printer becomes available for another XIO operation. If printer not ready is a result of a condition other than busy, the adapter reset control character performs no useful function.

If printer not ready is tested and found to be on, printer busy should then be tested. If printer busy is off, operator intervention is required unless the 1816 is in CE mode. However, printer not ready on with printer busy on indicates that the printer has not completed the function specified by the previous XIO. If a malfunction prevents completion of an operation, the printer and adapter are locked in a busy and not ready condition. To clear this condition, an XIO write with an adapter reset control character is required. However, the program must ensure that enough time is allowed for the previous operation to be completed before a reset is given. Otherwise, an operation may be prematurely terminated. Carrier return is the worst-case operation; it may require as much as 2 seconds for completion.

KEYBOARD NOT READY: When off, this indicator shows that the keyboard is attached, has dc power, is not in CE mode, and is not busy. The keyboard is normally not ready from the time a keyboard control is given until the keyboard service interrupt is generated, which is 25 ms after a character key has been pressed. This indicator is always on if no 1816 is attached in the first or fifth printer position.

The program must always determine that keyboard not ready is off before an XIO control or read is given. Otherwise, loss of information may occur with no indication to the program.

STORAGE PROTECT VIOLATION: This indicator is turned on if an attempt is made to read data from

the keyboard into a storage-protected core storage location.

KEYBOARD PARITY ERROR: This indicator is turned on if the P-C detects a parity error in the character received during an XIO read.

PRINTER PARITY ERROR: This indicator is turned on when a parity error is detected in the character received from the P-C.

CE BUSY: When the 1816 is in CE mode, this indicator is used in place of the printer busy indicator. All conditions defined in the printer busy status are applicable to this indicator in CE mode only. Programs utilizing CE mode use this indicator instead of the printer busy indicator.

CE NOT READY: When the 1816 is in CE mode, this indicator is used in place of both the keyboard not ready and the printer not ready indicators. All conditions defined for both the indicators are applicable to this indicator in CE mode only. Programs utilizing CE mode use this indicator instead of printer not ready or keyboard not ready indicators.

IBM 1054 Paper Tape Reader and IBM 1055 Paper Tape Punch

The IBM 1054 Paper Tape Reader (Figure 62) and IBM 1055 Paper Tape Punch (Figure 63) provide paper tape input/output for the 1800 system. One of each unit may be attached to the system.

FUNCTIONAL DESCRIPTION

Paper Tape Reader

The 1054 operates under direct program control and reads one-inch, eight-channel paper tape at a maximum rate of 14.8 characters per second.

Paper tape reading is initiated by an XIO control. This command loads a character into an input buffer and then moves the paper tape one character position. When the buffer has been loaded, an interrupt is initiated to signal the program that a character is available for reading into core storage. The character is read into core storage by a subsequent XIO read.

The elapsed time from the execution of the XIO control to the initiation of the interrupt is approximately 15 ms. To maintain the 14.8 characters per second operating speed of the 1054, the XIO read must be given within 60 ms after the interrupt. This timing ensures that another XIO control can be executed to energize the reader clutch preparatory to reading the next character.

Paper Tape Punch

The 1055 operates under direct program control and punches one-inch, eight-channel paper tape at a maximum rate of 14.8 characters per second.

Paper tape punching is initiated by an XIO write. This command starts the punch and causes the data in the core storage location specified by the command to be punched into the tape. Each core storage word contains one paper tape character

Character Coding

The 1054 reads input data into core storage in the form of an image of the punched holes. Figure 64 shows the relationship between bits of the core storage word and channels of the tape. One paper tape character is read into each addressed core storage location. Any code translation must be done by programming.

Punching is similar. The 1055 punches paper tape as an image of bit positions 0 through 7 of the core storage word. Figure 64 relates the bit positions to the channels. One character is punched from each addressed core storage location. Coding and recognition of control characters (such as feed code) and special data characters must be accomplished by programming.

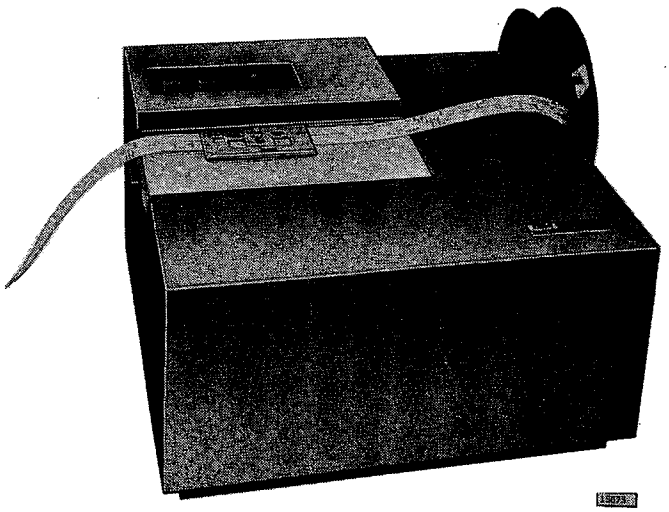


Figure 62. IBM 1054 Paper Tape Reader

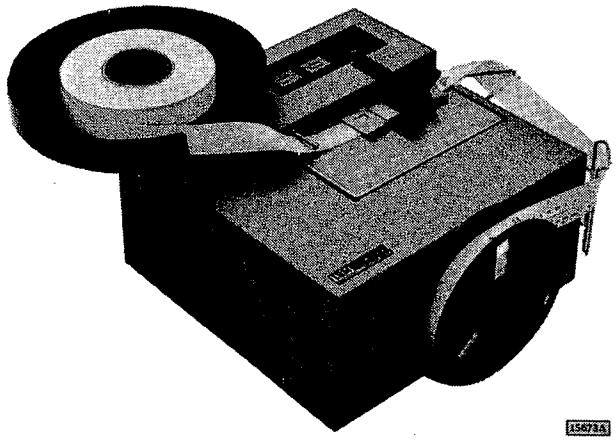


Figure 63. IBM 1055 Paper Tape Punch

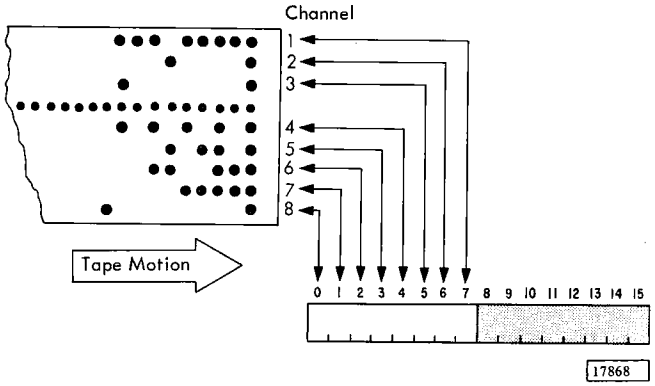


Figure 64. 1054/1055 Word Format

Paper Tape Initial Program Load

If no 1442 Card Read Punch is included in the system, the 1054 is wired for initial program load (IPL). IPL is initiated by pressing PROG LOAD on the P-C console. Doing so forces the 1054 into a run condition, in which it reads characters at its maximum rate of 14.8 characters per second. Data words are read into core storage starting at the location specified by the instruction (I) register (normally reset to /0000).

Paper tape channels 1 through 4 of each tape character are used as data bits for assembly into a 16-bit core storage word during IPL. Four tape characters are required to assemble one 16-bit word, as shown in Figure 65.

Once a word has been assembled in the 1054 adapter, it is automatically transferred to core storage. The I-register is increased by 1 for each word transferred.

The IPL operation continues until a channel-5 punch in other than a delete character is detected. (A delete character is defined as a hole in all tape channels except channel 8.) When a channel-5 punch is detected, IPL mode is terminated, the 1054 stops, the I-register is reset to /0000, and the P-C commences execution of the program. The tape character with the channel-5 punch is not read into core storage. It should be noted that the 1054 remains busy and not ready for several milliseconds after IPL mode is terminated.

During IPL, delete characters are recognized by the reader and not used for assembly into the 16-bit word. Delete characters are not recognized or handled in any special manner by the 1054 except in IPL mode.

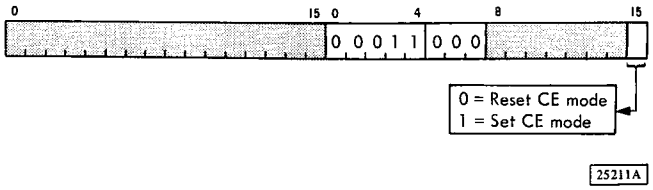
PAPER TAPE PROGRAMMING

Both the 1054 and 1055 operate under direct program control, utilizing the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO must have an area code of 00011 to address the 1054/1055. Both the 1054 and 1055 are addressed by the same area code and may operate simultaneously.

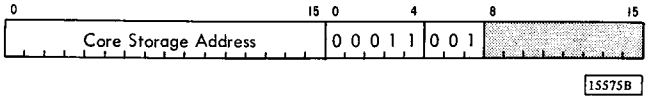
1054/1055 IOCC's

CE Mode



This command places the 1054/1055 in CE mode if modifier bit 15 is on, or removes the 1054/1055 from CE mode if modifier bit 15 is off.

Write



This command causes the character in bit positions 0 through 7 of the core storage location specified by the IOCC address word to be sent to the 1055 for punching.

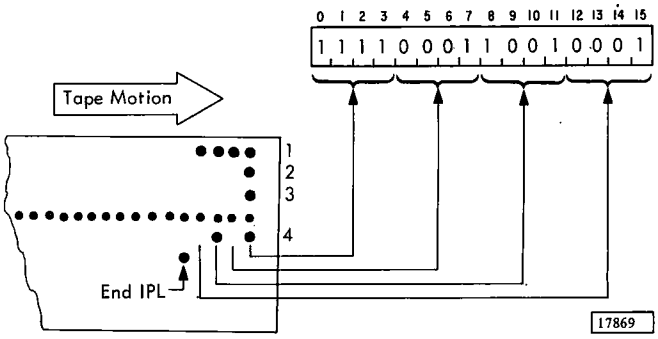
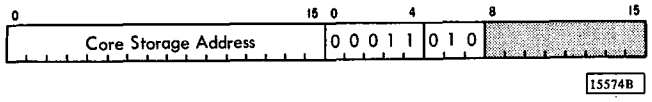


Figure 65. 1054 IPL Word Format

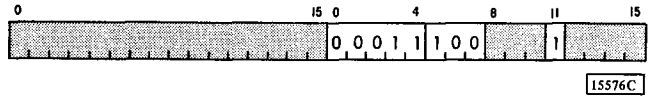
Read



This command causes the character in the paper tape buffer to be read into bit positions 0 through 7 of the core storage location specified by the IOCC address word. Bit positions 8 through 15 of the core storage location are set to 0.

Prior to issuing an XIO read, an XIO control should be executed to load a character into the buffer.

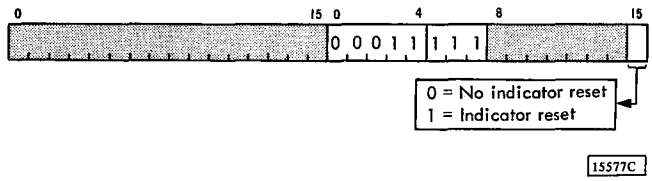
Control



This command causes one paper tape character to enter the paper tape buffer, the tape to advance one character position, and a reader service interrupt to be initiated. This interrupt signals that a character is ready in the buffer, to be read into core storage by a subsequent XIO read.

This command is valid only if modifier bit 11 (start paper tape reader) is on.

Sense Device



This command causes the 1054/1055 device status word (DSW) to be loaded into the accumulator (A). The DSW is shown in Figure 66.

Modifier bit 15 controls reset of the program resettable indicators. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset. Because the DSW is shared by the 1054 and 1055, care must be used in resetting indicators. Otherwise, indicators for one device may be lost when both devices are operating simultaneously.

1054/1055 DSW Interrupt Indicators

Two interrupt indicators are associated with the 1054/1055. These two interrupts are internally wired together and assigned to the same priority interrupt level. Figure 66 shows the 1054/1055 DSW format and defines interrupt and program resettable indicators.

READER SERVICE RESPONSE: This indicator turns on, causing an interrupt, when the 1054 completes execution of an XIO control. This interrupt indicates that a character is available in the paper tape buffer and can be read into core storage.

PUNCH SERVICE RESPONSE: This indicator turns on, causing an interrupt, when the 1055 finishes punching a character sent by an XIO write. This interrupt indicates that the 1055 can accept another command.

1054/1055 DSW Noninterrupt Indicators

Figure 66 shows the 1054/1055 DSW format and defines noninterrupt and program resettable indicators.

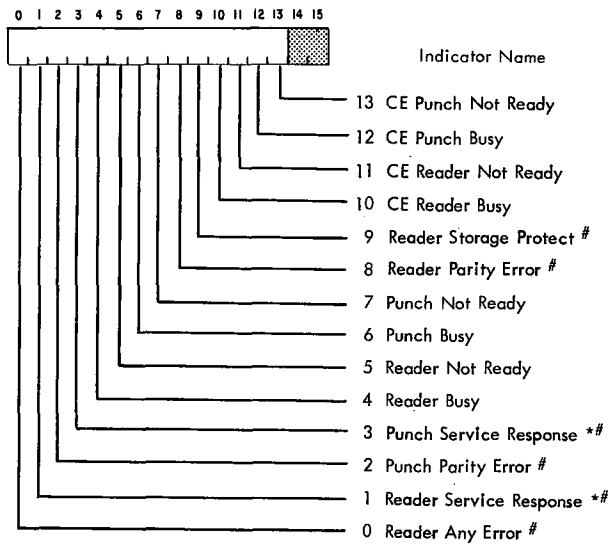


Figure 66. 1054/1055 Device Status Word

READER ANY ERROR: This indicator turns on during transfer of a word from the 1054 to core storage if either a parity error or storage protect violation is detection.

PUNCH PARITY ERROR: This indicator turns on if a parity error is detected in any character being sent to the 1055 by an XIO write.

READER BUSY: This indicator turns on when an XIO control (start paper tape reader) is given. It remains on until data is available (approximately 15 ms), as indicated by a reader service response interrupt.

Whenever reader busy is on, reader not ready is also on.

READER NOT READY: When off, this indicator shows that the 1054 is properly loaded with paper tape, the tape is feeding freely, and the 1054 is not busy or in CE mode.

The program must always determine that reader not ready (or CE not ready) is off before an XIO control or read is given. If an XIO read is given while this indicator is on, erroneous data can be read into core storage. No indication of the correctness of the data read is given.

If reader not ready is tested and found to be on, reader busy should then be tested. If reader busy is off, operator intervention is required unless the 1054 is in CE mode. However, the combination of reader not ready on and ready busy on indicates that the 1054 has not finished execution of a previous XIO control.

Reader not ready is on continuously if no 1054 is attached to the system.

PUNCH BUSY: This indicator is on for the total time the punch is mechanically engaged and punching a character (approximately 68 ms). During this time the 1055 is unable to accept another XIO write.

Whenever punch busy is on, punch not ready is also on.

PUNCH NOT READY: When off, this indicator shows that the 1055 is properly loaded with paper tape, the tape is feeding freely, the tape pressure lever is down and holding tape against the feed wheel, and the 1055 is not busy or in CE mode.

The program must always determine that punch not ready (or CE punch not ready) is off before an XIO write is given. If an XIO write is given while this indicator is on, data will probably be lost. No indication of the loss is given.

Punch not ready is on continuously if no 1055 is attached to the system.

READER PARITY ERROR: This indicator turns on if a parity error is detected in a character transferred from the 1054 to core storage by an XIO read.

READER STORAGE PROTECT: This indicator turns on if an XIO read attempts to transfer a character from the 1054 to a storage-protected core storage location.

CE READER BUSY: When the 1054 is in CE mode, this indicator is used in place of the reader busy indicator.

CE READER NOT READY: When the 1054 is in CE mode, this indicator is used in place of the reader not ready indicator.

CE PUNCH BUSY: When the 1055 is in CE mode, this indicator is used in place of the punch busy indicator.

CE PUNCH NOT READY: When the 1055 is in CE mode, this indicator is used in place of the punch not ready indicator.

The IBM 1442 Card Read Punch (Figure 67) provides card input/output for the 1800 system. A maximum of two 1442's (model 6 or 7) can be attached to the system.

FUNCTIONAL DESCRIPTION

The 1442, operating under data channel control, transports cards through the unit and accomplishes reading and punching as directed by the program. Cards are fed from a single supply hopper. They first pass the read station, then the punch station, as shown in Figure 68. Reading or punching is performed serially -- column by column.

Maximum machine speeds are:

Operation	Model	Speed
Read	6	300 cards per minute
	7	400 cards per minute
Punch	6	80 columns per second
	7	160 columns per second

Maximum reading rates are attained only when successive XIO initialize reads arrive early enough to re-energize the read clutch before the clutch latch point is reached. To accomplish this arrival timing, successive XIO initialize reads must arrive within 35 milliseconds (25 ms, model 7) after the operation complete interrupt is given by the 1442. If an XIO initialize read does not arrive within this time, the maximum reading rate becomes 285 cards per minute (cpm) for model 6 and 375 cpm for model 7.

Punching rates depend on the position of the card when the last column is punched. The punching speed ranges are:

Model 6: 49 cpm to 262 cpm
Model 7: 91 cpm to 355 cpm

The approximate time required to punch a single card is:

Model 6: 216 ms + 12.5 ms for each card column spaced or punched.

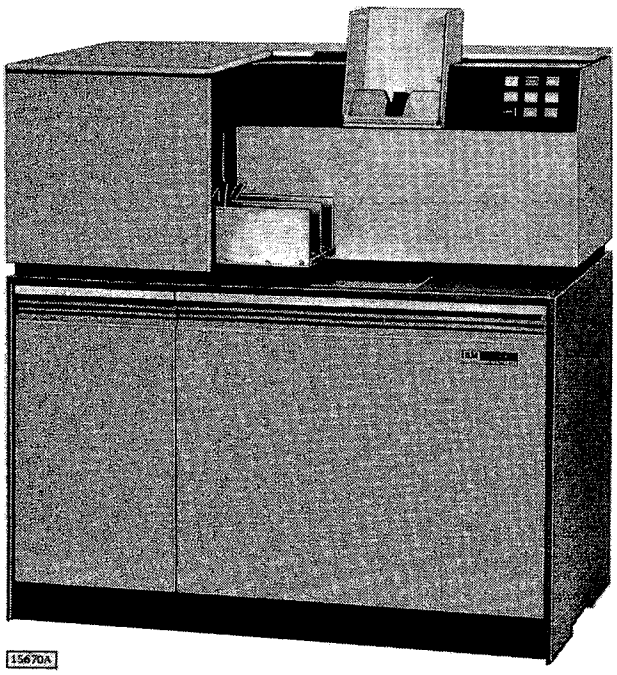


Figure 67. IBM 1442 Card Read Punch

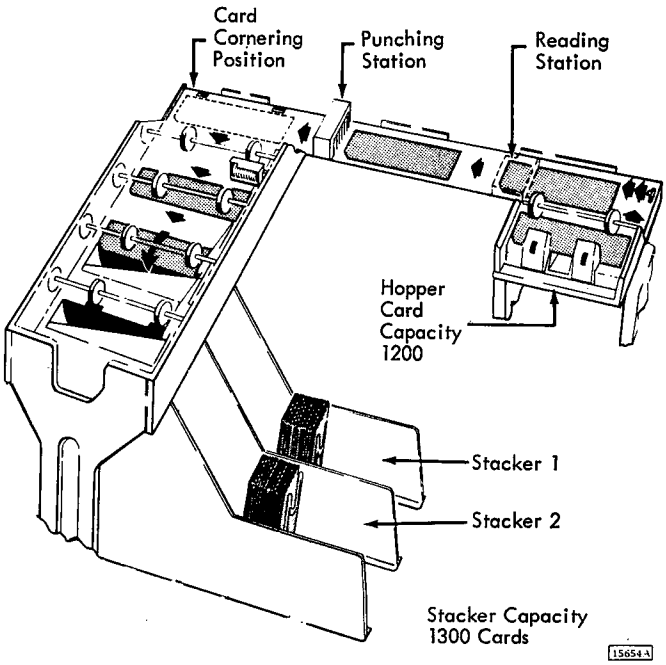


Figure 68. 1442 Card Path

Model 7: 163 ms + 6.25 ms for each card column spaced or punched.

Last Column Punched	Punch Time (ms)		Total Punch Cycle Time (ms)		Cards per Minute	
	Model 6	Model 7	Model 6	Model 7	Model 6	Model 7
1	13	6	229	169	262	355
10	125	63	341	226	176	265
20	250	125	466	288	127	208
30	375	188	591	351	102	171
40	500	250	716	413	84	145
50	625	313	841	476	71	126
60	750	375	966	538	62	112
70	875	438	1091	601	55	100
80	1000	500	1216	663	49	91

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Data Channel Assignment

If two 1442's are attached to the system, they must be assigned to separate data channels if they are to operate simultaneously.

Character Coding

The 1442 reads in either of two modes: card image or packed. It punches in card image mode only. Any combination of bits may be read or punched; therefore, any code translation required must be done by the stored program.

CARD IMAGE MODE: In this mode, the exact image of holes punched in the card is read and transferred to core storage. The relationship of the twelve rows in a card column to the bit positions of a core storage word is shown in Figure 69. Note that core storage word bit positions 12 through 15 are all set to 0. Card image character codes are shown in Figure 70.

PACKED MODE: In this mode, card rows 12 through 5 of the odd-numbered card columns and card rows 12 through 5 of the even-numbered card columns are assembled into one 16-bit word and transferred to core storage. Card rows 6 through 9 are ignored in all card columns. The 16-bit word is assembled as shown in Figure 71.

Card Initial Program Load

The first 1442 attached to the system is wired for initial program load (IPL). IPL is initiated by pressing PROG LOAD on the console. This causes the 1442 to read one card, in packed mode, into 40 ascending core storage locations beginning at the address specified by the instruction (I) register (normally reset to /0000). Following this load operation, the P-C branches to location /0000 and commences program execution. The mode switch should be on RUN or SIW/CS for program operation.

Power Down Consideration

If a card is left under the punches when the 1442 is powered down, it may be punched in one column. To prevent this, all cards should be run out and the unit made not ready prior to powering down.

Functional Keys

START: When initially loading the 1442 with cards, pressing START causes the bottom card in the hopper to move to the read station (run-in) and initiates ready status.

After manually stopping the 1442 or when initiating a last-card routine, pressing START restores ready status.

STOP: This key removes the 1442 from ready status. If card I/O is in process, the key must be held down until the operation complete interrupt is given; otherwise the 1442 will not recognize that STOP has been pressed.

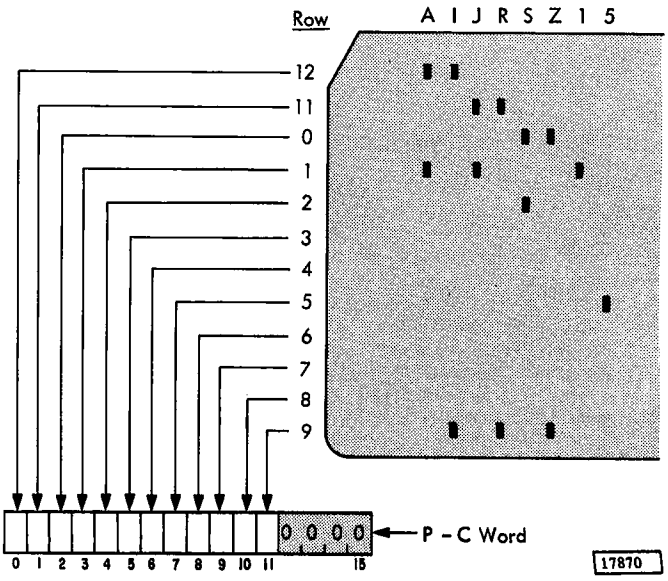

Figure 69. 1442 Card Image Format, Read or Punch

1816 Key	Hex	Core Storage Bit Image																IBM Card Code
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
*	4220	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	11,8,4
/	3000	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0,1
0	2000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0800	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	2
3	0400	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	3
4	0200	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	4
5	0100	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	5
6	0080	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	6
7	0040	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	7
8	0020	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	8
9	0010	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	9
$	4420	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	11,8,3
.	8420	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	12,8,3
,	2420	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0,8,3
EOF	0008	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	None
ER CHR	0004	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	None
ER FLD	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	None
=	00A0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	6,8
'	0120	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	5,8
(	8120	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	12,5,8
)	4120	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	11,5,8
+	80A0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	12,8,6
-	4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11
A	9000	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12,1
B	8800	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	12,2
C	8400	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	12,3
D	8200	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	12,4
E	8100	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	12,5
F	8080	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	12,6
G	8040	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	12,7
H	8020	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	12,8
I	8010	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	12,9
J	5000	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	11,1
K	4800	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11,2
L	4400	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	11,3
M	4200	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	11,4
N	4100	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	11,5
O	4080	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	11,6
P	4040	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	11,7
Q	4020	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	11,8
R	4010	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	11,9
S	2800	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0,2
T	2400	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0,3
U	2200	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0,4
V	2100	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0,5
W	2080	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0,6
X	2040	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0,7
Y	2020	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0,8
Z	2010	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0,9
Space	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
¢	8820	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	12,8,2
<	8220	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	12,8,4
|	8060	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	12,8,7
&	8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	12
!	4820	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	11,8,2
;	40A0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	11,8,6
¬	4060	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	11,8,7
%	2220	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0,8,4
_	2120	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0,8,5
>	20A0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0,8,6
?	2060	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0,8,7
:	0820	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	8,2
#	0420	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	8,3
@	0220	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	8,4
"	0060	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	8,7
0-8-2	2820	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0,8,2

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Figure 70. 1442 Card Image Character Codes

NPRO (Nonprocess Runout): This key is used to eject cards from the serial path without processing them and also resets the error conditions. The key is effective only if the hopper is empty. However, if the key is held depressed when the hopper goes empty during card operations, the operation complete interrupt for the card being processed is not given.

Lights

POWER ON: This light indicates that ac power is being supplied to the 1442.

CHIP BOX: This light indicates that the punch chip box is either full or has been removed. This condition removes the 1442 from ready status.

READY: This light indicates that the 1442 is prepared to accept commands from the P-C. The following conditions are required:

1. Power on.
2. Card properly registered in the read station.
3. Either cards in the hopper or 1442 in last-card routine.
4. Stacker not full.
5. Check light off.
6. Chip box light off.

CHECK: This light indicates that one of the eight error conditions exists. These are displayed on the back-lighted panel of the 1442 and are described in the following paragraphs. Any of these error conditions removes the 1442 from ready status and can be reset only by pressing NPRO with the hopper empty.

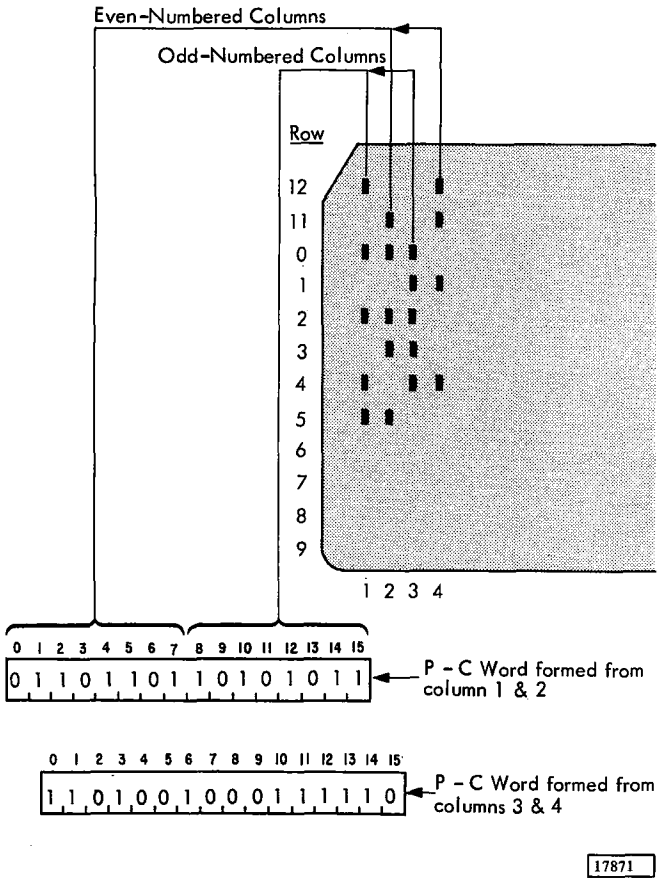


Figure 71. 1442 Packed Format, Read

HOPR (Hopper): This light indicates that a card failed to pass properly from the hopper to the read station area.

READ STA (Station): This light indicates that a card was not properly positioned (feed check) at the read station.

PUNCH STA (Station): This light indicates that a card was not properly positioned (feed check) at the punch station.

TRANS (Transport): This light indicates a card jam in the area between the punch station and the stackers.

FEED CLU (Clutch): This light indicates that a feed cycle was taken that was not requested.

READ REG (Registration): This light indicates that a read error occurred because of either (1) incorrect registration of the card, or (2) failure of the first and second readings of a card column to compare equally.

PUNCH: This light indicates that a punching error has been detected. Punching into prepunched columns does not cause a punch error.

OVERRUN: This light indicates that the data was lost because the channel failed to transfer data to or from core storage within the time the 1442 required service.

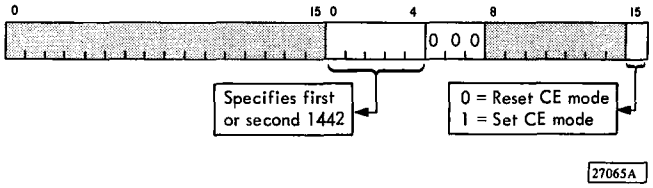
1442 PROGRAMMING

The 1442 operates under data channel control for data transfer and utilizes the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by the XIO must have an area code of 00010 to address the first 1442, or an area code of 10001 to address the second 1442. The following IOCC's provide for operation and control of the 1442.

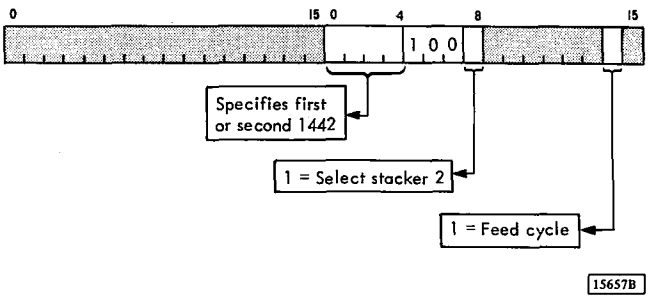
1442 IOCC's

CE Mode



This command places the 1442 in CE mode if modifier bit 15 is on, or removes the 1442 from CE mode if modifier bit 15 is off.

Control



This command causes the 1442 to perform a stacker select and/or feed cycle function, as indicated by

modifier bits 8 and 14, respectively. This command performs as a no-op if the 1442 is busy or not ready.

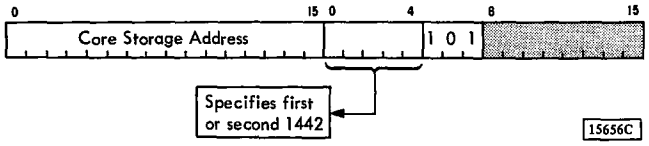
FEED CYCLE: This function ejects the card at the punch station to the stackers, feeds a card through the read station (without reading) and registers it at the punch station, and feeds the bottom card in the hopper into the read area.

The 1442 is busy during the feed operation. When the feed operation is completed, an operation complete interrupt is given.

STACKER SELECT: This function causes the next card leaving the punch area to enter the alternate stacker. It is effective for only one card. If feed cycle is also specified in the command, the card ejected from the punch station enters the alternate stacker.

The 1442 is not busy during a stacker select function. No interrupt is generated at the end of the operation.

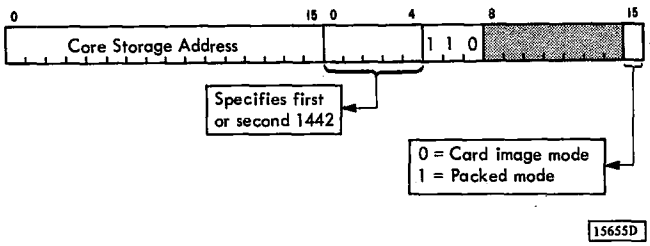
Initialize Write



This command causes data to be transferred from core storage to the 1442, and punched in card image mode. The starting location of this data is specified by the IOCC address word. Data is transferred under data channel (cycle steal) operation until the last data word to be punched is indicated by bit position 12 of the data word being on. After the last data word is punched, an operation complete interrupt is given.

The command performs as a no-op if the 1442 is busy or not ready.

Initialize Read

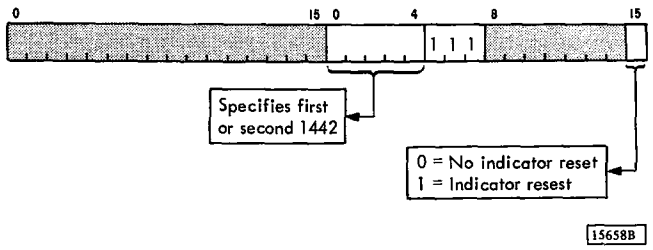


This command causes 80 columns of data (one card) to be read and transferred to core storage by means of data channel (cycle steal) operations. The starting core storage location is specified by the IOCC address word. An operation complete interrupt is given after all 80 columns have been read.

If modifier bit 15 is off, the data is read in card image mode and placed in 80 ascending core storage locations, beginning with the start address specified. If modifier bit 15 is on, the data is read in packed mode and placed in 40 ascending core storage locations, beginning with the start address specified.

This instruction performs as a no-op if the 1442 is busy or not ready.

Sense Device



This command causes the 1442 device status word (DSW) to be read into the accumulator. The DSW is shown in Figure 72.

Modifier bit 15 controls reset of the program resettable indicators in the DSW. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset.

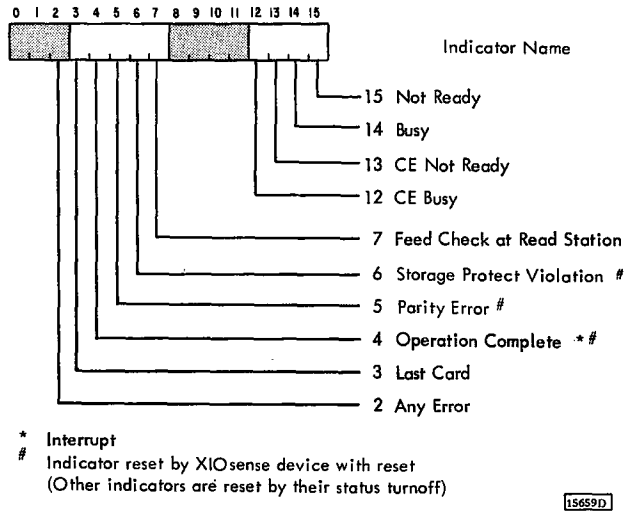


Figure 72. 1442 Device Status Word

1442 DSW Interrupt Indicators

Figure 72 shows the format of the DSW and defines interrupt and program resettable indicators.

OPERATION COMPLETE: This indicator turns on, causing an interrupt, after completion of a read or feed operation. The interrupt occurs 20.6 ms after column 80 has passed the read station in a model 6, or 15.4 ms after column 80 has passed the read station in a model 7.

Operation complete also turns on after the last column to be punched has been punched and checked, and the punch drive has stopped. This occurs 12.5 ms after the last column punched on a model 6, or 6.25 ms after the last column punched on a model 7.

Operation complete also turns on if an XIO is given after operation complete for a previous operation is given, but before one of the following errors is detected: transport, hopper misfeed, feed check at punch station, or feed clutch.

1442 DSW Noninterrupt Indicators

Figure 72 shows the format of DSW indicators and defines noninterrupt and program resettable indicators.

ANY ERROR: This indicator turns on if one or more of the following error conditions exist:

1. Parity error.
2. Storage protect violation.
3. Feed check at read station.
4. Overrun.
5. Read registration check.
6. Punch check.
7. Hopper misfeed.
8. Transport.
9. Feed check at punch station.
10. Feed clutch.

Error conditions 7 through 10 of the preceding list are not turned on until after operation complete is on, unless the operation was an XIO initialize write requiring an automatic feed cycle. If another operation is initiated before these error indicators are turned on, an operation complete interrupt is forced, and no reading or punching takes place.

LAST CARD: This indicator shows that column 80 of the last card has passed the read station and that the hopper and read station are empty.

PARITY ERROR: This indicator turns on if a transfer to or from core storage has resulted in a word not having correct (odd) parity. A parity error does not remove the 1442 from ready status.

STORAGE PROTECT VIOLATION: This indicator turns on if the 1442 attempts to read into a storage-protected core storage location. A storage protect violation does not remove the 1442 from ready status.

FEED CHECK AT READ STATION: When on, this indicator means that a card is improperly positioned at the read station.

CE BUSY: When the 1442 is in CE mode, this indicator is used in place of the busy indicator.

CE NOT READY: When the 1442 is in CE mode, this indicator is used in place of the not ready indicator.

BUSY: When on, this indicator means that a read, punch, or card feed operation is in progress and that the 1442 cannot accept another XIO initialize read, XIO initialize write, or XIO control. If one of these commands is given while busy is on, it is treated as a no-op. Whenever busy is on, not ready is also on.

NOT READY: When off, this indicator shows that the 1442 is in ready status, is not in CE mode, and is not busy. The 1442 is in ready status if all of the following conditions exist:

1. Power is on.
2. A card is registered at the read station or a last-card sequence is in progress.
3. Cards are in the hopper or last-card sequence is in progress.
4. Stacker is not full.
5. Check light is off.
6. START has been pressed after manual stop.
7. Chip box is not full and not removed.

If an XIO initialize read, XIO initialize write or XIO control is given while the 1442 is not ready or busy, it performs as a no-op.

READ AND PUNCH OPERATIONS

Before any operation can begin, the 1442 must be placed in ready status. With power on and cards in the hopper, pressing START causes the bottom card in the hopper to be fed into the read area (run in) and places the 1442 in ready status.

Card Feeding

Cards are moved through the 1442 in feed cycles. Each cycle causes the card at the punch station to be ejected to the stackers, the card at the read station to be transported through the read station and registered at the punch station, and the bottom card in the hopper to be fed into the read area.

A feed cycle is initiated by an XIO write (if no card is present at the punch station), XIO control (feed cycle), or XIO initialize read.

All cards pass through the read and punch stations, but reading and/or punching occurs only by program command.

Card Reading

Card reading is initiated by an XIO initialize read. If the 1442 is in ready status, the card at the read station is registered and fed through the read station. This feed causes columns 1 through 80 of the card to be read in one continuous motion. The card is read serially -- column by column -- beginning with column 1. Reading is accomplished through photocell sensing. Each column is read twice, and the readings are compared for agreement.

Data that has been read is transferred to core storage by means of data channel (cycle steal) operations. After all 80 columns have been read, an operation complete interrupt occurs.

Data can be read in card image mode or packed mode, depending on modifier bit 15 in the IOCC.

Card Punching

Card punching is initiated by an XIO initialize write. If the 1442 is in ready status and a card is registered at the punch station, a data channel (cycle steal) request is made for data transfer. An incremental punch drive causes the card to be punched and moved through the punch station.

If the 1442 is in ready status and a card is not registered at the punch station, a feed cycle is taken to move the card from the read station to the punch station. Punching then proceeds in the normal manner.

Punch checking is accomplished by comparing punch echo data (created by actual punching motion) with the punch buffer, which contains the character from the P-C.

Card motion and punching continue until a data word containing a 1 in bit position 12 (last character) is received from the P-C. When this occurs, the 1442 punches and advances the card one more column and then generates an operation complete interrupt. Once punching has been terminated in this manner, it cannot be restarted in this card. A punch terminator (bit 12) must be present within the first 80 words of data because an attempt to punch beyond column 80 will occur if a last character is not detected. An interrupt occurs only when a bit 12 is found in a data word.

Last-Card Sequence

When the hopper becomes empty during a feed cycle, the 1442 is removed from ready status. The operator may continue processing cards by loading more cards into the hopper and pressing START, or he may initiate a last-card sequence by pressing START without loading more cards in the hopper. When START is pressed without cards in the hopper, but with a card in the read station, the 1442 is placed in ready status. It then allows two more feed cycles to be taken. No operation complete is given at the end of the second feed cycle.

The program senses the occurrence of the last-card sequence by means of the last-card indicator in the device status word. This indicator is turned on after the last card has passed the read station (first feed cycle) and remains on until a second feed cycle has been taken.

Error Recovery

Error recovery requires the cooperation of the operator and programmer as indicated in the following examples:

1. If a parity error or storage protect violation occurs, the 1442 is not removed from ready status, data transmission does not stop, and no 1442 error light is turned on. Therefore the program must inform the operator of the error before the cards can be repositioned and the operation reinitiated.
2. If a hopper misfeed occurs, the card at the punch station has not been punched and the bottom card in the hopper has not been fed. If the command was XIO initialize write, the card at the punch station can be placed back in the hopper and the command given again. If the command was an XIO control (feed) to eject the card at the punch station prior to giving a punch command, the card that was ejected should not be placed back in the hopper unless the program is prepared to cause two feed cycles before any punching is done.

The preceding examples show that if an error occurs, a program may need to detect the difference between an I/O operation completed incorrectly (example 1) and an I/O operation not even initiated (example 2). This may be done as follows:

1. If the command given was an XIO control (feed cycle), the operation was completed incorrectly if the DSW feed check at read station indicator is on; otherwise the operation was not initiated.
2. If the command given was an XIO initialize read, the operation was completed incorrectly if the DSW parity error, storage protect violation, or feed check at read station indicator is on; otherwise, the core storage locations read into must be examined. If a column was read, the operation was completed incorrectly because of overrun or read registration check; if no column was read, the operation was not initiated due to one of the following errors; hopper misfeed, transport, feed check at punch station, or feed clutch.
3. If the command given was XIO initialize write, the card was incorrectly punched if overrun or punch check occurred. If feed check at read station is on, punching was not initiated although the automatic feed cycle did eject the card from the punch station. The program cannot detect the difference between a punch check (card punched incorrectly) and one of the following feed errors (card not punched): hopper misfeed, transport, feed check at punch station, or feed clutch.

1442 Usage Meter

This meter runs when the following conditions are present:

1. The unit is selected for operation by the program.
2. The processor is running.

Once the unit has been selected, the meter continues to run until a programmed stop occurs, or until a programmed or nonprocess runout clears all cards from the card transport area.

The IBM 1443 Printer (Figure 73) provides high-speed, on-line printing capabilities for the 1800 system. One 1443 (model 1 or 2) can be attached to the system.

FUNCTIONAL DESCRIPTION

The 1443 is a buffered printer and operates under data channel control for data transfer. This combination allows on-line printing with a minimum amount of P-C time.

Data to be printed must be edited and arranged in core storage in the exact form that it is to be printed. The data format in core storage is two characters per word, as shown in Figure 74.

An XIO initialize write causes data to be transferred to the print buffer two characters (one core storage word) at a time. The total number of characters transferred depends on the word count (n). A word count of n will cause 2n characters to be transferred; therefore, n must not be greater than one-half the number of possible print positions in the 1443.

Once data transfer is completed, the remaining positions of the print buffer are automatically filled with blanks. The 1443 then prints the line.

The total time demand on the P-C during buffer loading by means of data channel (cycle steal) operations depends on core storage cycle time, which is approximately 4(n+1) for 4-μs core storage, 2.25 (n+1) for 2.25-μs core storage, or 2(n+1) for 2-μs core storage, where n equals the word count.

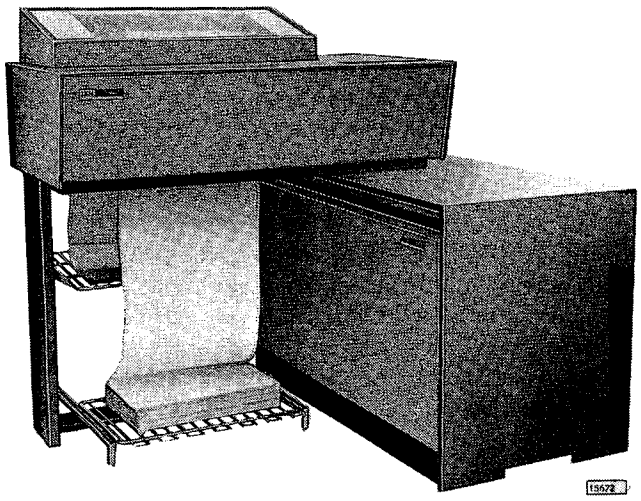


Figure 73. IBM 1443 Printer

Printing Speeds

The actual line-printing speed of the 1443 depends on the typebar being used. Four typebars are available: 13, 39, 52, and 63 characters. The printing speeds with the various typebars are:

Character Set	Lines per Minute	
	1443-1	1443-2
13	430	600
39	190	300
52	150	240
63	120	200

15565C

Print Positions

The standard 1443 has 120 print positions per line, horizontally spaced at 10 positions per inch. Twenty-four additional print positions are available as a special feature.

Character Sets and Coding

Four character sets are available, one for each typebar. The 52-character typebar is standard. Figure 75 shows the character coding required in

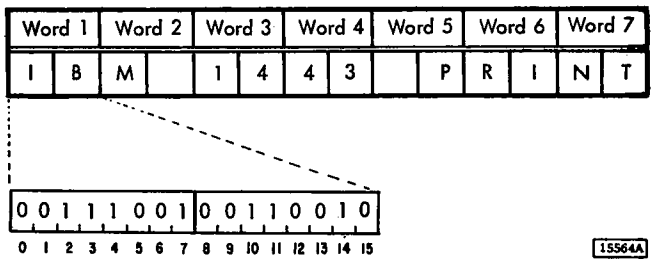


Figure 74. Core Storage Word Format, 1443

Char	Hex	Core Storage Bits 0	1	2	3	4	5	6	7	Typebar Character Set			
		8	9	10	11	12	13	14	15	63	52	39	13
A	31	0	0	1	1	0	0	0	1	x	x	x	
B	32	0	0	1	1	0	0	1	0	x	x	x	
C	33	0	0	1	1	0	0	1	1	x	x	x	
D	34	0	0	1	1	0	1	0	0	x	x	x	
E	35	0	0	1	1	0	1	0	1	x	x	x	
F	36	0	0	1	1	0	1	1	0	x	x	x	
G	37	0	0	1	1	0	1	1	1	x	x	x	
H	38	0	0	1	1	1	0	0	0	x	x	x	
I	39	0	0	1	1	1	0	0	1	x	x	x	
J	21	0	0	1	0	0	0	0	1	x	x	x	
K	22	0	0	1	0	0	0	1	0	x	x	x	
L	23	0	0	1	0	0	0	1	1	x	x	x	
M	24	0	0	1	0	0	1	0	0	x	x	x	
N	25	0	0	1	0	0	1	0	1	x	x	x	
O	26	0	0	1	0	0	1	1	0	x	x	x	
P	27	0	0	1	0	0	1	1	1	x	x	x	
Q	28	0	0	1	0	1	0	0	0	x	x	x	
R	29	0	0	1	0	1	0	0	1	x	x	x	
S	12	0	0	0	1	0	0	1	0	x	x	x	
T	13	0	0	0	1	0	0	1	1	x	x	x	
U	14	0	0	0	1	0	1	0	0	x	x	x	
V	15	0	0	0	1	0	1	0	1	x	x	x	
W	16	0	0	0	1	0	1	1	0	x	x	x	
X	17	0	0	0	1	0	1	1	1	x	x	x	
Y	18	0	0	0	1	1	0	0	0	x	x	x	
Z	19	0	0	0	1	1	0	0	1	x	x	x	
1	01	0	0	0	0	0	0	0	1	x	x	x	x
2	02	0	0	0	0	0	0	1	0	x	x	x	x
3	03	0	0	0	0	0	0	1	1	x	x	x	x
4	04	0	0	0	0	0	1	0	0	x	x	x	x
5	05	0	0	0	0	0	1	0	1	x	x	x	x
6	06	0	0	0	0	0	1	1	0	x	x	x	x
7	07	0	0	0	0	0	1	1	1	x	x	x	x
8	08	0	0	0	0	1	0	0	0	x	x	x	x
9	09	0	0	0	0	1	0	0	1	x	x	x	x
0	0A	0	0	0	0	1	0	1	0	x	x	x	x
+	10	0	0	0	1	0	0	0	0	x	x		
&	30	0	0	1	1	0	0	0	0	x	x		
-	20	0	0	1	0	0	0	0	0	x	x		x
/	11	0	0	0	1	0	0	0	1	x	x		
%	1A	0	0	0	1	1	0	1	0	x	x		
¤	3A	0	0	1	1	1	0	1	0	x	x		
#	2A	0	0	1	0	1	0	1	0	x	x		
=	0B	0	0	0	0	1	0	1	1	x	x		
'	1B	0	0	0	1	1	0	1	1	x	x	x	
.	3B	0	0	1	1	1	0	1	1	x	x	x	x
$	2B	0	0	1	0	1	0	1	1	x	x	x	
@	0C	0	0	0	0	1	1	0	0	x	x		
(	1C	0	0	0	1	1	1	0	0	x	x		
)	3C	0	0	1	1	1	1	0	0	x	x		
*	2C	0	0	1	0	1	1	0	0	x	x		x
'	0D	0	0	0	0	1	1	0	1	x	x		
_	1D	0	0	0	1	1	1	0	1	x			
¢	3D	0	0	1	1	1	1	0	1	x			
!	2D	0	0	1	0	1	1	0	1	x			
>	0E	0	0	0	0	1	1	1	0	x			
:	1E	0	0	0	1	1	1	1	0	x			
<	3E	0	0	1	1	1	1	1	0	x			
;	2E	0	0	1	0	1	1	1	0	x			
?	0F	0	0	0	0	1	1	1	1	x			
"	1F	0	0	0	1	1	1	1	1	x			
|	3F	0	0	1	1	1	1	1	1	x			
¬	2F	0	0	1	0	1	1	1	1	x			

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Figure 75. 1443 Character Codes

core storage for each printed character and the typebar with which each character can be used.

Carriage

The carriage, which is tape controlled, advances the forms as directed by the program.

Spacing and skipping of the carriage are under direct program control through the XIO control command. An XIO control can be used to initiate an immediate or a delayed start for space and skip operations. Immediate space or skip operations are performed at the time the XIO control is given. Delayed space or skip operations are performed at the end of the next print cycle. They supersede the automatic single spacing after print that occurs if there is no programmed carriage control.

Skipping speed is about 15 inches per second. The carriage can be single, double, or triple spaced on an immediate or delayed basis. An immediate space or skip requires 45 ms for the first line and 10 ms for each additional line. A delayed space or delayed skip of one or two lines is performed as part of the 1443 print cycle. The third line adds approximately 1 ms to the print time, and each additional line skipped adds 10 ms.

Continuous forms with marginal punched feed holes on both sides must be used in the 1443 carriage.

Functional Keys and Switches

START: Pressing this key places the 1443 in ready status provided:

1. AC and dc power are on.
2. Forms are properly loaded.
3. Typebar is in position.
4. Typebar motor switch is set to ON.
5. Carriage brush assembly is closed.
6. Six-to-eight line drive cover is closed.
7. No error condition exists.

STOP: Pressing this key removes the printer from ready status and turns off the ready light. If a print or control operation is already in progress, it is completed. If a print or control operation is not in progress, all further action is prevented until START has been pressed.

CARRIAGE RESTORE: Pressing this key when the ready light is off positions the carriage at the next channel 1 punch of the control tape. If the carriage clutch is disengaged, the form does not move. When the clutch is engaged, the form moves in synchronization with the control tape. If the printer is in ready status (ready light on), CARRIAGE RESTORE has no effect.

CARRIAGE SPACE: Pressing this key when the ready light is off causes the carriage to advance one space. Forms advance with the carriage if the carriage clutch is engaged. If the clutch is not engaged, the forms do not advance. CARRIAGE SPACE has no effect when the ready light is on.

RESET: Pressing this key causes all printer check circuit indicators to be reset.

CARRIAGE STOP: Pressing this key stops carriage operation and turns off the ready light. Do not press CARRIAGE STOP to stop printing operations; upon restarting, overprinting may occur.

TYPEBAR MOTOR: This switch has three positions: on, off, and typebar removal. The typebar motor switch is turned to the on position for normal operation. In the off position, the ribbon motor, typebar motor, and ready light are turned off; however, ribbon and typebar control circuits are still active. In the typebar removal position, the ribbon motor, typebar motor, and ready lights are turned off. Ribbon and typebar control circuits are also turned off to permit typebar removal. Use this position when removing or installing a typebar.

Do not turn this switch to off or typebar removal positions while the typebar is in motion.

TYPEBAR SELECTOR SWITCH: This switch is used to select the character bar being used. The typebar select switch has four settings: 13, 39, 52, and 63. This switch must be set to the position corresponding to the typebar being used or a sync check occurs.

This switch is installed only if the selective character feature is installed.

Lights

POWER ON: This light indicates that power is applied to printer control circuits.

READY: This light indicates that the 1443 is in ready status and able to accept program commands. Ready turns off if:

1. STOP or CARRIAGE STOP is pressed.
2. The printer runs out of forms and control tape channel 1 punch is sensed.
3. Typebar motor switch is turned to off.
4. Brush assembly is opened.
5. Six-to-eight line drive cover is opened.
6. A forms check switch is actuated.

SYNC CHECK: This light turns on when the typebar is out of synchronism with the printer. When this occurs the printer is removed from ready status. Pressing RESET turns the light off.

PARITY CHECK: This light turns on when a parity error is detected by the error checking circuits. It is reset manually by the console reset key or the printer reset key. It is reset by the program when the parity error indicator is program tested with an XIO sense device with reset.

FORM CHECK: This light turns on when a form check switch on a form tractor is actuated to indicate that either: (1) forms are feeding improperly, or (2) the form guide plates are not in operating position.

END-OF-FORM: This light turns on when approximately 4 inches of the last form remains to be printed. However, the printer continues to operate until the carriage control tape advanced to a channel 1 punch, which resets ready status. Pressing START places the printer in ready status and allows printing to continue until another control tape channel 1 punch is sensed. Ready status will again be reset.

CARRIAGE INTERLOCK: This light turns on if either of two conditions exists: (1) the typebar motor is on and the tape-brush assembly is not closed, or (2) the cover over the six-to-eight line drive is open.

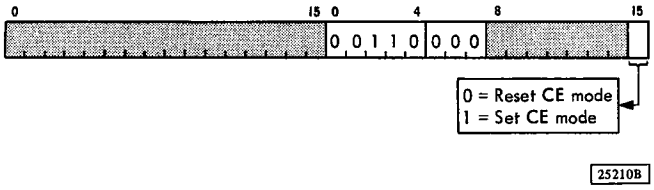
PRINTER PROGRAMMING

The 1443 operates under data channel control for data transfer and utilizes the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO must have an area code of 00110 to address the 1443. The following IOCC's are used for operation and control of the 1443.

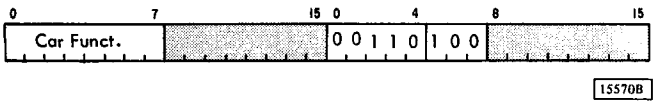
1443 IOCC's

CE Mode



This command places the 1443 in CE mode if modifier bit 15 is on, or removes the 1443 from CE mode if modifier bit 15 is off.

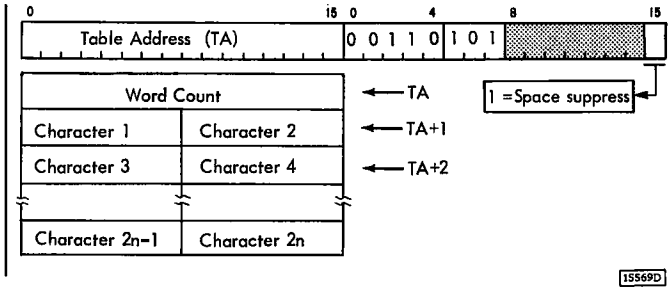
Control



This command is used to initiate the carriage control function specified by bits 0 through 7 of the address word. The various carriage control functions and their codes are shown in Figure 76. When the specified carriage control function is completed, a printer complete interrupt is generated.

This command performs as a no-op if the printer is busy or not ready, or if the carriage is busy.

Initialize Write



This command causes data in a table starting at the core storage location specified by the IOCC address word to be transferred to the 1443 buffer. The first word of the table contains the word count (n) which defines the number of data words in the message. This count causes 2n characters to be sent to the print buffer (two characters per word).

The word count and data words are transferred by means of data channel (cycle steal) operations. When the number of words specified by the word count have been transferred, a transfer complete interrupt is generated and the remainder of the print buffer is loaded with blanks without accessing core storage. When the last position of the print buffer is loaded, the 1443 automatically takes a print cycle.

Modifier bit 15 controls the space suppress function. If modifier bit 15 is on, the carriage will

Immediate Skip to	Hex	Bit 0 1 2 3 4 5 6 7	Skip after Print to	Hex	Bit 0 1 2 3 4 5 6 7
Channel 1	01	0 0 0 0 0 0 0 1	Channel 1	31	0 0 1 1 0 0 0 1
Channel 2	02	0 0 0 0 0 0 1 0	Channel 2	32	0 0 1 1 0 0 1 0
Channel 3	03	0 0 0 0 0 0 1 1	Channel 3	33	0 0 1 1 0 0 1 1
Channel 4	04	0 0 0 0 0 1 0 0	Channel 4	34	0 0 1 1 0 1 0 0
Channel 5	05	0 0 0 0 0 1 0 1	Channel 5	35	0 0 1 1 0 1 0 1
Channel 6	06	0 0 0 0 0 1 1 0	Channel 6	36	0 0 1 1 0 1 1 0
Channel 7	07	0 0 0 0 0 1 1 1	Channel 7	37	0 0 1 1 0 1 1 1
Channel 8	08	0 0 0 0 1 0 0 0	Channel 8	38	0 0 1 1 1 0 0 0
Channel 9	09	0 0 0 0 1 0 0 1	Channel 9	39	0 0 1 1 1 0 0 1
Channel 10	0A	0 0 0 0 1 0 1 0	Channel 10	3A	0 0 1 1 1 0 1 0
Channel 11	0B	0 0 0 0 1 0 1 1	Channel 11	3B	0 0 1 1 1 0 1 1
Channel 12	0C	0 0 0 0 1 1 0 0	Channel 12	3C	0 0 1 1 1 1 0 0
Immediate Space			Space after Print		
1 Space	21	0 0 1 0 0 0 0 1	1 Space	11	0 0 0 1 0 0 0 1
2 Spaces	22	0 0 1 0 0 0 1 0	2 Spaces	12	0 0 0 1 0 0 1 0
3 Spaces	23	0 0 1 0 0 0 1 1	3 Spaces	13	0 0 0 1 0 0 1 1

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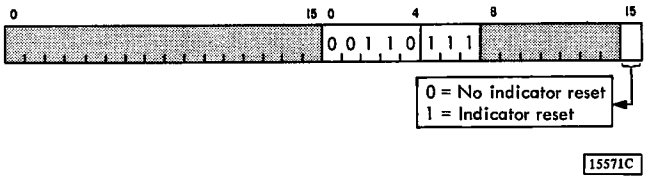
Figure 76. 1443 Carriage Control Functions and Codes

not perform an automatic space or any after-print control function after the line is printed. If modifier bit 15 is off, the carriage will perform an automatic space or any previously specified after-print control function after the line is printed.

This command performs as a no-op if the printer is busy or not ready, or if the carriage is busy.

Sense Device



This command causes the 1443 device status word (DSW) to be read into the accumulator. The DSW is shown in Figure 77. Modifier bit 15 controls the reset of the program resettable indicators in the DSW. If modifier bit 15 is on, the indicators are reset; if modifier bit 15 is off, the indicators are not reset.

1443 DSW Interrupt Indicators

Figure 77 shows the 1443 DSW format and defines interrupt and program resettable indicators.

TRANSFER COMPLETE: This indicator turns on, causing an interrupt, when the number of words specified by the word count have been transferred to the print buffer. When this interrupt occurs, the program can start placing the next line of print into the print message area.

PRINTER COMPLETE: This indicator turns on, causing an interrupt, when the printer has completed a carriage control function, or a print cycle and the subsequent carriage control function (if any). It signals that the next operation can be initiated.

1443 DSW Noninterrupt Indicators

Figure 77 shows the 1443 DSW format and defines noninterrupt and program resettable indicators.

ERROR: This indicator turns on if a parity check or sync check occurs in the 1443 during a print cycle, or a parity error is detected during transfer of data from core storage to the print buffer. The indicator can be reset by an XIO sense device with reset. If the indicator was turned on by a printer parity check or a parity error detected during data transfer, it can also be turned off by pressing console RESET. If a sync check turned the indicator on, XIO sense device does not reset it. RESET on the 1443 resets the indicator if a printer parity check or a sync check turned the indicator on. In addition to turning on the error indicator, a sync check also removes the 1443 from ready status.

CHANNEL 9: This indicator turns on when a channel 9 punch is detected in the carriage control tape. This indicator is turned off by detecting a channel 12 punch in the control tape.

CHANNEL 12: This indicator turns on when a channel 12 punch is detected in the control tape. This indicator is turned off by detecting a channel 1 punch in the control tape.

CHANNEL 1: This indicator is on only when a channel 1 punch is under the carriage control tape sensing brushes.

PARITY ERROR: This indicator turns on when a parity error is detected during data transfer from core storage to the print buffer.

CE CARRIAGE BUSY: When the 1443 is in CE mode, this indicator is used in place of the carriage busy indicator.

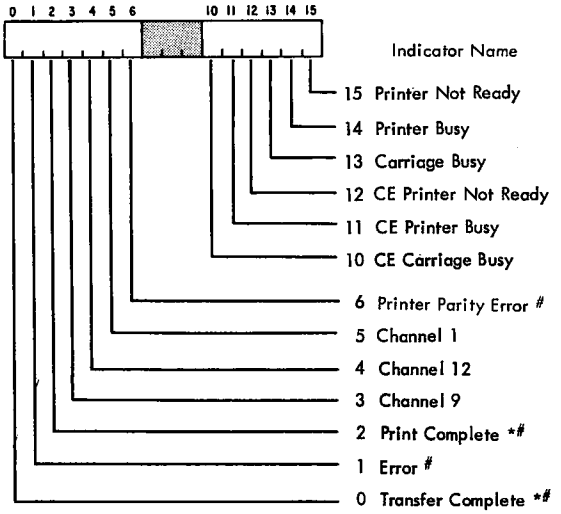


Figure 77. 1443 Device Status Word

CE PRINTER BUSY: When the 1443 is in CE mode, this indicator is used in place of the printer busy indicator.

CE PRINTER NOT READY: When the 1443 is in CE mode, this indicator is used in place of the printer not ready indicator.

CARRIAGE BUSY: When on, this indicator means that the carriage is in motion or that printing is in progress and the 1443 cannot accept another XIO initialize write or XIO control. If one of these commands is given while carriage busy is on, it is treated as a no-op.

PRINTER BUSY: When on, this indicator means that printing is in progress or that the carriage is in motion; in either case, the 1443 cannot accept another XIO initialize write or XIO control. If one of these commands is given while printer busy is on, it is treated as a no-op. Whenever printer busy is on, printer not ready is also on.

PRINTER NOT READY: This indicator is on if any of the following conditions exists:

1. Printer busy is on.
2. The 1443 is physically unable to accept a command.
3. The end-of-forms light is on.
4. The 1443 is in CE mode.

If an XIO initialize write or XIO control is given while printer not ready is on, it is treated as a no-op.

1443 Usage Meter

This meter runs when both of the following conditions are present:

1. The printer is selected for operation by the program.
2. The processor is running.

Once the printer has been selected, the meter continues to run until the printer is manually stopped by the operator, an out-of-forms condition exists, or a programmed stop of the P-C occurs.

The IBM 1627 Plotter (Figure 78) provides an exceptionally versatile, reliable, and easy-to-operate plotting system for the 1800 system. The plotter converts tabulated digital information into graphic form. Bar charts, flow charts, organization charts, engineering drawings, and maps are among the many graphic forms of data which can be plotted on the 1627 Plotter. One 1627 (model 1 or 2) can be attached to the system.

FUNCTIONAL DESCRIPTION

The 1627 operates under direct program control. Data is transferred serially from core storage to the 1627, where it is translated into actuating signals. These signals produce drawing movements on the 1627.

Actual recording is produced by incremental movement of the pen on the paper surface (y-axis) and/or incremental movement of the paper under the pen (x-axis). The pen is mounted in a carriage that travels horizontally across the paper. Vertical plotting motion is achieved by rotation of the pin-feed drum, which also serves as a platen (Figure 79).

The drum and pen carriage are bidirectional; that is, the paper moves up or down, and the pen moves right or left. Control is also provided to raise the pen from or lower the pen to the paper surface. The pen remains in the raised or lowered position until directed to change to the opposite status.

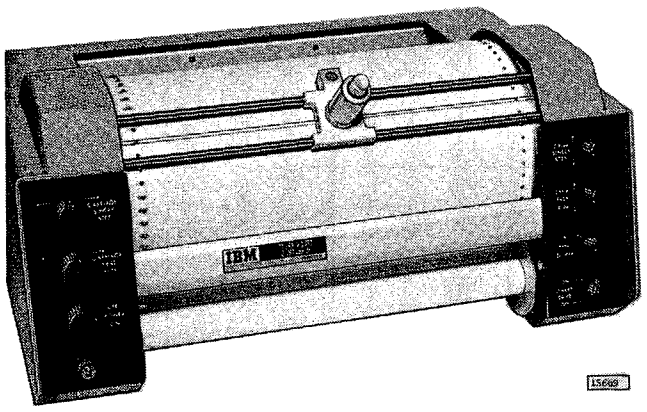


Figure 78. IBM 1627 Plotter

The drum and pen-carriage movements and pen status are controlled by digits transferred to the 1627. Bit positions 0 through 5 of each output word are decoded into directional signals which cause a 1/100-inch incremental movement of the pen carriage and/or paper, or a raise-pen or lower-pen movement. The relationship of bit positions 0 through 5 of the output word and pen or paper movement is as follows:

Bit Position	Movement
0	Pen down
1	Drum down
2	Drum up
3	Carriage right
4	Carriage left
5	Pen up

Figure 80 shows possible motion resulting from each word in the output record. It is possible to give contradictory bit combinations, such as 1 and 2 (drum down and drum up), or 3 and 4 (carriage right and carriage left). These are invalid and should not be used. No definite statement can be made about what action (if any) will occur if opposing movements are specified.

The time required to raise or lower the pen is 100 ms. The time to plot a point is approximately

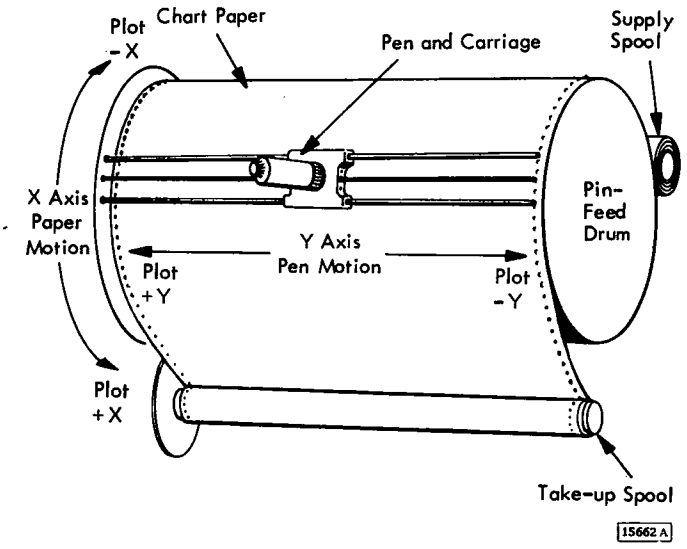
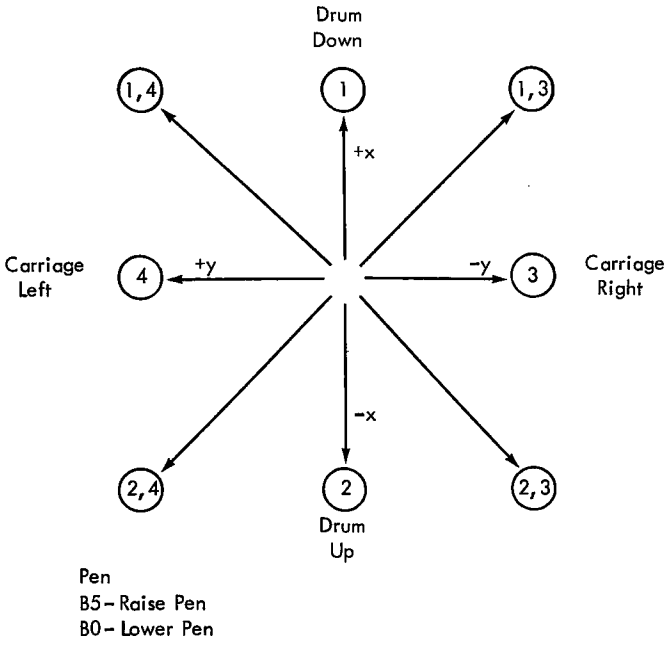


Figure 79. 1627 Paper and Pen Motions



Note: The encircled numerical figures are the P-C word bit positions that correspond to the indicated direction of plotting movement as viewed from the front of the plotter. Normally, graphs are plotted so that their horizontal axes are, in reality the X axis as shown above.

25205

Figure 80. 1627 Output Record Control

3.3 ms for a model 1 or 5 ms for a model 2. To keep plotter operation at full speed, the next control character must be sent to the 1627 within 0.5 ms after the service complete interrupt.

A summary of the 1627 operating characteristics is presented in Figure 81.

Functional Switches

POWER ON/OFF: This switch brings power from the P-C to the 1627. No power on delay is involved with the 1627; that is, the 1627 can operate as soon as power is applied. The power on light associated with the switch is on when power is on.

CARRIAGE FAST RUN: This switch allows the pen carriage to be stepped rapidly to the left or right at a rate of 120 steps a second. The carriage fast run switch is used to move the carriage to any desired area of the graph.

CARRIAGE SINGLE STEP: This switch allows the pen carriage to be moved in single step increments (1/100 inch), either left or right. The carriage single step switch permits the operator to accurately align the carriage along the y-axis of the chart.

DRUM FAST RUN: This switch allows the drum to move paper rapidly up or down at the rate of 120 steps a second. The drum fast run switch is used in conjunction with the carrriage fast run switch to position the pen to any desired area of the graph.

DRUM SINGLE STEP: This switch allows the drum to be rotated in single step increments (1/100 inch) in either direction. The drum single step switch is used in conjunction with the carriage single step switch to permit the operator to accurately align the pen on a point or fixed coordinate on the graph.

PEN: This switch provides a means for manually raising the pen from the surface of the drum or lowering the pen to the drum.

CHART DRIVE: This switch allows the front and rear chart drives to be disabled. When recording on single sheets of graph paper, the chart drive switch should be in the off position. When recording on roll paper, this switch should be in the on position.

VERNIER CONTROL: Large-size chart paper may vary in width due to high or low humidity; therefore a vernier control is provided on the 1627 model 2, to vary the size of pen-carriage increments. In this way, pen movement is adjusted to match the printed scale of the chart paper. The vernier control knob is located at the left end of the drum, above the switch panel. For work with nonscale paper, the control should be centered at the zero position.

PLOTTER PROGRAMMING

The 1627 operates under direct program control and utilizes the execute I/O (XIO) instruction.

		Model 1	Model 2
Speed	X, Y Increments	18,000 Steps/Min	12,000 Steps/Min
	Pen Status Change	600 Operations/Min	600 Operations/Min
Increment Size		1/100 Inch	1/100 Inch
Chart Paper	Width	12 Inches	31 Inches
	Plotting Width	11 Inches	29 1/2 Inches
	Length	120 Feet	120 Feet
	Sprocket Hole Dimensions	.130 Inch Dia on 3/8 Inch Centers	.188 Inch Dia on 1 Inch Centers

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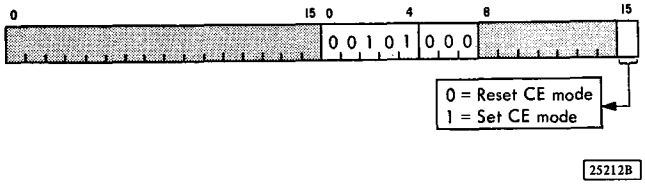
Figure 81. 1627 Operating Characteristics

The input/output control command (IOCC) referenced by an XIO must have an area code of 00101 to address the 1627. The following IOCC's are used for operation and control of the 1627.

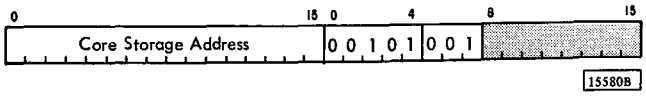
1627 IOCC's

CE Mode

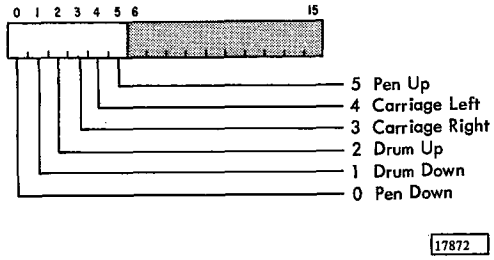


This command places the 1627 in CE mode if modifier bit 15 is on, or removes the 1627 from CE mode if modifier bit 15 is off.

Write

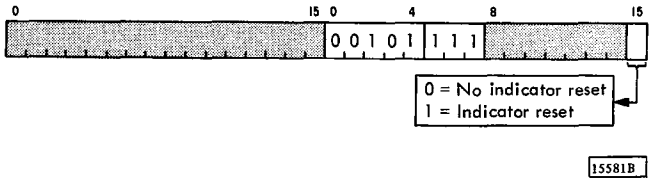


This command causes the data word at the core storage location specified by the IOCC address word to be sent to the 1627. Bit positions 0 through 5 of the data word are converted to pen movements as follows:



If this command is given while the 1627 is busy or not ready, loss of information will probably occur. No indication of the loss is given.

Sense Device



This command causes the 1627 device status word (DSW) to be read into the accumulator. The DSW is shown in Figure 82.

Modifier bit 15 controls reset of program resettable DSW indicators. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset.

1627 DSW Interrupt Indicator

Figure 82 shows the 1627 DSW format and defines interrupt and program resettable indicators.

SERVICE COMPLETE: This is the only interrupt associated with the 1627. This indicator turns on, causing an interrupt, when the 1627 has completed the action specified by the last XIO write. This interrupt indicates that the 1627 is able to accept another command.

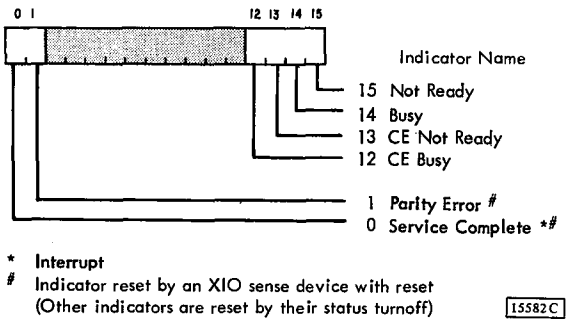


Figure 82. 1627 Device Status Word

1627 DSW Noninterrupt Indicators

Figure 82 shows the 1627 DSW format and defines noninterrupt and program resettable indicators.

PARITY ERROR: This indicator turns on when a parity error is detected during transfer of data from core storage to the 1627.

CE BUSY: When the 1627 is in CE mode, this indicator is used in place of the busy indicator.

CE NOT READY: When the 1627 is in CE mode, this indicator is used in place of the not ready indicator.

BUSY: This indicator is on when the 1627 is busy and cannot accept another character. If an XIO write is given while the 1627 is busy or not ready, loss of information will probably occur. No indication of the loss is given.

NOT READY: When off, this indicator means that the 1627 has power, is in ready status, and is not in CE mode.

The IBM 1810 Disk Storage (Figure 83) provides random access storage capabilities for the 1800 system. One 1810 (model A1, A2, A3, B1, B2, or B3) can be attached to the system. Models A1 and B1 contain one disk storage drive; models A2 and B2 contain two disk storage drives; models A3 and B3 contain three disk storage drives.

FUNCTIONAL DESCRIPTION

Data transfer to or from each disk storage drive in an 1810 is under data channel control. All three drives may be attached to the same data channel. However, the drives must be attached to separate data channels if they are to operate concurrently.

The disk storage recording medium is an oxide coated disk in an interchangeable IBM 2315 Disk Cartridge.

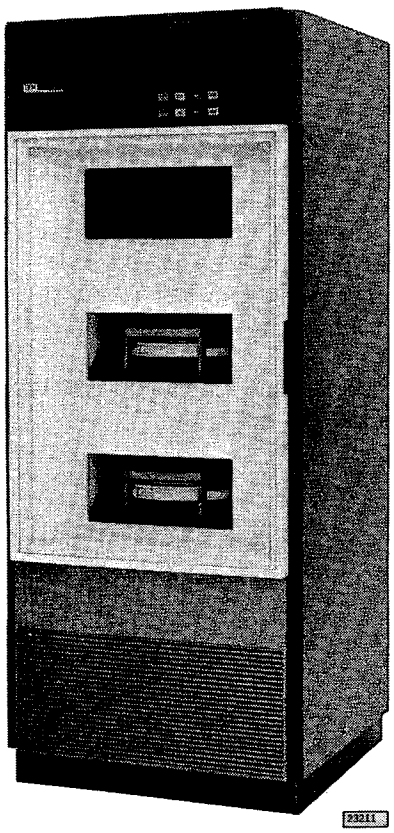


Figure 83. IBM 1810 Disk Storage

The access mechanism consists of two parallel horizontal arms that straddle the disk. Each arm has a magnetic read/write head, and each head is positioned to read or write on the corresponding disk surface. The entire assembly moves horizontally, allowing the heads to have access to the entire recording area (two surfaces). The access mechanism can be placed in any one of 203 positions by program command.

Writing or reading of disk information occurs as the disk surface revolves (at 1,500 rpm) past the read/write heads. Information is written on the disk by magnetizing small discrete areas on the disk in a circular pattern. Information is read from the disk by sensing the presence or absence of the magnetized spots around the circular pattern.

Disk Organization and Capacity

The circular patterns of data on the disk are called tracks. A track on the upper surface of the disk and its corresponding track on the lower surface of the disk are called a cylinder. The total number of cylinders is 203; 3 cylinders are used as spares to ensure that 200 cylinders are available for use. Figure 84 shows the innermost and outermost cylinders on a disk. The intermediate cylinders have been omitted for clarity.

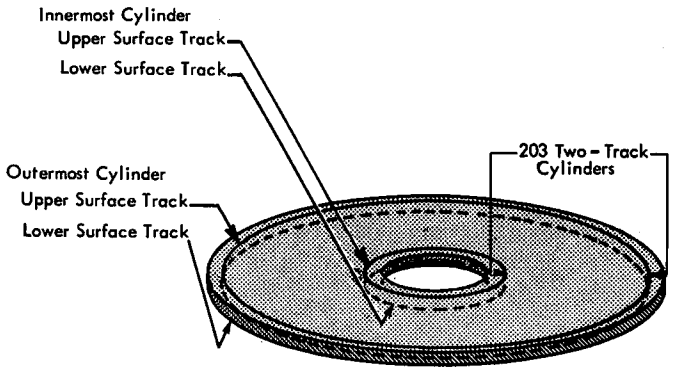
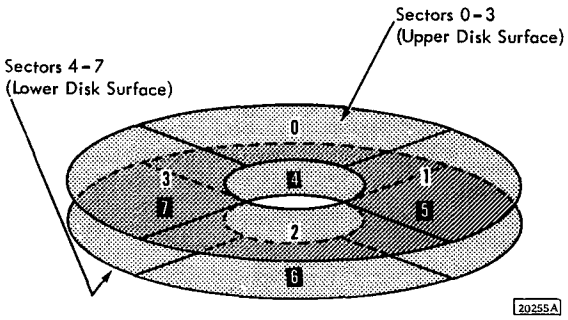


Figure 84. Cylinder Concept

Each track is divided into four equal segments called sectors. Sectors are numbered from 0 through 7. As shown in the following illustration, sectors 0 through 3 divide the upper surface tracks; sectors 4 through 7 divide the lower surface tracks. A sector contains 321 data words and is the largest segment of data that can be read or written with a single instruction.



The sector is the basic addressable unit for reading and writing. Each XIO initialize read or XIO initialize write must address one of the eight sectors available to the heads in each cylinder.

Although the capacity of the sector is 321 words, it is recommended that one word be written as a sector address, leaving 320 data words. A command may specify any number of words equal to or less than 321. A zero word count will force an operation complete interrupt with no reading or writing occurring. The 321-word capacity, then, refers only to a maximum number of words that may be transferred with one command and still ensure at least 235 μs before the next sector starts. This allows sufficient time for the issuance of the next XIO.

No circuitry is provided in the 1810 to limit reading or writing to 321 words. Therefore, the program must limit the word count. A 1810 word is composed of 16 data bits, 3 check bits, and 1 space bit. (The check and space bits do not appear on the in or out bus.) The following illustration shows the organizational components of disk storage. Note that the capacities are based upon the 320-word sector.

No of / Per	Word	Sector	Track	Cylinder	Disk
Bits	16	5,120	20,480	40,960	8,192,000
Data Words		320	1,280	2,560	512,000
Sectors			4	8	1,600
Tracks				2	400
Cylinders					200

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Timing

The magnetic disk revolves at 1500 rpm, making the revolution time 40 ms. The word rate is 36 kHz.

There is no timing consideration for switching read/write heads. The shortest time available between the end of a 321 word sector and the beginning of the next sector is approximately 235 μs. For every word not used, 27.8 μs may be added.

Access Time: Models A1, A2, and A3

The incremental access mechanism used with A-models of the 1810 requires 15 ms to move one or two cylinders. Therefore, the number of cylinders (n) must be even when calculating access time. (The next higher even number is used if an odd number of cylinders is specified.)

In addition to the time required to move from one cylinder to another, 20-25 ms must be allowed for carriage stabilization before reading or writing can occur. This delay occurs automatically; any XIO initialize read or XIO initialize write issued is executed immediately after the 20-25 ms delay. However, 20-25 ms is also required between accesses; this delay is usually accomplished by a read operation between accesses.

Figure 85 shows access time, including carriage stabilization, for A-models of the 1810.

Access Time: Models B1, B2, and B3

The direct access mechanism used with B-models of the 1810 moves in one continuous motion to the cylinder address. Access time, including carriage stabilization, is shown in Figure 86.

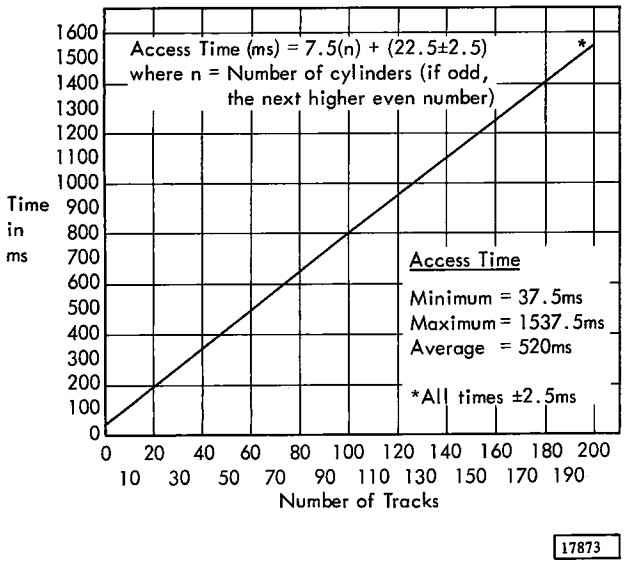


Figure 85. 1810 Access Time, "A" Models

Data Transfer Checking

Data transferred between core storage and disk storage is monitored for four conditions to ensure accuracy in data transfer.

Parity

All words transferred to or from core storage are checked for odd parity; that is, each word must have an odd number of bits turned on.

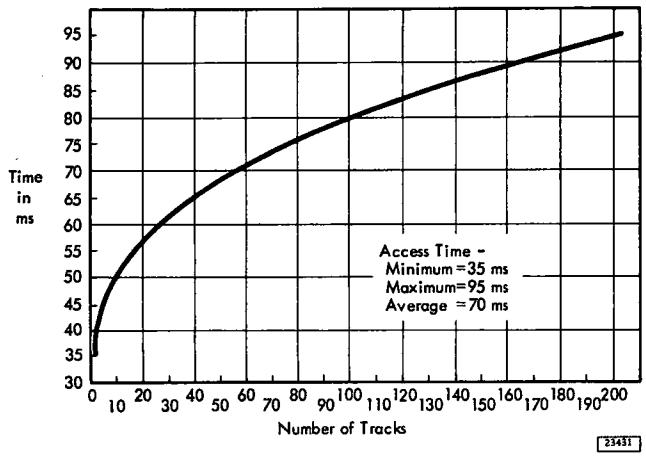


Figure 86. 1810 Access Time, "B" Models

Storage Protect Violation

Each core storage address is checked for a storage-protect bit before a new word is placed there. If an attempt is made to transfer data to a protected area, an indicator is set in the 1810 device status word but operation is not terminated. However, data in the protected location is not changed. Data is written from core storage to disk storage without this check. The storage-protect bit prevents data transfer from disk to core storage only.

Data Overrun

If a disk drive is not assigned to a data channel with sufficiently high priority, data may be lost. Data overrun checks that the previous word has been transferred to or from core storage before the next word on the disk requires service.

Modulo 4

The disk storage adapter generates up to three additional check bits for each word written. These bits are written at the end of each word so that the total number of bits in each disk storage word is divisible by 4. This divisible-by-4 (modulo 4) condition is checked as the word is written on the disk and as it is read from the disk.

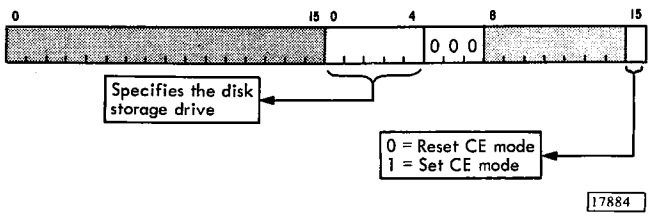
DISK STORAGE PROGRAMMING

The 1810 Disk Storage Drives operate under data channel control for data transfer and utilize the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO must have an area code of 00100, 01000, or 01001 for disk storage drives 1, 2, or 3, respectively. The following IOCC's are used for operation and control of the disk storage drives.

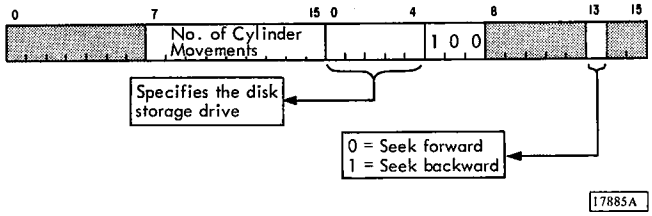
1810 IOCC's

CE Mode



This command places the disk storage drive, specified by the area code, in CE mode if modifier bit 15 is on, or removes the disk storage drive from CE mode if modifier bit 15 is off.

Control: A—Models

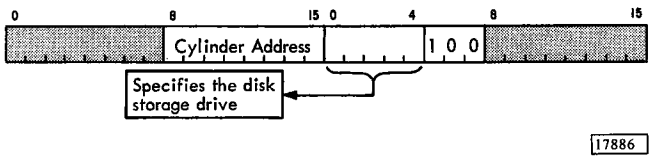


This command causes the carriage to move (seek) the number of cylinders specified by bits 7 through 15 of the IOCC address word. The number of cylinders specified may be from 1 through 202.

Modifier bit 13 specifies the direction of the seek. If modifier bit 13 is on, the carriage moves backward (toward the outer edge of the disk). If modifier bit 13 is off, the carriage moves forward (toward the center of the disk). At the end of the seek operation, an operation complete interrupt is given.

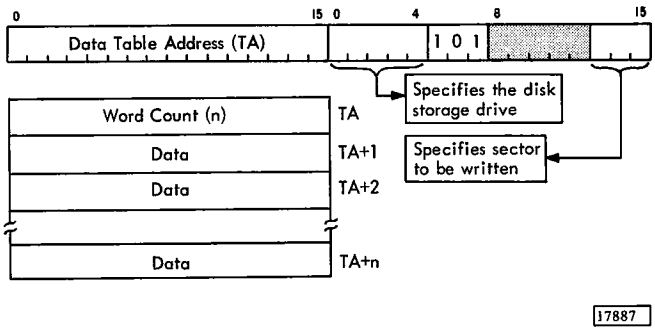
If two seek operations are given without a 22.5-ms delay between them, an error may occur on the next read/write operation.

Control: B—Models



This command causes the carriage to move (seek) to the cylinder address specified by the IOCC address word. An operation complete interrupt is given when the seek operation is completed. The cylinder address may range from 0 through 202. A cylinder address greater than 202 will cause a seek error and an operation complete interrupt.

Initialize Write



This command causes data in a table starting at the core storage location specified by the IOCC address word to be written in the sector indicated by modifier bits 13 through 15. The first word of the table contains the word count (n), which defines the number of data words to be written. Up to 321 words (one complete sector) may be specified. A separate command must be given for each sector or portion of a sector to be written.

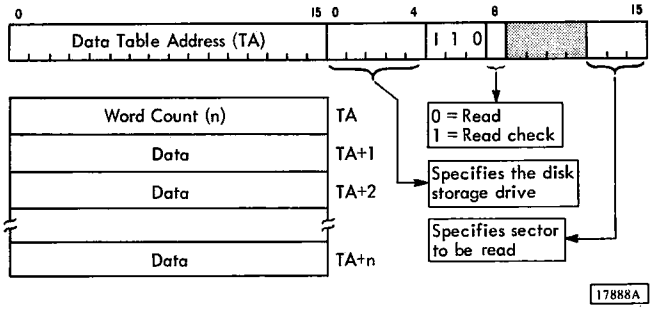
The word count and data words are transferred by means of data channel (cycle steal) operations. When the number of data words specified has been written, an operation complete interrupt is given. This command is treated as a no-op if given while the disk storage drive is busy or not ready.

WRITE CHECKING: To achieve the maximum level of performance, the program should provide for repetition of XIO initialize writes that indicate any data transfer errors. These errors are often due to temporary conditions that are not present in subsequent retries.

An XIO initialize write that does not write correctly, because of temporary or intermittent conditions, can be detected immediately by performing a read check operation. Thus, "soft" write errors can be corrected while the data is still available.

In IBM programming systems, use of read check is optional. The programmer should weigh the time consumed by error recovery procedures against the time consumed in read checking.

Initialize Read



This command causes data words to be read from the disk storage sector specified by modifier bits 13 through 15 and transferred to a table starting at the core storage location specified by the IOCC address word. The first word of the table in core storage contains the word count (n) which defines the number of data words to be read. Up to 321 words (one complete sector) may be specified. A separate command must be given for each sector or portion of a sector read.

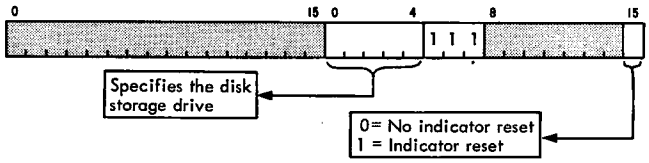
The word count and data words are transferred by means of data channel (cycle steal) operations. When the number of words specified has been read, an operation complete interrupt is given.

Modifier bit 8 controls the specific read operation; read or read check. If modifier bit 8 is off, a normal read-to-core-storage operation is performed as described in the preceding paragraphs. If modifier bit 8 is on, a read check operation is performed. A read check operation differs from a read-to-core-storage operation in that data read is not transferred to core storage but is simply checked for modulo 4 errors.

An XIO initialize read is treated as a no-op if given while the disk storage drive is busy or not ready.

READ ERRORS: The program should provide for repetition of XIO initialize reads that indicate any data transfer errors. These errors are often due to a temporary condition that is not present in subsequent retries.

Sense Device



This command causes the device status word (DSW) of the selected disk storage drive to be read into the accumulator. The DSW is shown in Figure 87.

Modifier bit 15 controls reset of the program resettable indicators in the DSW. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset.

1810 DSW Interrupt Indicator

Figure 87 shows the format of the 1810 DSW and defines interrupt and program resettable indicators.

OPERATION COMPLETE: This indicator turns on, causing an interrupt, after completion of a seek operation, or after the number of words specified by the word count has been read, read checked, or written. This indicator must be reset (XIO sense device with reset) before a new XIO initialize read, XIO initialize write, or XIO control is given.

1810 DSW Noninterrupt Indicators

Figure 87 shows the format of the 1810 DSW and defines noninterrupt and program resettable indicators.

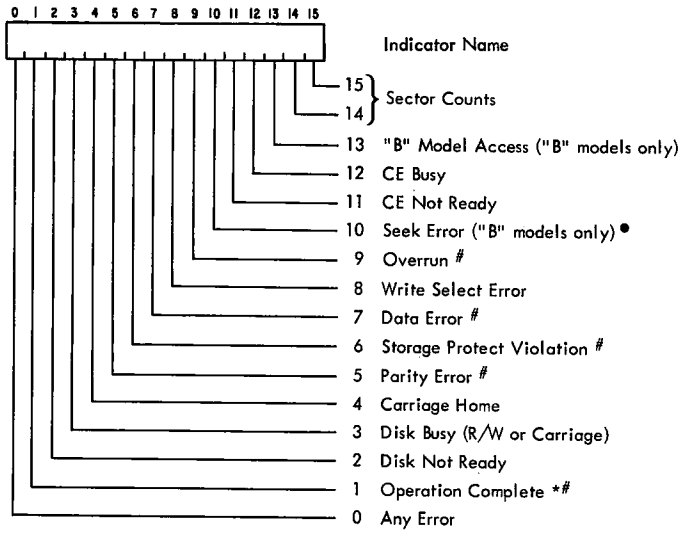


Figure 87. 1810 Device Status Word

ANY ERROR: This indicator turns on if any of the following indicators turns on: data error, parity error, storage protect violation, overrun, or a B-model seek error. The indicator turns off when all individual error conditions are reset.

DISK NOT READY: This indicator is on when the disk storage drive is busy, an 1810 interlock has not been properly satisfied, or the disk storage drive is in CE mode. The disk storage drive is unable to accept an XIO initialize read, XIO initialize write, or XIO control when this indicator is on. If one of these commands is given while disk not ready is on, it is treated as a no-op.

DISK BUSY (R/W Or Carriage): This indicator is on whenever the disk storage drive is in CE mode or is busy executing an XIO initialize read, XIO initialize write, or XIO control. If one of these commands is given while disk busy is on, it is treated as a no-op.

CARRIAGE HOME: This indicator is on when the carriage is positioned at cylinder 0 (home).

PARITY ERROR: This indicator turns on if a parity error is detected during data transfer to or from core storage and the disk storage drive.

STORAGE PROTECT VIOLATION: This indicator turns on if the disk storage drive attempts to read into a storage-protected core storage location. The read operation does not stop. However, protected storage remains unchanged.

DATA ERROR: This indicator turns on whenever a modulo 4 error is detected. It also turns on if a read or write operation is not completed before the next sector pulse is detected.

WRITE SELECT ERROR: This indicator turns on if a failure in the write selection circuitry which could result in loss of data is detected. The indicator can be turned off only by stopping the disk storage drive.

OVERRUN: This indicator turns on if the data channel fails to transfer data within the time the disk storage drive requires service.

SEEK ERROR (B-Models Only): This indicator turns on if an access operation is not completed within 200 ms. In this case, the indicator is turned off with the next valid seek command. The indicator also turns on if a cylinder address greater than 202 is specified. In this case the indicator is turned off by XIO sense device with reset.

CE NOT READY: When the disk storage drive is in CE mode, this indicator is used in place of the disk not ready indicator.

CE BUSY: When the disk storage drive is in CE mode, this indicator is used in place of the disk busy (R/W or carriage) indicator.

B-MODEL ACCESS (B-Models Only): This indicator identifies the disk storage drive as a B-model, which requires absolute cylinder addresses for seek operations.

SECTOR COUNTS: These three DSW bits identify the next pair of sectors that are available for reading or writing.

The IBM 2401/2402 Magnetic Tape Units (Figure 88) provide magnetic tape input/output capabilities for the 1800 system. The magnetic tape units attach to the system through a tape control unit provided only by the 1802 Processor-Controller (P-C).

A maximum of two 2401's (models 1, 2, or 3) or one 2402 (model 1, 2, or 3) can be attached to the tape control unit. The 2401 has a single tape drive, while the 2402 has two tape drives within a single unit. Both the 2401 and 2402 are nine-track tape units. However, a seven-track read/write head feature is available for both units. Intermixing of seven- and nine-track tape units is permitted.

FUNCTIONAL DESCRIPTION

A complete description of the 2401/2402 is presented in System/360 Components Description -- 2400 Series Magnetic Tape Units, Order No. GA22-6866. Figure 89 presents a summary of their characteristics.

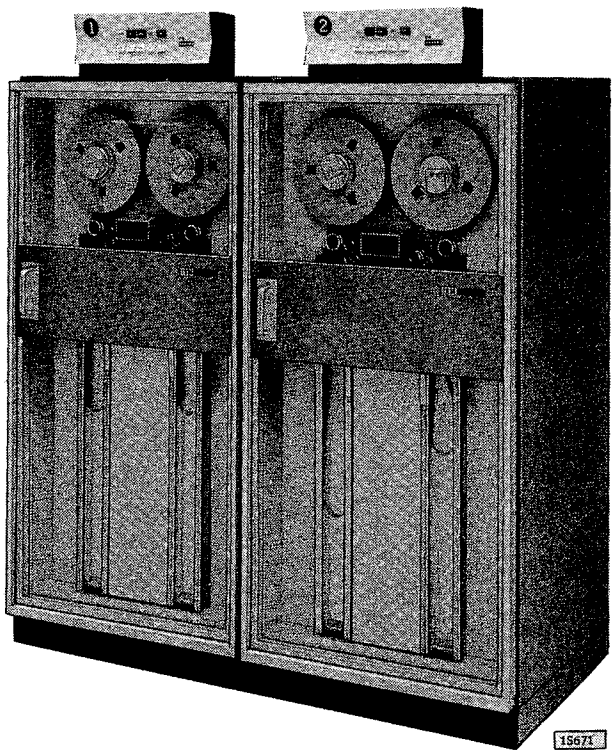


Figure 88. IBM 2401/2402 Magnetic Tape Unit

All buffering, and all logical and control functions necessary to operate the 2401/2402 are performed by the tape control unit in the 1802 P-C. The tape control unit operates on a data channel, and data transfers between core storage and the 2401/2402 are performed by means of data channel (cycle steal) operations.

Writing or reading magnetic tape, under program control, occurs as the tape is moved across a read/write head. Data is written by magnetizing small discrete areas on the tape in parallel channels called tracks. Data is read by sensing the presence or absence of the magnetized spots.

Tape control functions, such as backspace or rewind, can also be performed under program control and are used to position the tape to the desired point at which reading or writing is to start.

Tape Organization and Data Formats

Information on tape is made up of characters (known as bytes), which are used to form logical data records. Data records are usually arranged in blocks. A tape block may consist of one or more records. Blocks are separated by an interblock gap as shown in Figure 90. During writing, the gap is automatically produced at the end of a block. A block is therefore defined or marked by an interblock gap before and after the block.

Blocks of any practical size may be written. However, the minimum block length for writing is

Characteristics	Model 1		Model 2		Model 3	
Number of Tracks	7	9	7	9	7	9
Density (b/in.) Bits per Inch	800 556 200	800	800 556 200	800	800 556 200	800
Data Rate (bytes/sec)	30,000 20,850 7,500	30,000	60,000 41,700 15,000	60,000	90,000 62,500 22,500	90,000
Tape Speed (inch/sec)	37.50	37.50	75.00	75.00	112.50	112.50
Interblock Gap (inches)	0.75	0.60	0.75	0.60	0.75	0.60

17874

Figure 89. 2401/2402 Characteristics Summary

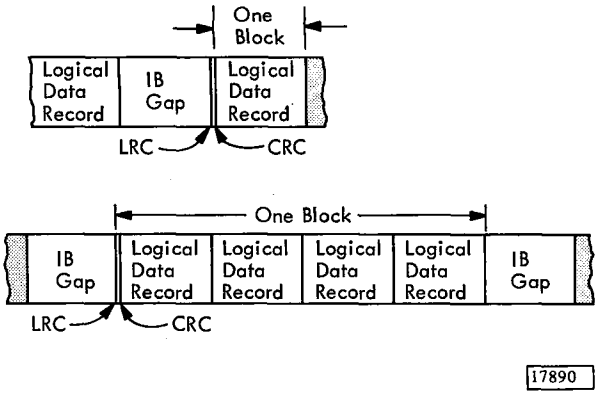
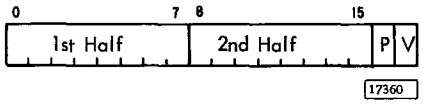


Figure 90. Tape Block Concept

18 bytes. The minimum block length for reading is 12 bytes.

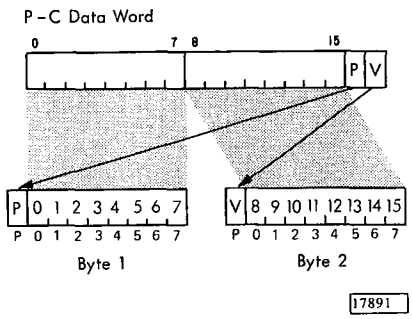
Each word transferred to or from the P-C consists of 16 data bits plus two parity bits (P and V) as follows:



The 16 data bits are read from or written into core storage while the two parity bits are transferred between only the B-register and the 2401/2402. P is a parity bit for data bits 0 through 7, and V is the parity bit for data bits 8 through 15.

Data Format (Nine-Track)

When reading or writing with nine tracks, each word is read from or written on the tape in two eight-bit bytes plus parity as follows:

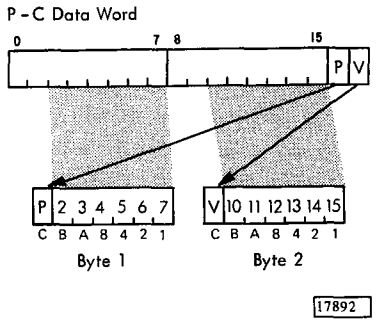


The P- and V-bits are read and written as the parity check bit for their respective bytes.

Data Formats (Seven-Track)

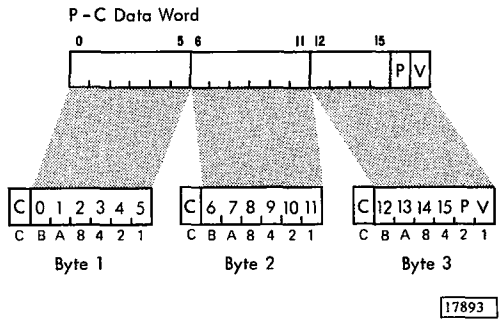
When reading or writing with seven tracks, an unpacked or packed mode of operation is available.

In unpacked mode, each word is read from or written on the tape as 2 six-bit bytes plus parity as follows:



The P- and V-bits are read and written as the parity check bit for their respective bytes. Note that data bits 0, 1, 8, and 9 are not used.

In seven-track packed format, each word is read from or written on the tape as 3 six-bit bytes plus parity as follows:



The P- and V-bits in this case are read and written as data bits even though each is a parity bit for one-half of the P-C word. The parity check bits (C) read and written are generated automatically for each of the three bytes and are not part of the P-C word.

Seven-track packed format is designed for use on 1800 systems only. Data written on other systems, such as the IBM 7090, cannot be read on an 1800

system unless the correct P- and V-bits are generated and written on the tape. Reading data containing incorrect P- and V-bits causes data words with incorrect parity to be placed into core storage and the parity error indicator in the 2401/2402 DSW to be turned on. When this data with incorrect parity is read out of core storage for processing, a parity error is detected, causing an internal interrupt that must be serviced.

Data Checking

To ensure validity of the data, various checking functions are performed when reading or writing magnetic tape. These checks are made in addition to parity checking of the data transfer between the P-C and 2401/2402.

Longitudinal Redundancy Check (LRC)

The longitudinal redundancy check monitors all tracks on the tape to ensure the presence of an even number of 1-bits in each track. As a block is written, an odd or even indication of the number of 1-bits in each track is automatically determined for each block. A check bit is written in each track at the end of the block to make the total number of 1-bits (including the check bit) in each track even. The vertical combination of these check bits is the LRC character.

When tape is read, either in a read operation or in a read-back check of a write operation, the same odd-even indication is determined for each track. The LRC check character is included in the calculation. If any track indicates an odd number of bits, an LRC error is indicated.

Vertical Redundancy Check (VRC)

The vertical redundancy check or parity check provides a means of checking for the proper number of one bits in each byte or character. One track on the tape contains the parity or check bit. During a read or read backward operation, or during a write or write tape mark operation, each byte is checked for an even number of 1-bits while operating in even-parity mode, and checked for an odd number of 1-bits while operating in odd-parity mode. (Nine-track tape is always written in odd parity.) If the number of 1-bits for each byte does not correspond to the parity mode, a VRC error is indicated.

Cyclic Redundancy Check (CRC)

The cyclic redundancy check is effective only in nine-track read and read backward operations, and serves as a means to correct single-track read errors. As a block is written, a special CRC character is automatically calculated from the data bytes and written on the tape after the body of the block (excepting the tape mark block), but before the LRC character. During a read operation, the CRC character is again calculated and compared with the CRC character written on the tape. If the two CRC characters do not agree, an error is indicated. In this case, the CRC character is used in determining the track in error.

Skew Check

During a write, write tape mark, or erase operation, bytes are checked for excessive skew (vertical bit alignment of a byte). If excessive skew occurs, a skew error is indicated.

Parity Mode (Seven-Track)

The 1800 can read or write seven-track magnetic tape in either even-parity or odd-parity mode. Modifier bit 15 of a XIO initialize read or XIO initialize write specifies the mode: 1 is even parity; 0 is odd parity. All nine-track operations are performed as odd parity only.

When reading or writing seven-track tape in even parity, the following facts should be noted about tape characters consisting entirely of 0's:

1. An all-0 tape character from core storage is written on tape as an A-bit and a C-bit.
2. A character containing only an A-bit and C-bit read from tape is placed in core storage as an all-0 character.
3. A character containing only an A-bit (@) from core storage is written on tape as an A-bit and a C-bit. Therefore, when this character is read back, it is placed back in core storage as an all-0 character.
4. No data error indication occurs if the A-bit and C-bit are transferred properly.

Tape Mark

A tape mark read from nine-track tape sets data word bits 3, 6, and 7 with odd parity.

A tape mark read from seven-track tape in unpacked mode sets data word bits 4, 5, 6, and 7 with even parity.

A tape mark read from seven-track tape in packed mode sets data word bits 2, 3, 4, and 5 with even parity.

Timings

Data channel (cycle steal) requests must be honored within an average of 16 μs to permit operation of 2401/2402 Magnetic Tape Units, Model 3, at the maximum data rate of 90,000 bytes per second. The tape control unit should be assigned to a data channel with high enough priority to ensure that data is not lost.

On systems with a selector channel and a 2401/2402 model 3, 2401/2402 operations cannot overlap selector channel operations.

When a tape drive is selected by an XIO sense device, a second XIO sense device must be given after a minimum interval of 5 μs to receive a valid indication of any of the following conditions:

1. Tape at load point.
2. Tape channel busy or rewinding.
3. Tape channel busy or not ready.
4. End-of-tape or tape mark.

Data Chaining

Magnetic tape operations can utilize the scan control facility to chain data tables together. This allows more than one data table to be treated as a single data table during read or write operations.

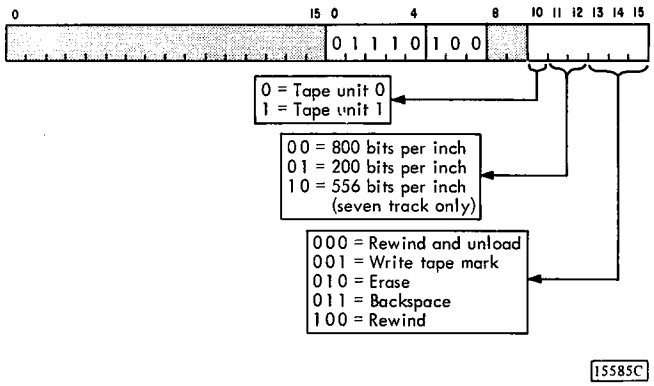
MAGNETIC TAPE PROGRAMMING

Magnetic tape operates under data channel control for data transfer and utilizes the execute I/O (XIO) instruction.

The input/output control command (IOCC) referenced by an XIO must have an area code of 01110 to select the tape control unit. The following IOCC's are used for operation and control of magnetic tape.

2401/2402 IOCC's

Control



This command, if accepted, causes the tape unit specified by modifier bit 10 to perform the control function specified by modifier bits 13 through 15. Tape unit device status word indicators marked with the symbol • in Figure 91 are also reset.

Modifier bits perform the following functions:

TAPE UNIT SELECT (Bit 10): This modifier bit selects the tape unit: 0 = tape unit 0, and 1 = tape unit 1.

DENSITY (Bits 11 and 12): These modifier bits specify the density as follows:

00 = 800 bits per inch.
01 = 200 bits per inch.
10 = 556 bits per inch.

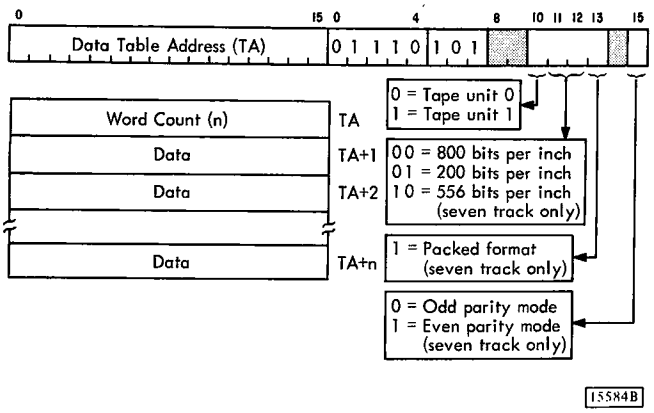
A density of 200 bits per inch should be used with any backspace control function.

CONTROL FUNCTION (Bits 13-15): These modifier bits specify the control function as follows:

000 = Rewind unload.
001 = Write tape mark.
010 = Erase.
011 = Backspace.
100 = Rewind.

If an XIO control is given to a tape unit not previously selected by an XIO sense device, or to a tape unit that is busy or not ready, the command is rejected and an interrupt is given.

Initialize Write



This command, if accepted, causes data in a table starting at the core storage location specified by the IOCC address word to be written on the tape unit specified by modifier bit 10. The command also resets certain device status word indicators, shown in Figure 91. The first word of the table contains the word count (n), which defines the number of data words to be written from the table, and the scan control bits.

The word count, scan control bits, and data words are transferred by means of data channel (cycle steal) operations. After the specified number of data words has been written, data channel operation continues as directed by the scan control bits. After the last word in the last data table has been transferred, an operation complete interrupt is given.

Modifier bits perform the four functions described next.

TAPE UNIT SELECT (Bit 10): This modifier bit selects the tape unit: 0 = tape unit 0, and 1 = tape unit 1.

DENSITY (Bits 11 and 12): These modifier bits specify the density as follows:

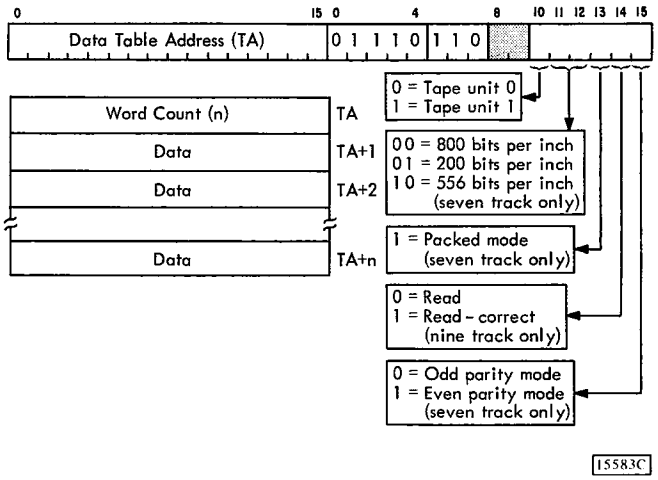
00 = 800 bits per inch.
01 = 200 bits per inch.
10 = 556 bits per inch.

FORMAT (Bit 13): This modifier bit specifies the format for seven-track operation: 0 = unpacked format, and 1 = packed format. This bit is ignored for nine-track operations.

PARITY MODE (Bit 15): This modifier bit specifies the parity mode for seven-track operation: 0 = odd parity, and 1 = even parity. This bit is ignored for nine-track operations.

If an XIO initialize write is given to a tape unit not previously selected by an XIO sense device, or to a tape unit that is busy or not ready, the command is rejected and an interrupt is given.

Initialize Read



If accepted, this command causes data to be read from the tape unit specified by modifier bit 10 and transferred to a table starting at the core storage location specified by the IOCC address word. Certain device status word indicators are also reset. (See Figure 91.) The first word of the table contains the word count (n), which defines the number of data words to be transferred to the table, and the scan control bits.

The word count, scan control bits, and data words are transferred by means of data channel (cycle steal) operations. After the specified number of data words has been transferred, data channel operation continues as directed by the scan control bits. After the last word in the last data table has been transferred, an operation complete interrupt is given.

Modifier bits perform the five functions described next.

TAPE UNIT SELECT (Bit 10): This modifier bit selects the tape unit: 0 = tape unit 0, and 1 = tape unit 1.

DENSITY (Bits 11 and 12): These modifier bits specify the density as follows:

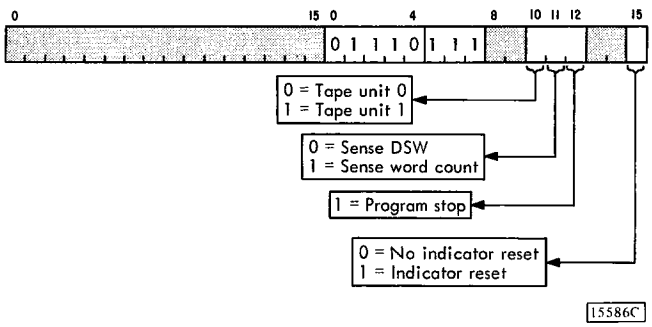
00 = 800 bits per inch.
01 = 200 bits per inch.
10 = 556 bits per inch.

FORMAT (Bit 13): This modifier bit specifies the format for seven-track operation: 0 = unpacked format, and 1 = packed format. This bit is ignored for nine-track operations.

READ MODE (Bit 14): This modifier bit specifies the type of read operation: 0 = normal read, and 1 = read while correcting. Read while correcting should always be used unless error correction is to be eliminated. This modifier bit is ignored for seven-track operation. It is also ignored during the first time a tape block is read (error not yet detected) for nine-track operation. See "Error Correction (Nine-Track)" for details.

PARITY MODE (Bit 15): This modifier bit specifies the parity mode for seven-track operation: 0 = odd parity, and 1 = even parity. This bit is ignored for nine-track operations.

Sense Device



This command may be used to:

1. Place a tape unit in selected mode.
2. Sense the tape unit device status word (DSW).
3. Reset program resettable DSW indicators.
4. Sense the word count.
5. Perform an operation stop to clear the data channel.

The modifier bits indicate the function, as described next.

TAPE UNIT SELECT (Bit 10): This modifier bit selects the tape unit: 0 = tape unit 0, and 1 = tape unit 1.

DSW Select (Bit 11): This modifier bit selects the word to be sensed: 0 = device status word, and 1 = channel word count.

PROGRAM STOP (Bit 12): This modifier bit is used to select program stop operation: 0 = no program stop operation, and 1 = program stop operation.

RESET (Bit 15): This modifier bit controls the reset of the program resettable indicators in the device status word: 0 = no indicator reset, and 1 = indicator reset.

The following paragraphs describe the various functions that may be performed with an XIO sense device.

TAPE UNIT SELECTION: Before a tape unit may be used, it must be placed in selected mode to prepare the unit for program operation. Tape unit 0 is automatically selected when P-C console RESET is pressed. Tape unit selection is changed by the XIO sense device.

Once a unit is selected, it remains selected until changed by another XIO sense device.

If an attempt is made to select a tape unit while the other is selected and busy, the busy tape unit remains selected. Bit position 1 of the DSW will show that the selection remained unchanged.

SENSE DSW: If modifier bit 11 is off, an attempt is made to select the tape unit specified by modifier bit 10, and the DSW of the selected tape unit is read into the accumulator. The DSW is shown in Figure 91.

Modifier bit 15 controls reset of the program resettable DSW indicators. If modifier bit 15 is on, the indicators are reset. If modifier bit 15 is off, the indicators are not reset.

The indicators identified by DSW bits 12, 13, 14, and 15 require a minimum of 5 μs from selection of the tape unit before their status can be accurately placed in the DSW. Therefore, if the status of these indicators is desired, the XIO sense device that reads the DSW must be given at least 5 μs after the XIO sense device that selects the tape unit.

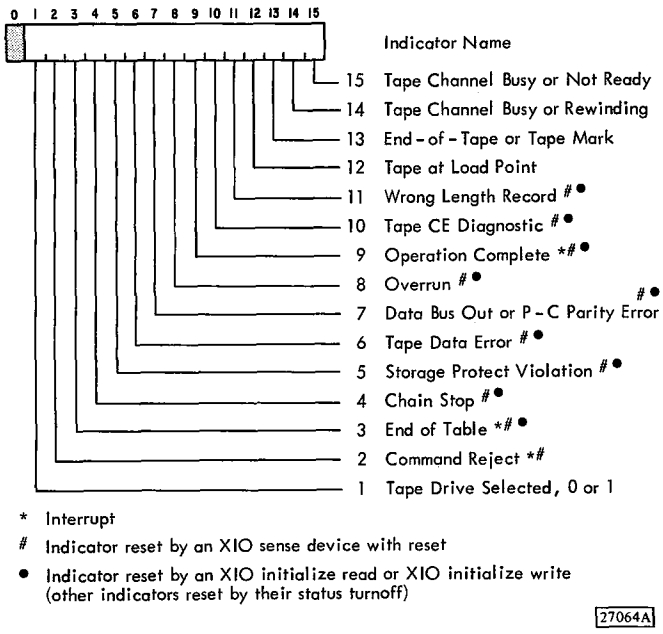


Figure 91. 2401/2402 Device Status Word

The DSW should be sensed and checked after each read or write because tape errors do not cause interrupts.

SENSE WORD COUNT: If modifier bit 11 is on, the channel word count is read into the accumulator, and modifier bits 10 and 15 are ignored. The channel word count, which is in bit positions 2 through 15, gives the word count difference if the number of data words on magnetic tape did not equal the word count of the command. If the tape block is longer than the command word count, the channel word count is in true form. If the tape block is shorter than the command word count, the channel word count is in 1's complement form. The form can be determined by interrogating bits 0 and 1:

Bit Positions 0 and 1	Word Count
00	True binary form
11	1's complement form

OPERATION STOP: If modifier bit 12 is on, an operation stop is performed by setting the word count to 0. In addition, the other functions specified are performed.

2401/2402 DSW Interrupt Indicators

Figure 91 shows the format of the 2401/2402 DSW and defines interrupt and program resettable indicators.

COMMAND REJECT: This indicator turns on, causing an interrupt, if an XIO initialize read, XIO initialize write, or XIO control is rejected for one of the following reasons:

1. Addressed unit busy or not ready.
2. Attempt to write on file protected unit (includes tape mark or erase).
3. Backspace or rewind when already at load point.
4. Parity error (P-C or out bus) while initiating commands.
5. Command given for unselected unit.

If a command is rejected because the tape drive is not ready, the rejected command will combine with command reject to set operation complete. If the command is rejected for other reasons, command reject will be set without operation complete. Any operation in progress will set operation complete at its normal time.

END OF TABLE: This interrupt occurs, if requested by the scan control bits, when the specified word count on a magnetic tape I/O operation becomes equal to 0.

When chaining, with an interrupt after each table, and using short tables and a long interrupt subroutine, a subsequent interrupt may be lost if it occurs before the DSW indicator is reset.

OPERATION COMPLETE: This interrupt occurs at the completion of a write tape mark, read, write, erase, or backspace operation. This interrupt also occurs immediately after the initiation of a rewind or rewind unload operation.

2401/2402 DSW Noninterrupt Indicators

Figure 91 shows the format of the 2401/2402 DSW and defines noninterrupt and program resettable indicators.

TAPE UNIT SELECTED: This indicator specifies which of two possible tape units is currently selected by the tape control, 0 or 1.

CHAIN STOP: This indicator turns on if a parity error (P-C or out bus) occurs while loading the channel address register or word counter during chaining and not during initializing. An XIO initialize write operation is terminated at this point and an operation complete interrupt occurs. Any transfer of data for

an XIO initialize read operation will be terminated although the operation complete interrupt does not occur until an interblock gap is encountered.

STORAGE PROTECT VIOLATION: This indicator turns on if a tape read operation attempts to store data into a storage-protected location. The transfer of data is terminated, although the tape proceeds to the interblock gap.

TAPE DATA ERROR: This indicator turns on if any of the following read or write checks is detected:

1. Read/write VRC error.
2. Write high-clip VRC error.
3. Write-no-echo error or read lost character.
4. Write skew error.
5. Read/write LRC error.
6. Read CRC error.

During reading of seven-track tape in packed format, a tape error can cause bad parity in core storage. If this occurs, a parity error occurs when the data with bad parity is read from core storage. This error causes an internal interrupt condition.

DATA BUS OUT OR P-C PARITY ERROR: This indicator turns on if a P-C parity error is detected on the out bus or in bus, or if an out bus parity error is detected by the tape control unit.

OVERRUN: This indicator turns on if the data channel fails to transfer data in the time the 2401/2402 requires service.

TAPE CE DIAGNOSTIC: This indicator is for the customer engineer's use as a modifier of tape data error indicators. It turns on if any one of the following tape control checks is detected:

1. Read high-clip VRC check.
2. Read clock VRC check.
3. Write clock VRC check.
4. Delay counter VRC check.

WRONG LENGTH RECORD: This indicator turns on if the number of words of data read from magnetic tape in an XIO initialize read operation is not identical to the programmed word count, or if a tape mark is encountered during an XIO initialize read operation. This indicator also comes on if a record block on tape does not contain byte multiples exactly matching the total of P-C words. In this case, one or more extra bytes are added to fill up the last P-C word, and this complete word is transferred to core storage with the word counter counting this last word.

TAPE AT LOAD POINT: This indicator turns on if the tape is physically at load point. Since the first block written on a tape has an extra-long block gap preceding it, this indicator will not be on after a backspace has positioned the tape at the beginning of the first block. This indicator is reset only by the tape physically leaving the load point. Care must be taken to ensure that the tape unit sensed is the tape unit desired by the programmer.

END-OF-TAPE OR TAPE MARK: This indicator turns on if end-of-tape is sensed during an XIO initialize read, XIO initialize write, write tape mark, or if a tape mark has been read during an XIO initialize read operation. This indicator is not set by tape marks encountered during an XIO initialize write, write tape mark, erase, or backspace operation.

If only a tape mark was sensed, this indicator is reset by an accepted XIO initialize read, XIO initialize write, or XIO control. It can also be reset by a XIO sense device. To reset the indicator if end-of-tape is sensed, it is necessary to perform one of the following tape operations: (1) backspace (even if the backspace does not encounter end-of-tape indicator), (2) rewind, or (3) rewind unload.

Reading a tape mark always causes the wrong length record indicator to be set. Sensing end-of-tape does not stop the transfer of data and therefore does not cause the wrong length record indicator to be set unless a short or long record condition also exists.

TAPE CHANNEL BUSY OR REWINDING: This indicator turns on during an XIO initialize read, XIO initialize write, write tape mark, erase, or backspace operations. The indicator is also on during rewind and rewind unload operations after initialization of these operations. Care must be taken to ensure that the tape unit sensed is the tape drive desired by the programmer.

TAPE CHANNEL BUSY OR NOT READY: During XIO initialize read, initialize write, write tape mark, erase, and backspace operations, the tape unit is considered to be ready and busy. During rewind and rewind unload operations, the tape unit is considered to be not ready and not busy. Accordingly, the tape channel busy or not ready indicator is on during all of the aforementioned operations. This indicator is also on if the tape unit is not physically ready. Care must be taken to ensure that the tape unit sensed is the tape unit desired by the programmer.

Error Correction (Nine-Track)

An XIO initialize read can automatically recover any number of errors (pick-ups or dropouts) on any one

track, if modifier bit 14 of the IOCC is on. However, for this automatic error correction to work, a certain type of read retry procedure is required. This procedure intermixes a number of read retries on one block with moving tape to another block (which is usually backward past the tape cleaner), then moves back to the desired block for more read retries. The standard recovery procedure is to first read a block; then, if errors exist, backspace and read-correct (read with modifier bit 14) each block up to ten times. Finally, if errors still exist, perform five backspaces (equal to 3" with minimum blocks) to ensure that the tape block desired has moved past the tape cleaner and to ensure that the error-correction circuitry has been reset (requires two backspaces).

For the first block on the tape (where backspacing two blocks is not possible), tape block movement has to be replaced by temporarily selecting the opposite tape unit through an XIO sense device for error correction to function. This may be done even when there is only one tape unit attached.

The next step is to move tape forward by reading blocks with a word count of 0 to reach the beginning of the desired block and continue the standard recovery procedure with read-correct until tape block movement past the cleaner is required again. Repeat this procedure up to 9 times for a total of 100 read-correct operations before concluding that a block is not correctable.

In some cases, the 10 read-corrects on the same block can be reduced, but not reduced to less than 3. The 10 block movements past the tape cleaner can also be reduced, but not reduced to less than 2.

2401 and 2402 Usage Meters

These meters run when both of the following conditions are present:

1. The tape unit is selected for operation by the program.
2. The P-C is running.

Communications Adapter

INTRODUCTION

The communications adapter (CA) extends the capabilities of the 1800 system by permitting communications with other systems that have appropriate communications attachments. The functional characteristics of the CA comply with the conventions established for binary synchronous communications (BSC). This compliance makes the CA compatible with the following:

- System/360 with synchronous data adapter II of the 2701 Data Adapter Unit.
- System/360 with 2703 Transmission Control Unit.
- 1130 system with synchronous communications adapter.
- Other 1800 systems with the CA feature.
- 2770 Data Communications System.
- 2780 Data Transmission Terminal and other BSC devices.

For the user not familiar with data communications, the following manuals are referenced:

IBM Data Communications Primer, Order No. GC20-1668
IBM Binary Synchronous Communications, Order No. GA27-3004

The CA provides half-duplex, synchronous (by bit and by character) data transmission over private or leased voice-grade lines, or switched telephone networks. Either two-wire or four-wire connections may be used. The CA may also operate in full-duplex mode, thus reducing line turnaround delays, but message transmission is half-duplex only (transmission in one direction at a time). In dial-up network operation, the CA will automatically answer calls originated by a remote station (auto-answer function).

Selectable Features and Options

NUMBER OF LINES: Up to four CA basic units may be attached to an 1800 system. Either one or two communications lines (line adapters) can be attached to the CA basic unit, thus giving a maximum of eight communications lines, all of which may operate simultaneously.

TRANSMISSION CODE: Either American National Standard Code for Information Interchange (ASCII) normal or Extended Binary-Coded-Decimal Interchange Code (EBCDIC) normal and transparent may be selected as the transmission code. Both line adapters on a CA must use the same code.

CLOCKING: Either business machine or data set clocking may be specified. Choice of clocking is dependent on the data set. However, the clocking (business machine or data set) must be identical in all stations on a communications link.

LINE SPEED: Either line adapter may be assigned a speed of 600 (World Trade Corporation only), 1,200, 2,000, 2,400 or 4,800 baud. Choice of speed is dependent on the data set and quality of lines used.

TRANSMISSION MODE: Either line adapter may be assigned transmit controlled carrier or continuous carrier operation. Continuous carrier operation is permitted on four-wire communications links only.

PRIMARY OR SECONDARY STATION: Either line adapter may be assigned as a primary or secondary station. The receive timeout for the primary station occurs at 2.7 seconds; the timeout at the secondary occurs at 3 seconds. This option assists in breaking equipment contention, which can occur when two stations attempt to transmit simultaneously.

DATA CHANNEL: Each line adapter may be assigned to a separate data channel. For concurrent operation of both line adapters, they must be assigned to separate data channels.

CA READY: This option may be installed in either line adapter to prevent disconnecting a dial-up data set when the line is deinitialized. This is an aid to program debugging and may be left installed if program disconnect is not required.

Auto-Answer Function

This function, providing the controls necessary to give "off-hook" and "hang-up" indications, allows a

line adapter to automatically answer incoming calls on switched networks.

Outgoing calls are initiated manually. No provision for automatic calling is available.

Data Set Interface

The line-adapter-to-data set interface conforms to the Electronic Industries Association (EIA) RS-232C Standard.

FUNCTIONAL DESCRIPTION

Each line adapter functions as an I/O control between the P-C and the transmission line. The line adapter is fully controlled by execute I/O (XIO) instructions, data chaining, and recognition of the data link control characters that it receives from communications networks or the P-C.

A line adapter can start transmitting or receiving only after being properly initialized by an XIO. After being initialized, the line adapter monitors data received from the remote station or the P-C for control characters and performs the proper action when they are detected.

Data transfer to and from core storage by means of data channel (cycle steal) operation begins after generation and recognition of a sync pattern.

The data to be transmitted is stored two characters (bytes) per core storage word. As many as 4,095 bytes may be used to construct a data table. Data transfer ends after recognition of an end control character or program reset, or when the end of the data table is reached and data chaining is not specified by the scan control.

The P-C and its program control and initiate all operations within a line adapter and are responsible for:

- Proper sequencing of commands.
- Translation to and from data codes.
- Interpreting sense and status information.
- Initiating and terminating operations.
- Proper message and control format.
- Recognizing control characters.

Data Flow

In transmit mode, data flow is from core storage to the eight-bit common bus, to the nine-bit serializer/deserializer (SERDES), to the data set, to the communications line (Figure 92). Each 16-bit core storage word constitutes two 8-bit characters. When the byte counter contains an even count, the high order

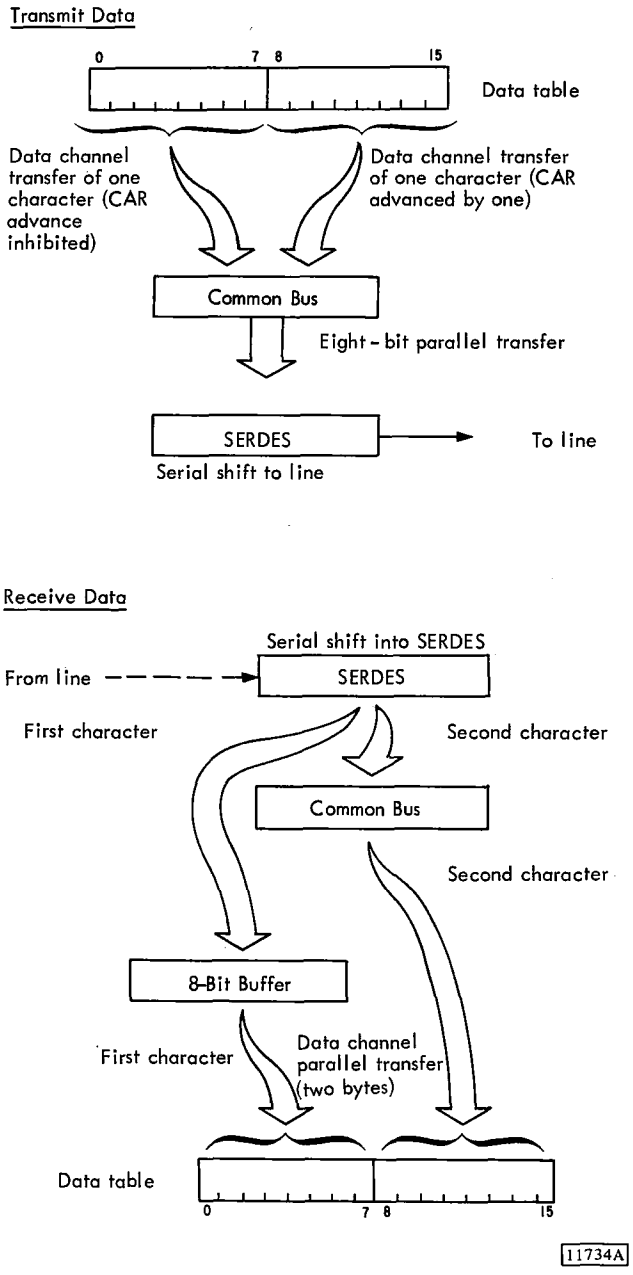


Figure 92. CA Data Flow

character (bit positions 0 through 7) is transferred to the common bus, and the channel address register (CAR) is not advanced. When the byte counter contains an odd count, the low order character (bit positions 8 through 15) is transferred to the common bus, and the CAR is advanced.

In receive mode, data flow is from the communication line to the data set, to the SERDES, to the common bus or eight-bit buffer register, to core storage. The 8-bit buffer is used to pack two 8-bit characters into one 16-bit core storage word. When the byte counter contains an even count, the eight-bit buffer is loaded from the SERDES and the channel address register (CAR) is not advanced. When the byte counter contains an odd count, the character in the SERDES is transferred via the common bus to core storage, along with the character in the eight-bit buffer, and the CAR is advanced.

Data transfer between core storage and SERDES is parallel by byte and serial by character. Data transfer between SERDES and the communications line is serial by bit.

CA Transmission Code

The CA uses either EBCDIC (Figure 93) or ASCII (Figure 94) for transmission code. Both codes utilize eight bits per character. (ASCII uses seven bits plus a parity bit.) Because a core storage word consists of 16 data bits, CA characters are packed two characters per word in core storage; one character in bit positions 0 through 7 and one character in bit positions 8 through 15. All characters are transmitted low order bit first as follows:

	Bit Positions							
Core Storage Word	0	1	2	3	4	5	6	7
	8	9	10	11	12	13	14	15
EBCDIC	0	1	2	3	4	5	6	7
ASCII	P	7	6	5	4	3	2	1

First Bit to Line

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Control Characters

Ten communications control characters provide the control character set to implement control functions.

Communications control characters and sequences defined for the BSC system are listed in Figure 95 and described in the following paragraphs.

SOH (Start of Heading): SOH is used as the first character in a block of heading data in a message. A heading may consist of a series of noncontrol characters, which may be used to process the text portion of a message. If a heading is subdivided into shorter transmission blocks by use of ETB or ITB, SOH is used to start any block that continues the transmission of the heading. Use of SOH following ITB is optional, but should be used only if the block ended by ITB was heading.

STX (Start of Text): STX is used to indicate the start of the text portion of a message and to terminate a heading. Text is that portion of a message treated as an entity to be transmitted to a remote station without change. If text is subdivided into shorter transmission blocks by use of ETB, STX is also used to start each block of text that continues transmission of the text. Use of STX at the start of a text block following an ITB is optional.

ITB (Intermediate Transmission Block): ITB is used to block data by indicating end of intermediate text or heading without causing line turnaround. Block check characters (BCC) are immediately transmitted following an ITB. Another message block follows the ITB and BCC. SOH or STX may be included or omitted as the first character of the block following an ITB, provided the type of information (heading or text) in the two blocks is the same. However, SOH normally does not follow a previous text block, only a previous heading block.

ETB (End of Transmission Block): ETB is used to indicate the end of a transmission block which is not the end of the message. ETB is followed immediately by the BCC's and calls for a response from the receiving station. After an affirmative response, transmission of the message is resumed with an SOH or STX, depending on whether the ETB came within the heading, between the heading and text, or within the text.

ETX (End of Text): ETX is used to terminate a text or message. ETX is followed immediately by the BCC's and calls for a response from the receiving station. After an affirmative response, transmission may continue with SOH or STX. ETX should not be used to terminate a heading.

Bit Positions 0, 1, 2, 3 → / 4, 5, 6, 7 ↓	Hex	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0	NUL	DLE	DS		SP	&	-	ACK0								0
0001	1	SOH	DC1	SOS				ACK1	F1	a	j			A	J		1
0010	2	STX	DC2	FS	SYN				F2	b	k	s		B	K	S	2
0011	3	ETX	DC3						F3	c	l	t		C	L	T	3
0100	4	PF	RES	BYP	PN				F4	d	m	u		D	M	U	4
0101	5	HT	NL	LF	RS				F5	e	n	v		E	N	V	5
0110	6	LC	BS	EOB / ETB	UC				F6	f	o	w		F	O	W	6
0111	7	DEL	IL	PRE / ESC	EOT				F7	g	p	x		G	P	X	7
1000	8		CAN						F8	h	q	y		H	Q	Y	8
1001	9	RLF	EM						\	i	r	z		I	R	Z	9
1010	A	SMM	CC	SM		¢	!		:								LVM
1011	B	VT	CU1	CU2	CU3	.	$	WACK	#								
1100	C	FF	IFS		DC4	<	*	%	@ RVI								
1101	D	CR	IGS	ENQ	NAK	(	)	—	'								
1110	E	SO	IRS	ACK		+	;	>	=								
1111	F	SI	IUS	BEL	SUB	!	¬	?	"								PAD Char

	Bit Positions
Core Storage	0 1 2 3 4 5 6 7
Word	8 9 10 11 12 13 14 15
EBCDIC	0 1 2 3 4 5 6 7

Last bit to line

First bit to line

Note: IUS character (/1F) performs the intermediate transmission block (ITB) function.

Control function when preceded by DLE

Duplicate assignment

Control characters

Turnaround characters when preceded by DLE (not used by MPX)

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Figure 93. EBCDIC (as used in Binary Synchronous Communications)

Bit Positions P, 7, 6, 5 → / 4, 3, 2, 1 ↓	Hex	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0		DLE	SP		@			P	NUL			0 ACK0		P	\	
0001	1	SOH			1 ACK1		Q	a			DC1	!		A			q
0010	2	STX			2		R	b			DC2	"		B			r
0011	3		DC3	#		C			s	ETX			3		S	c	
0100	4	EOT			4		T	d			DC4	$		D			t
0101	5		NAK	%		E			u	ENQ			5		U	e	
0110	6		SYN	&		F			v	ACK			6		V	f	
0111	7	BEL			7		W	g			ETB	'		G			w
1000	8	BS			8		X	h			CAN	(		H			x
1001	9		EM	)		I			y	HT			9		Y	i	
1010	A		SUB	*		J			z	LF			:		Z	¡	
1011	B	VT			; WACK		[	k			ESC	+		K			{
1100	C		FS	,		L			¦	FF			< RVI		—	¦	
1101	D	CR			=		]	m			GS	-		M			}
1110	E	SO			. >		¬	n			RS	.		N			~
1111	F		US	/		O			DEL	SI			?		—	o	PAD Char

	Bit Positions
Core Storage	0 1 2 3 4 5 6 7
Word	8 9 10 11 12 13 14 15
ASCII	P 7 6 5 4 3 2 1

Last bit to line

First bit to line

Control function when preceded by DLE

Control characters

Turnaround characters when preceded by DLE (not used by MPX)

Note: US character (/1F) performs the intermediate transmission block (ITB) function.

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Figure 94. ASCII (as used in Binary Synchronous Communications)

Name of Function	Functional Mnemonic	Code Realization EBCDIC	Code Realization USASCII
Start of Heading	SOH	SOH	SOH
Start of Text	STX	STX	STX
End of Transmission Block	ETB	ETB	ETB
End of Text	ETX	ETX	ETX
End of Transmission	EOT	EOT PAD[3]	EOT PAD[3]
Enquiry	ENQ	ENQ	ENQ
Negative Acknowledge	NAK	NAK PAD[3]	NAK PAD[3]
Synchronous Idle	SYN	SYN	SYN
Data Link Escape	DLE	DLE	DLE
End of Intermediate Transmission Block	ITB	IUS	US
Even Acknowledge	ACK0	DLE (70)[1]	DLE0
Odd Acknowledge	ACK1	DLE/	DLE1
Wait Before Transmit-positive Acknowledge	WACK	DLE,	DLE;
Mandatory Disconnect[2]	DISC	DLE EOT[3,4]	DLE EOT[3,4]
Reverse Interrupt	RVI	DLE @	DLE <
Temporary Text Delay	TTD	STX ENQ	STX ENQ
Transparent Start of Text	XSTX	DLE STX	
Transparent Intermediate Block	XITB	DLE IUS	
Transparent End of Text	XETX	DLE ETX	
Transparent End of Trans. Block	XETB	DLE ETB	
Transparent Synchronous Idle	XSYN	DLE SYN	
Transparent Block Cancel	XENQ	DLE ENQ	
Transparent TTD	XTTD	XSTX XENQ	
Data DLE in Transparent Mode	XDLE	DLE DLE	

Notes: 1. Hexadecimal representation (no control or graphic assignment).
2. For switched data link only.
3. The four low-order bits of trailing PAD are required for detection of control character.
4. EOT performs normal function. DLE is ignored.

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Figure 95. Control Characters and Sequences

EOT (End of Transmission): EOT is used to terminate transmission and is the only means of ending message transfer. Any valid EOT transmitted or received terminates transmission immediately and does not call for a response. A valid EOT is defined as a SYN SYN EOT PAD sequence.

ENQ (Enquiry): ENQ is used to request a reply from a remote station. In point-to-point operation, ENQ is used by a transmitting station to bid for a line. If the transmitting station receives an affirmative response, transmission may begin.

NAK (Negative Acknowledgement): NAK is used by a receiving station as a negative response to a transmitting station. A valid NAK is defined as a NAK PAD sequence. A NAK response to a message block transmission indicates that the block was received in error. NAK is also the not-ready reply to a station selection.

SYN (Synchronous Idle): SYN characters are automatically generated by the line adapter and are used to establish synchronism and to maintain synchronism is absence of any other character. In normal mode, the program can insert SYN characters for time fills (up to 2.5 seconds only).

DLE (Data Link Escape): DLE is used to provide additional line control characters by indicating the start of a contiguous two-character sequence.

PAD: Two PAD characters are used by the line adapter: pre-SYN PAD and end PAD. The pre-SYN PAD is provided automatically by the line adapter and precedes the SYN SYN sequences at the start of each transmission. Pre-SYN PAD characters (/55) are used to establish bit phase.

End PAD character (/FF) must be provided by the program and must follow any control character or sequence that initiates line turnaround.

Control Sequences

Control sequences are formed by two contiguous control characters and are used for additional control functions not defined by single control characters. The sequences are: transparent mode control, standard affirmative reply, and turnaround. Transparent mode control sequences are described under "Transparent Mode Control." The remaining sequences are described in the following paragraphs.

STANDARD AFFIRMATIVE REPLIES: In normal data exchange, it is customary to acknowledge each received message block with an affirmative reply. If the reply cannot be positive because the received message was faulty, a NAK must be used as the reply.

For a positive reply, odd-numbered messages (first, third, fifth, and so on) are acknowledged with ACK1, and even-numbered messages are acknowledged with ACK0. A third positive acknowledgment is WACK, which indicates to the transmitting station that the receiver has a temporary not-ready condition. The fourth positive reply is RVI, which requests that data transmission be reversed so that an important message can be sent by the receiving station.

Standard replies are composed of a DLE as the leader, followed immediately by specific bit combinations as the trailer. (See Figure 95.) Standard replies as well as NAK are not recognized if SOH or STX has been previously detected in the message stream.

Standard replies as well as NAK cause an end-character-decoded interrupt allowing the program to initiate line turnaround.

TURNAROUND SEQUENCES: These sequences are used to cause an end-character-decoded interrupt, thus allowing the program to initiate line turnaround.

Turnaround sequences are formulated by a DLE as the leader, followed immediately by any of the turnaround characters indicated in Figures 93 and 94.

The character sequence DLE turnaround can be used as an acknowledgment to which a special meaning may be assigned by prior agreement.

Turnaround character sequences are not recognized if SOH or STX has been previously detected in the message stream.

Data Transmission Checking

Data checking is based upon transmission of additional information with each transmission block of data (heading and/or text blocks). This extra information permits error detection by the receiving station. This information is called a block check character (BCC). The three checking methods used to generate BCC's are described next.

CYCLIC REDUNDANCY CHECK (CRC-16): This checking is performed automatically by the line adapter and is used only with EBCDIC in both normal and transparent modes. CRC produces a 16-bit check character by an arithmetic accumulation of the message bits for each transmission block. This 16-bit CRC character is transmitted as two contiguous BCC's immediately following the end-of-block character. The receiving station also produces its own CRC character using the same method. This 16-bit CRC character is compared for agreement with the two BCC's received. If they do not agree, a BCC error is set in the device status word.

CRC accumulation begins following the first appearance of an SOH or STX in normal mode or an SOH or DLE STX in transparent mode. The SOH, STX, or DLE STX is not included in the accumulation. CRC accumulation ends with and includes the end-of-block character (ITB, ETB, or ETX). If ITB is the end-of-block character, CRC accumulation for the next block begins automatically without an SOH or STX. All characters transmitted or received during accumulation are included, except those characters that are not sent to core storage at the receive station. These characters are: SYN SYN, DLE SYN, or first DLE in DLE DLE sequence.

VERTICAL REDUNDANCY CHECK (VRC): VRC is performed automatically by the line adapter and is used only with ASCII in normal mode. This code structure defines an eighth bit to provide odd parity for each character. A vertical redundancy check (parity) is performed on each character; if its parity is not odd, data parity error is set in the device status word. The VRC check is made on all transmissions: responses, control sequences, headings, and text.

LONGITUDINAL REDUNDANCY CHECK (LRC): LRC is performed automatically by the line adapter and is used only with ASCII in normal mode. The LRC character is an eight-bit character. It consists of the bits necessary to make the total number of 1-bits even in each individual bit level of the code for the entire transmission block. The LRC character is transmitted as one BCC immediately following the end-of-block character. The receiving station produces its own LRC character, which is compared for agreement with the BCC received. If they do not agree, a BCC error is set in the device status word.

LRC accumulation begins after the first appearance of an SOH or STX. The first SOH or STX is not included in the accumulation. LRC accumulation includes and ends with the end-of-block character (ITB, ETB, or ETX). If ITB is the end-of-block character, LRC accumulation for the next block begins automatically without an SOH or STX. All characters transmitted or received during accumulation are included except those characters that are not sent to core storage (SYN SYN).

Transparent Mode Control

Transparent mode allows the full 256 EBCDIC character codes to be transmitted as text. Transparent mode is used when binary information, or external codes are to be transmitted or received. No provision for transparent mode operation using ASCII is provided.

A line adapter enters transparent mode after a DLE STX sequence. In transparency, a transmitting line adapter inserts a second DLE after each data DLE received from core storage. For example, a DLE ETB sequence transmitted during transparent mode appears as a DLE DLE ETB sequence, and the control character sequence of DLE ETB is not recognized. At the receiver, the DLE preceding the inserted DLE is deleted and not sent to core storage.

A line adapter leaves transparent mode when a single DLE followed by an ITB, ETB, ETX, or ENQ

is detected. Exit from transparent mode is accomplished by placing a DLE followed by an ITB, ETB, ETX, or ENQ in the next-to-last word of a transmit data table. When the line adapter receives the DLE from core storage, the byte counter is decreased to 3. The combination of a DLE and a byte count of 3 prevents insertion of the additional DLE. Therefore, a control sequence is detected.

DLE SYN sequences are used to maintain synchronism in transparent mode in place of SYN SYN sequences used in normal mode. Frequency of insertion depends on the line speed. DLE SYN sequences cannot be used by the program as time fills in transparent mode.

Timeout Controls

Timeouts are used to ensure efficient utilization of the communications line and to prevent tie-ups due to false sequences or missed turnaround characters.

Some timeout conditions cause an interrupt, but the program has the option to suppress the timeout interrupt.

TRANSMIT TIMEOUT (No Interrupt): This timeout is used to automatically insert the synchronous idle sequence in the output data stream as follows:

1. In normal mode, and also in transparent mode with external clocking, a SYN SYN or DLE SYN sequence is inserted every 1.00 (±0.15) sec.
2. In transparent mode with business machine clocking, a DLE SYN sequence is inserted at one of several possible intervals, depending on the line speed:

   600 baud: 900 (±100) ms (WTC only)
   1200 baud: 475 (±50) ms
   2000 or
   2400 baud: 255 (±25) ms
   4800 baud: 106 (±12) ms

In either case, insertion of the synchronous idle sequence is delayed if insertion would occur between:

- A DLE and its following control character.
- An ITB character and the following BCC's.
- The block check characters (BCC's).

In the case of all non-ITB ending sequences, insertion is abandoned. Timeout is restarted when the synchronous idle sequence (SYN SYN or DLE SYN) is detected in the message stream.

TIMEOUT (Interrupt): This timeout has the following purposes:

- Limits the waiting time allowed for a transmitting station to receive a reply (3 seconds).
- Monitors incoming or outgoing data for SYN patterns. A timeout interrupt will occur in 3 seconds if any of the following conditions occur in the data stream:
  1. A (SYN SYN) sequence is not decoded in normal mode.
  2. Continuous SYN characters are decoded in normal mode.
  3. A DLE SYN sequence is not decoded in transparent mode.
  4. Continuous DLE SYN sequences are decoded in transparent mode.
- Causes a timeout interrupt if the data set fails to respond to a request-to-send with a clear-to-send within 3 seconds.

The timeout interrupt can be changed to a nominal 2 seconds by issuing an XIO initialize write or XIO sense device, and specifying continue timer (modifier bit 10 on) in either case. If this is done, the timeout is changed from 3 seconds to 2 seconds and the timer is started. The new timeout period remains effective until changed by one of the following events:

1. A timeout interrupt occurs.
2. A change from receive to transmit, or vice versa, occurs because of data table chaining or another XIO initialize write.
3. An XIO initialize write or XIO sense device with modifier bit 12 (clear CA) on is given.

A timeout interrupt can be suppressed if bit 3 of the data table byte count word is on.

Actual time periods for timeout interrupt are:

Time Period	Secondary Station	Primary Station
3-second timer	3.0 seconds	2.7 seconds
2-second continue timer	2.0 seconds	1.9 seconds
all times ± 100 milliseconds		

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LINE ADAPTER INITIALIZATION

Before a line adapter can transmit or receive information, it must be initialized to a state in which it is

either seeking characters received from the line or seeking characters from core storage to transmit on the line.

Initializing is started by an XIO initialize write. This command defines the line adapter to be initialized and a data table in core storage. The first word of the data table contains scan control bits, line adapter control bits, and the byte count associated with the data table. This word (Figure 96) is transferred to the line adapter by means of data channel (cycle steal) operations and is used to complete initialization of the line adapter. The various functions the information in this word performs are described in the following paragraphs.

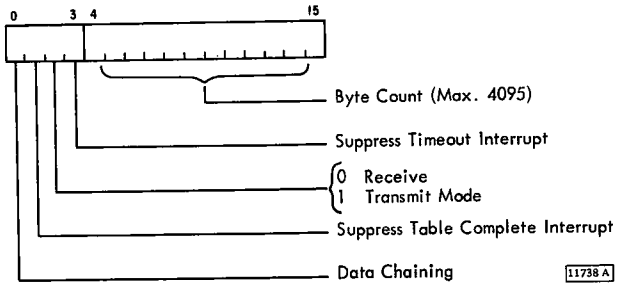

Figure 96. CA Byte Count Word

Scan Control

The scan control bits (0 and 1) perform the normal functions of data chaining control and table complete interrupt control. These two functions are described next.

DATA CHAINING: When this bit is on, automatic chaining to another data table occurs when the byte count is decreased to 0. The core storage word following the data table word containing the last byte must contain the address of the next data table. The first word of the next data table must contain its own address to prevent a channel address register (CAR) check. The second word of the next data table contains scan control bits, line adapter control bits, and the byte count for that data table.

Data chaining from transmit to receive tables or vice versa is allowed within certain restrictions. The rules for data chaining are given in Figure 97. Note that chaining of receive tables is permitted. However, the Multiprogramming Executive (MPX) Operating System does not allow chaining of receive data tables.

TABLE COMPLETE INTERRUPT: When this bit is off, a table complete interrupt is given when the byte count is decreased to 0. When this bit is on, table complete interrupt is suppressed.

Line Adapter Control

The line adapter control bits (2 and 3) further define the initialize operation as described next.

RECEIVE/TRANSMIT MODE: When this bit is off, the line adapter is placed in receive mode and begins monitoring the line for characters received. When this bit is on, the line adapter is placed in transmit mode. This mode causes the line adapter to transmit a synchronization sequence consisting of pre-SYN and SYN characters, followed by the first character from the data table.

SUPPRESS TIMEOUT INTERRUPT: When this bit is off, the timeout interrupt is not suppressed. When this bit is on, timeout interrupt is suppressed.

Byte Count

The byte count (bits 4 through 15) specifies the number of eight-bit characters (two per core storage word) in the data table. All characters in a data table must be counted. If the byte count is odd, the first character position (bits 0 through 7) following the byte count word is ignored by the line adapter and is not transmitted.

DIAGNOSTIC FUNCTIONS

A line adapter is placed in diagnostic mode by an XIO initialize write with modifier bit 8 on. In diagnostic

From Table	To Table	Chaining
Transmit with XITB	Transmit	Mandatory
Transmit w/o XITB	Transmit	Optional (1)
Transmit with XITB	Receive	Illegal
Transmit w/o XITB	Receive	Mandatory (2)
Receive	Receive	Optional (3)
Receive	Transmit	Illegal

1) If message transmission not completed.
2) If message transmission completed and response is expected.
3) Chaining two receive tables may present programming problem in determining the location of end character. See description of bits 3 and 4 of operating DSW.

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Figure 97. CA Data Chaining Rules

mode, operation of the line adapter is changed as follows:

1. In transmit mode, the send data line to the data set is looped back to the input of the SERDES.
2. All characters are read from or stored in bits 8 through 15 of the data table words.
3. After each character in transmit mode, and before each character in receive mode, the diagnostic device status word (DSW) is stored in the transmit and receive data tables, respectively. This storing is automatically accomplished by means of data channel (cycle steal) operations.

Figure 98 illustrates the format of diagnostic transmit and receive data tables. Note that space must be reserved in the tables for the diagnostic DSW's. When constructing diagnostic data tables, consideration must be given to characters that may be automatically inserted into the transmission stream by the line adapter. With external clocking, for example, a synchronous idle sequence (SYN SYN or DLE SYN) is automatically inserted if a synchronous idle sequence is not detected in the data stream within 1 second intervals. The added synchronous idle sequence would add two additional diagnostic DSW's to both data tables. In transparent mode, this insertion can be avoided by using shorter data tables (approximately 50 characters in length). In normal mode, SYN SYN sequences can be placed in the transmit data table at intervals of less than 1 second. Transparent mode transmission also leaves exposure to automatic insertion of a second DLE following any DLE in the transmit data table. This DLE insertion would cause one additional diagnostic DSW in both data tables.

The XIO sense device also provides a diagnostic function (program receive input) when a line adapter is in receive mode. Modifier bit 8 being on in the XIO sense device causes a space (0-bit) to enter the SERDES. A subsequent XIO sense device causes a mark (1-bit) to enter the SERDES. Thus the input to the SERDES can be program controlled with a series of XIO sense device appropriately timed.

When using program receive input, the data set cable must be in test position to avoid interference with input data on the transmission line.

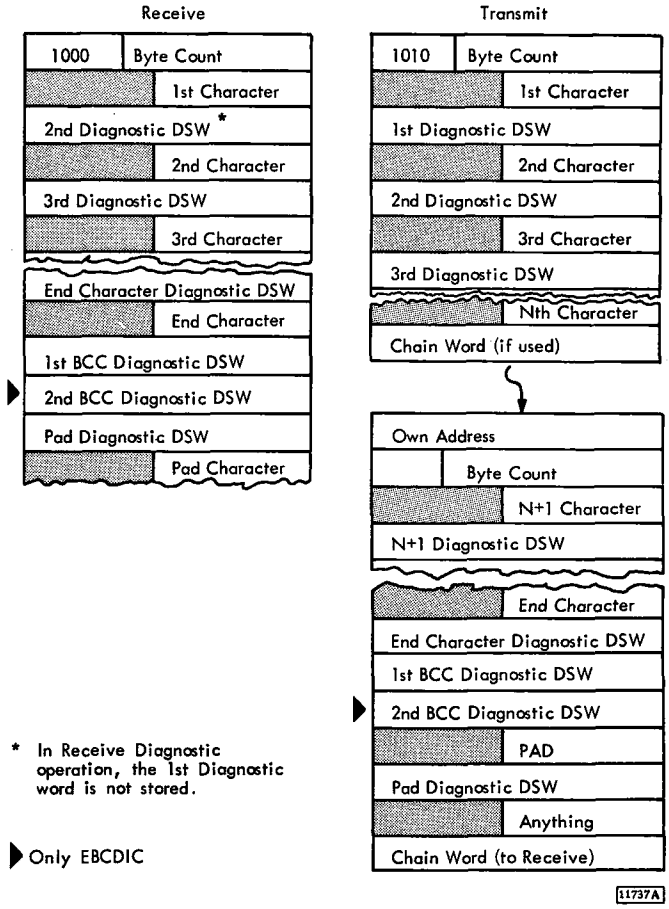


Figure 98. CA Diagnostic Data Tables

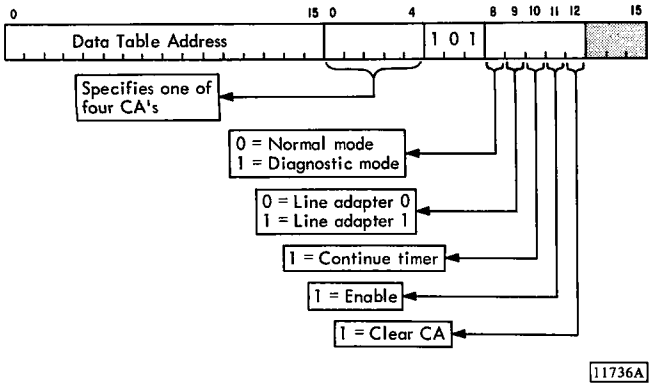
CA PROGRAMMING

Each line adapter on a CA operates under data channel control for data transfer. The two line adapters of a CA may share a single data channel if concurrent operation of both line adapters is not desired. However, if concurrent (overlap) operation is desired, the line adapters must be assigned to separate data channels.

The line adapters are individually controlled through use of the execute I/O (XIO) instruction. The input/output control command (IOCC) referenced by an XIO must have an area code of 10101, 10110, 10111, or 10100 to address CA's 1, 2, 3, or 4, respectively. The following IOCC's are used for operation and control of the line adapters.

CA IOCC's

Initialize Write



This command is used to initialize the line adapter specified by modifier bit 9. The IOCC address word specifies the core storage address of a data table. The first word of the data table contains the byte count, scan control bits, and line adapter control bits which further define the initialize operation. After the initialization sequence, data transfer between the line adapter and data table in core storage occurs by means of data channel operations at a character rate of 1/8 baud. (See "Line Adapter Initialization.")

In applications using "connect data set to line" philosophy (normally used for two-wire leased or switched lines), this command also turns on data terminal ready to the data set. Once on, data terminal ready is reset by an XIO sense device with modifier bit 11 (enable) off and modifier bit 12 (clear CA) on, or by a dc reset. In applications using "data terminal ready" philosophy, data terminal ready is controlled by modifier bit 11 (enable) of an XIO initialize write or XIO sense device.

Modifier bits of an XIO initialize write perform the functions described next.

DIAGNOSTIC MODE (Bit 8): This modifier specifies the mode of operation: 0 = normal mode, and 1 = diagnostic mode. (See "Diagnostic Functions.")

LINE ADAPTER (Bit 9): This modifier bit specifies the particular line adapter on the CA: 0 = line adapter 0, and 1 = line adapter 1.

CONTINUE TIMER (Bit 10): When on, this modifier bit changes the 3-second timeout period to 2 seconds and starts the timer. The new timeout period remains effective until: (1) a timeout interrupt occurs, (2) a change from receive to transmit mode, or vice versa, occurs, or (3) a clear CA function is given.

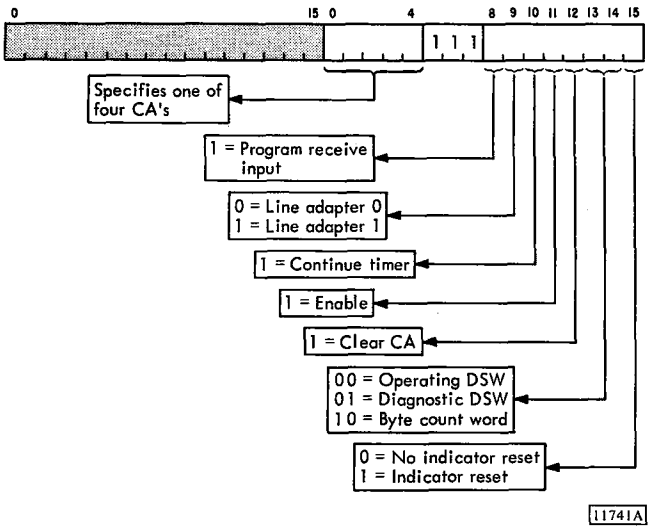
Continue timer may be specified when the program is not ready to transmit or receive the next message block. In the case of transmit, STX ENQ (TTD) should be sent after the timeout. In the case of receive, DLE, (WACK) should be sent.

ENABLE (Bit 11): This modifier bit performs the following two functions:

1. When on, the enable bit sets a latch that enables the line adapter to recognize a data set ringing condition and provide a ringing interrupt to the program. However, the line adapter can recognize a ringing condition only when it is not initialized (not in transmit or receive mode), even if the enable ringing interrupt latch is set. Because an XIO initialize write places the line adapter in transmit or receive mode, the enable ringing interrupt function is negated until the line adapter is deinitialized. Once the enable ringing interrupt latch is set, an XIO sense device with modifier bit 11 (enable) off and modifier bit 15 on is required to reset it.
2. Enable may also be used with the XIO initialize write to directly control data terminal ready in applications using "data terminal ready" philosophy. When enable is on, data terminal ready is turned on. Once data terminal ready is on, a clear CA function with modifier bit 11 (enable) off, or a dc reset, is required to turn it off.

CLEAR CA (Bit 12): When on, this modifier bit causes a reset of the line adapter to permit restart from a known condition. The device status word is also reset by this function. However, SERDES is not reset. A clear CA function should always be given before initializing a line adapter.

Sense Device



This command is used to load one of the three device status words (DSW's) of a line adapter into the accumulator.

IOCC modifier bits may also specify various other functions, described next.

PROGRAM RECEIVE INPUT (Bit 8): This modifier bit is used only during diagnostic mode and should be off for normal operation. (See "Diagnostic Functions.")

LINE ADAPTER (Bit 9): This modifier bit specifies the particular line adapter on the CA: 0 = line adapter 0, and 1 = line adapter 1.

CONTINUE TIMER (Bit 10): This modifier bit performs the same function with an XIO sense device as it does with an XIO initialize write.

ENABLE (Bit 11): This modifier bit performs the same functions with an XIO sense device as it does with an XIO initialize write.

CLEAR CA (Bit 12): This modifier bit performs the same function with an XIO sense device as it does with an XIO initialize write. In addition, data terminal ready is reset if a switched network is being used. The actual length of time that data terminal ready is allowed to be reset ("on hook") without causing the data set to remove clear-to-send depends on the type of data set used.

DSW SELECTION (Bits 13 and 14): These modifier bits select the DSW to be loaded into the accumulator as follows:

00 = Operating DSW.
01 = Diagnostic DSW.
10 = Byte count.

RESET (Bit 15): This modifier bit controls reset of program resettable indicators when sensing the operating DSW. If modifier bit 15 is on, program resettable indicators in the operating DSW are reset. If modifier bit 15 is off, program resettable indicators in the operating DSW are not reset.

Modifier bit 15 is used in conjunction with modifier bit 11 to reset the enable ringing interrupt latch. Modifier bit 15 must be on and modifier bit 11 must be off to reset the latch.

CA Operating DSW Interrupt Indicators

Figure 99 shows the operating DSW format and defines interrupt and program resettable indicators.

CHANNEL STOP: This indicator turns on, causing an interrupt, if a P-C parity error, storage protect violation, channel address register (CAR) check, or an out bus parity error is detected other than during data transfer. Channel stop being on inhibits further data channel operation.

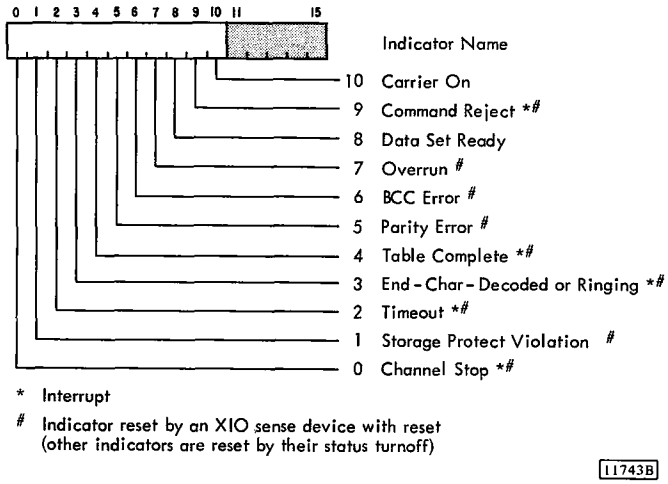


Figure 99. CA Operating Device Status Word

TIMEOUT: This indicator turns on, causing an interrupt, if any of the following conditions occurs:

1. SYN SYN sequence not detected for 3 seconds while line adapter is initialized.
2. Continuous SYN characters received for 3 seconds while line adapter is initialized.
3. DLE SYN sequence not detected for 3 seconds while line adapter is in transparent mode.
4. Continuous DLE SYN sequences detected for 3 seconds while line adapter is in transparent mode.
5. Data set does not respond to request-to-send with clear-to-send within 3 seconds.
6. Table is complete and no-chaining-specified condition exists in transmit mode, and a receive table has not been initiated.

If continue timer was specified in a previous command, the 3 second timeout in conditions 1 through 5 occurs in 2 seconds.

Timeout interrupt is suppressed if bit 3 of the data table byte count word is on.

END-CHARACTER-DECODED OR RINGING: This indicator turns on, causing an interrupt, if one of the following end characters is detected during receive mode:

ETB	EOT
ETX	NAK
ENQ	DLE turnaround

For EOT and NAK, at least four 1-bits of the following PAD character must be received for the character to be recognized as an end character. The actual interrupt is delayed until after the PAD character is stored.

EOT, NAK, and DLE turnaround do not cause interrupts if they appear after an SOH/STX in the received data stream.

When end-character-decoded or ringing is on, all data channel (cycle steal) operations for the line adapter are stopped. Therefore, the byte counter can be sensed before resetting the interrupt and then used to find the location of the end character. The following method may be used to locate the end character provided no receive data table chaining has occurred.

1. Complement the sensed byte count. (For example, complement of 0111 is 1000.)
2. Subtract the complemented byte count from the original byte count.
3. If the original byte count is odd, add 1 to the difference obtained in step 2.
4. Divide the result by 2.
5. Add the quotient to the address of the byte count word for the table. The resultant address is the core storage location containing the end character. If the divide in step 4 produced a remainder, the end character is in bits 8 through 15 of the core storage word; otherwise it is in bits 0 through 7.

End-character-decoded or ringing indicator is also turned on by a data set ringing condition provided ringing has been enabled and the line adapter is not initialized (in transmit or receive mode). If the line adapter is initialized, data set ringing condition does not set this indicator.

Since both an end-character-decoded or data set ringing condition can set this indicator, the program must retain the initialization state of the line adapter to distinguish between the two conditions.

If this indicator is turned on by a ringing condition, the line adapter must be initialized, or ringing must be disabled, before an XIO sense device with reset can reset the indicator. (This reset prevents the ringing condition from causing another interrupt.)

TABLE COMPLETE: Unless suppressed by bit 1 of the byte count word being on, this indicator turns on, causing an interrupt, when the byte count is decreased to 0. A byte count of 0 denotes the end of the data table.

In receive mode, table complete occurs simultaneously with end-character-decoded if the receive data table ends with the PAD character following the end character.

COMMAND REJECT: This indicator turns on, causing an interrupt, if an XIO initialize write that does not specify clear CA (bit 12) is given under either of two conditions: (1) the selected line adapter is in transmit mode, or (2) this line adapter has received SYN SYN and has not received a character requiring line turnaround. The command rejected is ignored.

CA Operating DSW Noninterrupt Indicators

Figure 99 shows the operating DSW format and defines noninterrupt and program resettable indicators.

STORAGE PROTECT VIOLATION: This indicator turns on if the line adapter attempts to store data in

a storage-protected location. This indicator turning on causes channel stop to turn on, thereby causing an interrupt.

PARITY ERROR: This indicator turns on if a parity error is detected during data transfer between the line adapter and core storage, or if a VRC error is detected while the line adapter is transmitting or receiving in ASCII.

If a parity error is detected during data transfer to core storage, the word is stored with bad parity. If a VRC error is detected while receiving ASCII, the parity of the byte containing the character is corrected when the byte is transferred to core storage. However, the parity of the ASCII character contained in the byte is not corrected.

Detection of a VRC error while transmitting ASCII does not stop transmission, but causes a data parity error to turn on and an invalid block check character (BCC) to be transmitted. Therefore, data parity error and data BCC error will both be on in the receiving line adapter.

BCC ERROR: This indicator turns on if the block check character (BCC) accumulated while receiving data does not match the BCC received from the transmitting station. In EBCDIC, the BCC consists of two CRC characters (eight bits each). In ASCII, the BCC is one 8-bit LRC character.

OVERRUN: This indicator turns on if the data channel fails to transfer data during the time the line adapter requires service.

If overrun occurs during transmission, message transmission does not stop, but subsequent data has missing bits and is not correct. An invalid block check character (BCC) is transmitted at the end of the message block. This invalid BCC causes a data BCC error to be indicated at the receiving station.

DATA SET READY: This indicator is on whenever data set ready from the data set is on.

CARRIER ON: When two-wire switched networks are being used, this indicator is on whenever the data set is indicating that a carrier is being detected on the line. When four-wire networks are being used, this indicator is always on.

Byte Count DSW

The byte count DSW is shown in Figure 100.

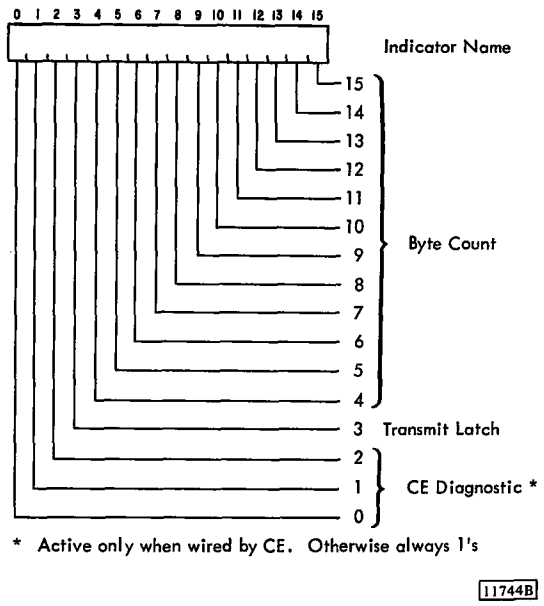


Figure 100. CA Byte Count Device Status Word

CE DIAGNOSTIC BITS: These bits are provided for diagnostic purposes and are meaningful only when wired by a customer engineer (CE). Otherwise these bits are always on.

TRANSMIT LATCH: This indicator reflects the status of the transmit latch and is on when the line adapter is in transmit mode.

BYTE COUNT: These bits reflect the status of the byte count at the time it was sensed. The byte count is in 1's complement form.

Diagnostic DSW

The diagnostic DSW is shown in Figure 101.

CE DIAGNOSTIC BIT: This bit is provided for diagnostic purposes and is meaningful only when wired by a customer engineer (CE). Otherwise this bit is always on.

CHARACTER PHASE: In transmit mode, this indicator is off from the time of initialization to the time the pre-SYN and SYN SYN sequences used for bit and character synchronization are transmitted. In receive mode, this bit is off from the time of

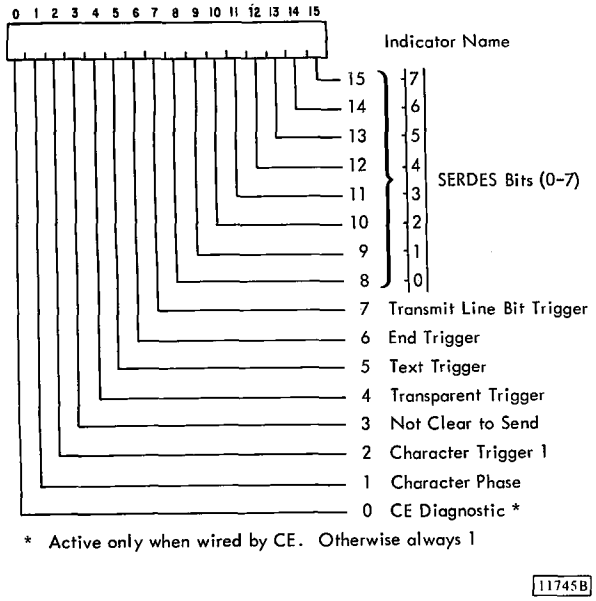


Figure 101. CA Diagnostic Device Status Word

initialization to the time a SYN SYN sequence is detected, indicating character phase.

CHARACTER TRIGGER 1: This indicator reflects the status of the first bit in the character counter. This counter is held reset except when the adapter is transmitting or receiving the following:

1. The initial pre-SYN and SYN SYN sequence.
2. SYN characters in the data stream.
3. Characters following an end character.

Under these conditions, the indicator alternately turns on and off at each character time.

NOT CLEAR TO SEND: This indicator is on when the data set is not in transmitting state.

TRANSPARENT TRIGGER: This indicator is turned on by a DLE STX sequence. It is turned off by a DLE followed by an ETB, ITB, ETX, or ENQ.

A clear CA function also resets this trigger.

TEXT TRIGGER: This indicator is turned on by the first character after SOH or STX in a message. It is reset when the mode is changed from transmit to receive mode or vice versa.

A clear CA function also resets this trigger.

END TRIGGER: This indicator turns on if any one of the following characters is recognized: ETB, ETX, ITB, or ENQ. It also turns on if NAK, EOT, or DLE turnaround is recognized and not preceded by an SOH or STX in the data stream.

In transparent mode, only ETB, ETX, ITB, and ENQ are recognized, and each must be preceded by a single DLE.

This indicator is reset at end-character-decode time or by a clear CA function.

TRANSMIT LINE BIT TRIGGER: This indicator reflects the status of the transmit line bit trigger and is on whenever a 1-bit (mark) is being transmitted on the line.

SERDES: These eight indicators reflect the status of SERDES bit positions 0 through 7. The contents of SERDES are shifted from bit position 0 to bit position 7. Therefore, SERDES output to the line is via bit position 7, and SERDES input from the line is via bit position 0.

In two-wire systems, transmitted data returns to the SERDES input after a certain delay; normally the delay equals the transmit time through the data set. However, if the switch on the data set cable is set to TEST, the delay equals one bit time.

DATA SET CONTROL LINE OPTIONS

Various options are provided for controlling the data terminal ready and request-to-send control lines to the data set. These options allow the customer to design a method of data set control that is suitable for the types of data sets and transmission lines used as well as for the particular application.

The method used to control data set ready and request-to-send are selected and assigned, during system installation, according to the options selected by the customer.

Data Terminal Ready

Three methods for controlling the data terminal ready line are available. These methods are described in the following paragraphs.

The first method of control is to provide a continuous data terminal ready signal to the data set. In this case, data terminal ready is on continuously and is not controlled by the program or conditions occuring during operation. This method of control may be used in (1) four-wire operations, (2) two-wire leased line operations, or (3) two-wire switched line operations that do not use the ringing interrupt feature.

The second method of control is to provide a data terminal ready signal to the data set when the line adapter is first initialized by the program for a

transmit or receive operation. In this case, data terminal ready is turned on by an XIO initialize write to initialize the line adapter. Once on, data terminal ready remains on until reset by an XIO sense device with modifier bit 11 (enable) off and modifier bit 12 (clear CA) on, or by a dc reset. If a clear CA operation is desired without resetting data terminal ready, modifier bit 11 (enable) should be on in the XIO sense device. This second method of control may be used in (1) two-wire switched line operations, (2) applications using "connect data set to line" philosophy, and (3) applications that use the ringing interrupt and subsequent auto-answer features.

The third method of control is to provide the program with the ability to turn data terminal ready on or off independent of other operations. In this case, data terminal ready is turned on by modifier bit 11 (enable) being on in an XIO initialize write or XIO sense device. Once on, data terminal ready remains on until reset by modifier bit 11 (enable) being off and modifier bit 12 (clear CA) being on in an XIO initialize write or XIO sense device. A clear CA operation may be performed without resetting data terminal ready by turning on modifier bits 11 and 12 in the XIO initialize write or XIO sense device. The third method of control is normally used in applications using "data terminal ready" philosophy.

Request to Send

Three methods for controlling the request-to-send line are available. These methods are described in the following paragraphs.

The first method of control is to provide a request-to-send signal to the data set when the line adapter is first initialized by the program for a transmit or receive operation. In this case, request to send is turned on by an XIO initialize write to initialize the line adapter. Once on, request to send remains on until reset by an XIO sense device with modifier bit 11 (enable) off and modifier bit 12 (clear CA) on, or by a dc reset. If a clear CA operation is desired without resetting request to send, modifier bit 11 (enable) should be on in the XIO sense device. This method of control may be used in applications using continuous carrier operation.

The second method of control is to provide a request-to-send signal to the data set only when the line adapter is in an initialized state (in transmit or receive mode). In this case, request to send is on when the line adapter is in either transmit or receive mode and is off when the line adapter is not in transmit or receive mode. The second method of control is normally used in applications using "data terminal ready" philosophy.

The third method of control is to provide a request-to-send signal to the data set only when the line adapter is actually transmitting to the line. In this case, request to send is on when the line adapter is actually transmitting data to the line and is off when the line adapter is not transmitting data to the line. The third method of control is normally used in applications, such as two-wire switched lines, where the carrier is desired only when actually transmitting data to the line.

IMPLEMENTATION OF BSC

Transmit Mode

During transmit mode, data is transferred from core storage to a remote station via a line adapter and communication facilities. Transmission proceeds until stopped by one of the following events: (1) a chain to a receive data table occurs, (2) the line adapter is reinitialized to receive mode, or (3) a clear CA function is given.

The following paragraphs describe implementation of the BSC control characters in transmit mode.

SYN: SYN characters are generated automatically. They are used to establish and maintain character phase as follows:

1. A SYN SYN sequence is transmitted prior to the first character in the transmit data table to establish character phase (synchronism).
2. In normal mode, a SYN SYN sequence is automatically inserted in the data stream every second to maintain synchronism.
3. In transparent mode, a DLE SYN sequence is automatically inserted in the data stream (at a rate determined by the line speed) to maintain synchronism.

SYN characters can be inserted by the program as time fills for up to 2.5 seconds in normal mode. DLE SYN sequences cannot be used for time fills in transparent mode.

SOH AND STX: These two characters are used to indicate start of heading or text and to initiate accumulation of the CRC or LRC character for the message block.

The initial SOH, STX, or DLE STX in a transmit data table should be so placed that the end character causing line turnaround appears in bits 8 through 15 of the core storage word.

When an odd byte count is used, the first character transmitted is in bits 8 through 15 of the first data word. The character in bits 0 through 7 is not transmitted.

ETB, ETX, AND ENQ: These characters are used as end characters that cause line turnaround. After an ETB or ETX is transmitted, the line adapter automatically sends the accumulated BCC's, which are then followed by the PAD character from the data table. For an ENQ ending, the BCC's are not transmitted. The PAD character follows the ENQ character.

ITB: ITB is used as an end character that does not cause line turnaround. After an ITB is transmitted, the line adapter automatically sends the accumulated BCC's, which are then followed by the next message block in the transmit data table.

An ITB is not restricted to a specific location within a transmit data table in normal mode. In transparent mode, a DLE ITB sequence must appear in the next-to-last word of the transmit data table to be interpreted as DLE ITB. In this case, data chaining is required.

DLE: DLE is used to provide additional line control characters. A DLE STX sequence places the line adapter in transparent mode.

While in transparent mode, the line adapter inserts a DLE into the data stream whenever a DLE is received from core storage (except when the byte count is 3 or less). This enables the receiving station to differentiate between data DLE sequences and control DLE sequences.

The DLE SYN sequence is used to maintain synchronism in transparent mode. It is automatically generated by the line adapter.

DLE followed by ETX, ETB, ITB, or ENQ in the next-to-last word of a transmit data table causes the line adapter to leave transparent mode and proceed with normal transmission ending.

PAD: To ensure that the last bit of the last character is properly transmitted, a PAD character must follow each turnaround character (ETB, ETX, EOT, ENQ, NAK, or DLE turnaround). With ETB and ETX, the PAD character is actually transmitted following the BCC's. In any case, the PAD character follows the character in the transmit data table.

Receive Mode

During receive mode, the line adapter monitors the communications line for data and responds accordingly when control characters are received. The line adapter remains in receive mode until: (1) a chain to a transmit data table occurs, (2) the line adapter is reinitialized to receive mode, or (3) a clear CA function is given. The following paragraphs describe implementation of BSC control characters in receive mode.

SYN: After being set to receive mode, the line adapter establishes character phase with the transmitting station when it detects a SYN SYN sequence. If character phase is not established within 3 seconds, a timeout interrupt is set.

In normal mode, all SYN characters are stripped from the received data and are not sent to core storage.

SOH AND STX: These two characters indicate start of heading or text and initiate accumulation of the CRC or LRC character for the message block.

ETB AND ETX: These two characters indicate to the line adapter that BCC's are to follow immediately. The BCC's received are compared for agreement with the accumulated BCC's in the receiver. If the BCC's agree, no transmission error occurred. If the BCC's disagree, the BCC error indicator is set in the device status word (DSW).

The line adapter remains in receive mode when ETB or ETX is received. However, data channel operations are stopped. An end-character-decoded interrupt is set after the BCC's are compared and the PAD character is stored. This interrupt allows the program to sense the byte count to locate the end of the message block and initiate the line turnaround function.

ITB: ITB indicates to the line adapter that BCC's are to follow immediately. The BCC's received are compared for agreement with the accumulated BCC's in the receiver. If the BCC's agree, no transmission error occurred. If the BCC's do not agree, the BCC error indicator is set in the DSW.

The line adapter remains in receive mode, data channel operations are not stopped, and no end-character-decoded interrupt is given.

ENQ, NAK, EOT, AND DLE TURNAROUND: These characters are all decoded by the line adapter and cause an end-character-decoded interrupt after the PAD character is stored in core storage. NAK, EOT, and DLE turnaround do not cause an interrupt if they appear in the data stream after an SOH or STX.

ENQ and NAK do not cause an interrupt unless four 1-bits (low-order portion of following PAD) are detected by the line adapter immediately following the ENQ or NAK.

DLE: A DLE STX sequence causes the line adapter to enter transparent mode. In transparent mode, a

DLE DLE sequence is interpreted as a data character. The first DLE is stripped from the received data and is not transferred to core storage. A DLE SYN sequence is detected as a synchronous idle character in transparent mode and is not transferred to core storage.

A DLE followed by an ETB, ETX, ITB, or ENQ causes the line adapter to leave transparent mode and proceed with normal transmission ending.

If DLE ITB is used in transparent mode, the following message block must start with DLE STX to place the line adapter back in transparent mode.

TRANSMIT AND RECEIVE EXAMPLES

Normal Mode

Figure 102 illustrates an example of transmission between two stations in normal mode. Either EBCDIC or ASCII can be used in normal mode.

Transparent Mode

Figure 103 illustrates an example of transmission between two stations in transparent mode. Only EBCDIC may be used in transparent mode.

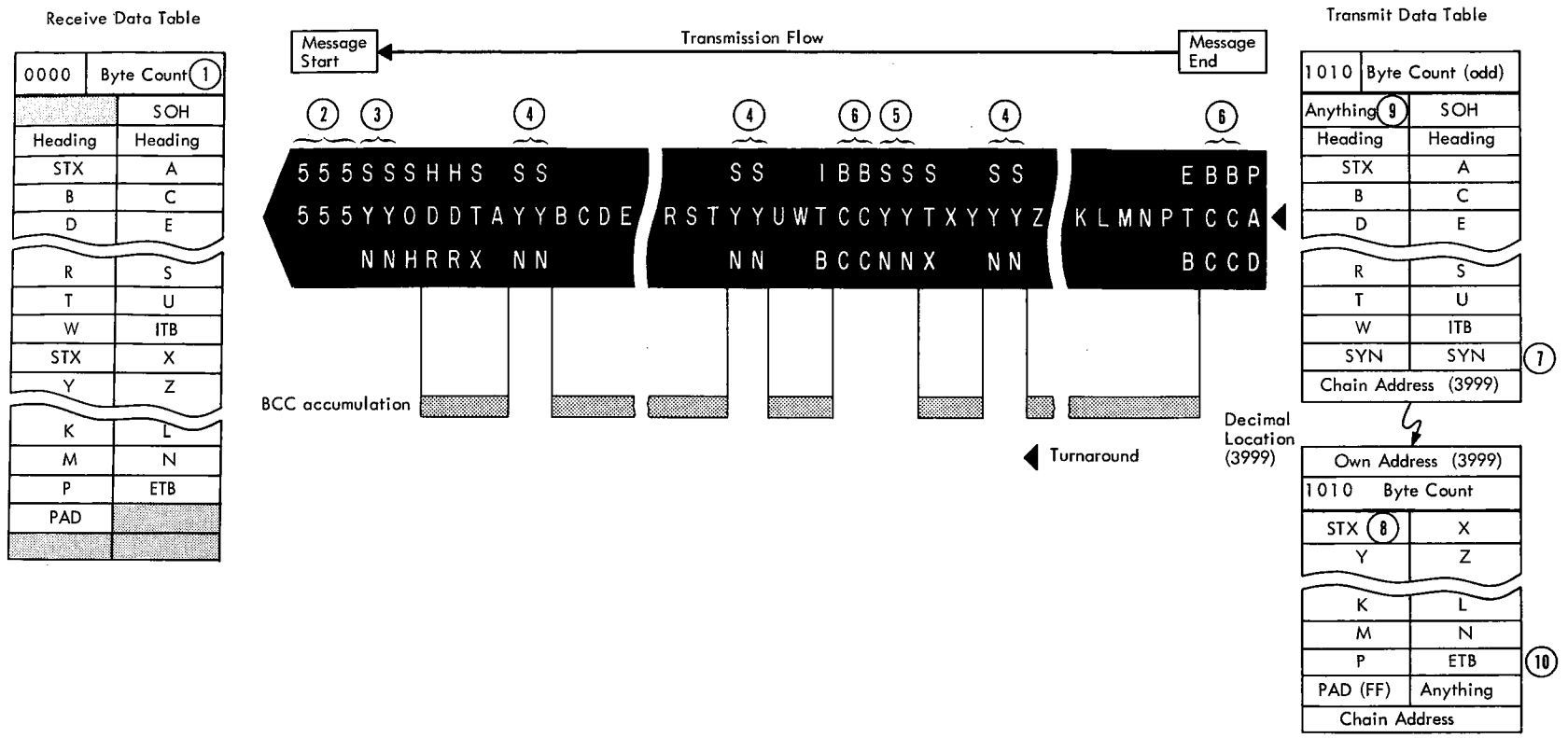


Figure 102. Transmit/Receive Sequence – Normal Mode

Notes:

(1) Byte count must be long enough to accommodate longest transmitted message. Chaining can also be used.

(2) Pre-SYN PAD characters automatically generated by transmit station and stripped at receive station. Three pre-SYN pads are required for business machine clocking, one for data set clocking.

(3) Initial double SYN sequence automatically generated by transmit station and is used to establish character phase between stations.

(4) Synchronous idle characters automatically inserted and stripped by transmit and receive stations. Used to maintain synchronization.

(5) Double SYN characters from transmit data table treated as a synchronous idle sequence.

(6) BCC's automatically inserted in message stream. Only one BCC is used in ASCII code.

(7) SYN characters optional.

(8) STX after ITB optional.

(9) Because of odd byte count, table starts at low order half of the core location word. High order bits can be anything.

(10) END characters must appear at this table location to terminate.

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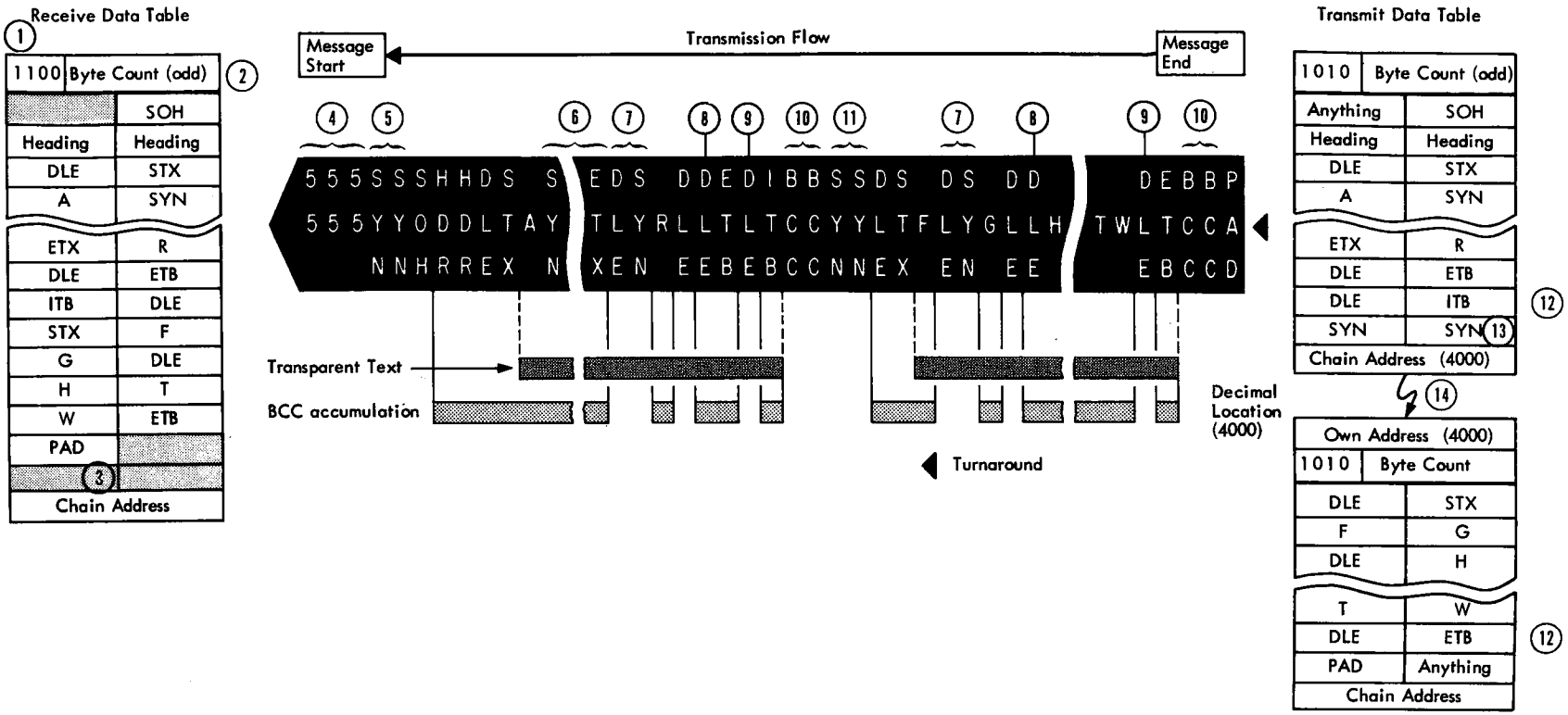

Figure 103. Transmit/Receive Sequence – Transparent Mode

Notes:

1. Suppress table complete optional.
2. Byte count must be long enough to accommodate longest transmitted message. Chaining can be used.
3. Data channel operations stop. Byte counter, which can be sensed, is used to find the END character.
4. Pre-SYN PAD characters automatically generated by transmit station and stripped at receive station.
5. Double SYN sequence automatically generated by transmit station and used to establish character phase.
6. In transparency, and EBCDIC bit code can be transmitted. CA does not respond to control characters unless they are prefixed with DLE and they appear at proper transmit table location.
7. Synchronous idle characters automatically inserted and stripped by transmit and receive stations. Used to maintain synchronization.
8. In transparency, when DLE appears in table, adapter inserts a second DLE (except when byte count is 3 or less). At receive end this DLE is stripped.
9. The DLE of the ending sequence is stripped at the receive station.
10. BCC's automatically inserted in message stream.
11. Double SYN characters from transmit data table treated as synchronous idle.
12. End characters must be placed at these table locations since byte count is checked to determine when an end character appears.
13. SYN characters are required when ITB is located in right half of word.
14. Chaining is required when ITB and transparent mode is used.

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Selector Channel

The selector channel provides the facilities for attaching an IBM 2841 Storage Control with as many as eight IBM 2311 Disk Storage Drives to the 1800 system. An 1826 Data Adapter Unit, Model 2 or Model 3, provides housing for the selector channel.

Mode of Operation

The selector channel operates in burst mode only and uses the cycle-stealing facilities of a data channel. The maximum instantaneous data rate that can be handled by the selector channel is 330,000 eight-bit bytes per second. This figure is based on two assumptions: (1) the attached control unit does not have a buffer, and (2) the selector channel is assigned to the highest priority data channel. The actual data rate of any one configuration depends on the control unit, I/O device, and mode of operation. For example, the 2841/2311 combination has an approximate data rate of 156,000 bytes per second.

Programming Compatibility

The selector channel is controlled by the 1800 execute I/O (XIO) instruction. The control concepts of the selector channel are the same as for the System/360 channel; that is, a channel command word (CCW), channel status word (CSW), start I/O, and halt I/O are used. However, the formats of these words and commands differ from those used with System/360 programming. Therefore, 1800 programming and System/360 programming for the same devices are not compatible.

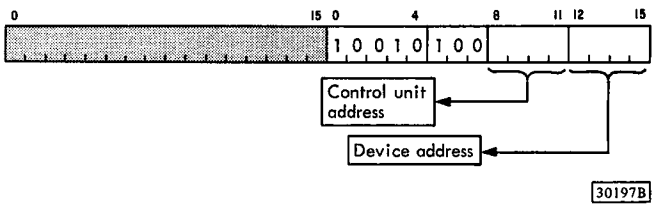
This section of this manual describes programming and operating characteristics of the selector channel. The disk storage concepts, programming, and actual CCW command codes used for 2841/2311 operations are described in the SRL publication IBM System/360 Component Description -- 2841 and associated DASD, Order No. GA26-5988. Although the CCW's described in that publication are in System/360 format, the functions of the various fields described are the same as those of the corresponding fields in the 1800 CCW format. For example, the flag and command code fields in both CCW formats provide the same functions.

SELECTOR CHANNEL PROGRAMMING

The selector channel utilizes a data channel to communicate with the processor-controller (P-C). Data and commands are both transferred between the selector channel and P-C by means of data channel operations. The execute I/O (XIO) instruction is used to control selector channel operations. An input/output control command (IOCC) referenced by an XIO must have an area code of 10010 to address the selector channel. The following IOCC's are used to control selector channel operations.

Selector Channel IOCC's

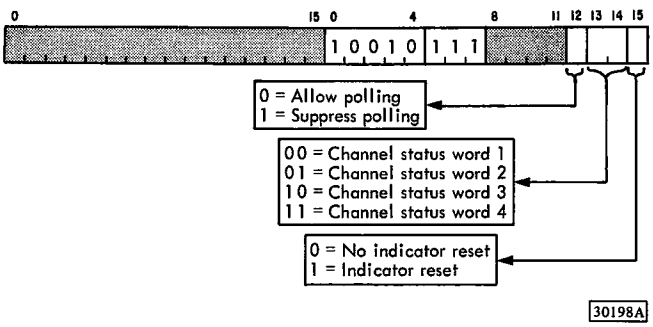
Control (Halt I/O)



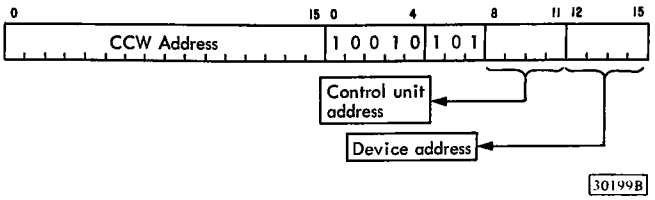
This command is used as a halt I/O and causes termination of the current I/O operation at the selector channel. If the channel is not busy, the device specified by the modifier bits is selected and signaled to terminate the current operation without further data transfer. If the channel is busy, the operation is terminated and the device currently using the channel is immediately disconnected. In this case, the modifier bits are ignored. A unit status pending interrupt caused by channel end/device end occurs after the channel and/or device is cleared.

If a program check occurs, an XIO control (halt I/O) should be given to reset the selector channel

Sense Device



Initialize Write (Start I/O)



This command causes one of the four words comprising the selector channel status word (CSW) to be read into the accumulator. Modifier bits 13 and 14 specify the word to be read, and modifier bit 15 controls reset of the program resettable indicators in the CSW. If modifier bit 15 is on, the reset function is performed. If modifier bit 15 is off, the reset function is not performed. (The individual words of the CSW, interrupt indicators, and program resettable indicators are described under "Channel Status Word.")

Modifier bit 12 of an XIO sense device controls the channel polling function. Polling is the ability of the selector channel to acknowledge a request for service from a control unit. If modifier bit 12 is on, polling is suppressed. If modifier bit 12 is off, polling is allowed.

Aside from XIO sense device with modifier bit 12 on, polling also is suppressed by: (1) initiation of a start I/O operation (XIO initialize write), or (2) the selector channel accepting a request for service from a control unit.

Regardless of the cause of the suppression, polling remains suppressed until: (1) an XIO sense device with modifier bit 12 off is given, (2) a halt I/O (XIO control) is given, or (3) RESET on the P-C console is pressed.

A request for service from a control unit is usually the result of device end or attention turning on in the unit status portion of the CSW. If polling is not suppressed and a control unit requests service, the unit address-status portion of the CSW is transferred from the control unit to the selector channel, and a unit status pending interrupt is given to the P-C. The selector channel suppresses further polling until the program reads the status word and reinitiates polling.

Polling should be suppressed when any operation is in progress in the channel or control unit. Polling should always be enabled after the last interrupt has been serviced, unless another operation is being started. In that case, polling must be suppressed. This allows the selector channel to acknowledge a request from the control unit, such as attention or a device becoming ready.

Polling must also be enabled after receiving a busy in response to a start I/O. This allows the selector channel to acknowledge the request (from the control unit) that indicates when the device or control unit is no longer busy.

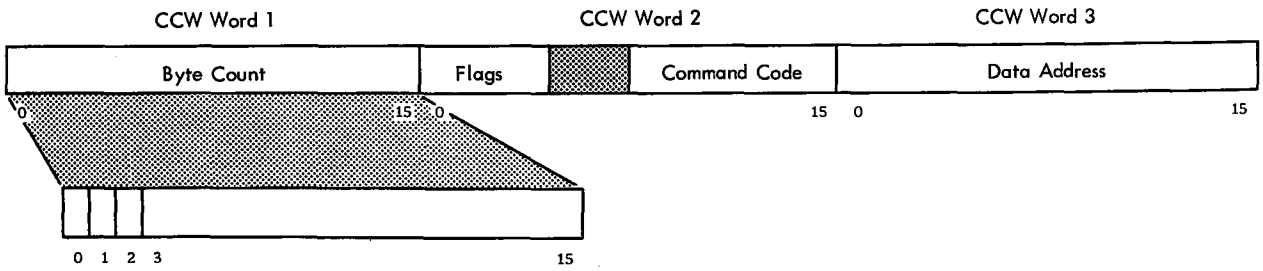
To prevent losing the interrupts that occur at the end of busy, a delay of approximately 30 μs should be provided between the XIO sense that suppresses poll and the XIO sense that checks for an interrupting condition before a start I/O. The selector channel may have started to acknowledge a request from a control unit at the time polling was suppressed. If a start I/O is performed before sensing for this interrupting condition, the unit status, device, and control unit address will be lost.

Polling should be reinitiated following completion of a start I/O operation by issuing an XIO sense device with modifier bit 12 equal to 0.

This command is used as a start I/O to initiate all selector channel I/O operations. The address field contains the core storage address of a channel command word (CCW). The CCW specifies the operation to be performed by the channel, control unit, and device as well as the core storage area associated with the operation. IOCC modifier bits 8 through 11 select the control unit, and modifier bits 12 through 15 select the device to which the operation pertains.

Once the IOCC area code, function, and modifiers have been sent to the selector channel and the CCW address has been loaded into the data channel address register (CAR), the P-C is released. The selector channel continues the operation by means of data channel (cycle steal) operations by fetching the addressed CCW from core storage.

If an XIO initialize write (start I/O) is given while the selector channel is busy, it is ignored and no indication is given to the program.



Bit	Indication
0	Used only with 32,768 word core storage and above
1	Used only with 16,384 word core storage and above
2	Used only with 8,192 word core storage and above
3-15	Used with bits 0-3 (if applicable) and specifies the number of 8-bit bytes in the input or output data field

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Figure 104. Byte Count (CCW Word 1)

Channel Command Word

The channel command word (CCW) contains the information that directs selector channel I/O operations. The CCW consists of three 16-bit words and may be located in any three contiguous core storage locations. The information in a CCW is separated into four fields:

Byte count.
Flag.
Command code.
Data address.

Byte Count

The byte count is located in word 1 of the CCW (Figure 104) and specifies the length (in eight-bit bytes) of the input or output field. The maximum length which may be specified is 65,535 bytes. Two 8-bit bytes are contained in each core storage word. Therefore, data transfer between the selector channel and core storage is performed two bytes (one core storage word) at a time. If an odd byte count is specified for a write operation, the byte in bit positions 8 through 15 of the last core storage word is not used even though it is transferred to the channel. If an odd byte count is specified for a read or sense operation, the byte in bit positions 8 through 15 of the last core storage word is not used for data, but is reset to 0.

All CCW's, except those specifying transfer-in-channel, but including those specifying immediate commands, must have a non-0 byte count. Although data is not transferred during an immediate command and the CCW specifies a non-0 byte count, incorrect length is not indicated in the CSW.

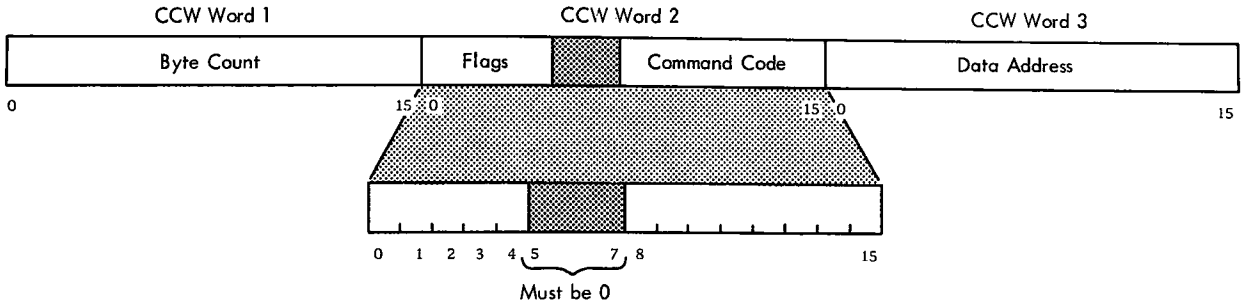
Flag

The flag field consists of bit positions 0 through 4 in word 2 of the CCW (Figure 105). The bits in the flag field further define the operation as follows:

CHAIN DATA (CD): When on, this flag specifies chaining of data. Data chaining causes the selector channel to automatically fetch the next sequential CCW when the byte count of the present CCW is decreased to zero. The new CCW is fetched from the three contiguous core storage locations beginning with the next higher location following the last CCW. The command code in the new CCW is ignored unless it specifies transfer-in-channel. However, the byte count, flags, and data address are used to continue the operation specified by the first CCW. Data chaining continues until a CCW with the CD flag off is encountered and the byte count of that CCW reaches 0, or until the device terminates the operation by presenting ending status.

Note that data chaining (CD flag is on) suppresses command chaining.

CHAIN COMMAND (CC): When on, this flag specifies chaining of commands. Command chaining causes the selector channel to automatically fetch the next sequential CCW at the completion of the current CCW operation (signaled by device end). The new CCW is fetched from three contiguous core storage locations beginning with the next higher location following the last CCW. All fields in the new CCW are used to initiate a new I/O operation. Command chaining continues until a CCW with the CC flag off is encountered and the operation specified by that CCW is completed.



Bit	Indication
0	CD - Specifies data chaining
1	CC - Specifies command chaining
2	SLI - Suppress length indication
3	PCI - Program control interrupt
4	Skip
5-7	Not used
8-15	Command Codes
0 0 0 0 0 0 0 0	Test I/O
M M M M M M 1 0	Read
M M M M M M 0 1	Write
M M M M M M 1 1	Control
M M M M 0 1 0 0	Sense
X X X X 1 0 0 0	Transfer in Channel

M = Modifier
X = Bit ignored

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Figure 105. Flags and Command Code (CCW Word 2)

It should be noted that data chaining takes precedence over command chaining; that is, if the CD and CC flags are both on, data chaining is performed and command chaining is suppressed.

SUPPRESS LENGTH INDICATION (SLI): This flag is used to determine whether occurrence of an incorrect length condition is to be indicated to the program. An incorrect length condition occurs if the number of bytes designated by the byte count in a CCW is not equal to the number of bytes requested or offered by an I/O device.

Indication of an incorrect length condition is suppressed if the SLI flag is on and the CD flag is off in the CCW. If the SLI flag and CC flag are both on in a CCW, the incorrect length indication is suppressed and command chaining takes place regardless of an incorrect length condition. Incorrect length indication is also suppressed if a CCW specifies an immediate command, even though the byte count must be non-0.

Indication of an incorrect length condition is always given to the program if the SLI flag is off, or if the CD flag is on in the CCW. In the latter case, indication of an incorrect length condition is given even if the SLI flag is on.

PROGRAM CONTROL INTERRUPTION (PCI): When on, this flag causes the selector channel to generate an interrupt upon fetching the CCW. This capability allows the program to detect when specific chained commands are about to be performed.

SKIP: When on, this flag suppresses data transfer to core storage during a read or sense operation. When the skip flag is off, normal read transfer occurs.

Command Code

The command code field consists of bit positions 8 through 15 in word 2 of the CCW (Figure 105). The two low-order bits (14 and 15) of the command code identify the operation to the selector channel. If these two bits are off, the operation is identified by the four low-order bits (12 through 15).

The selector can perform four basic operations:

Output forward (write or control).
Input forward (read or sense).
Branch (transfer-in-channel).
Test I/O.

All eight bits of the command code are transferred to the control unit. The high-order bits are modifiers that indicate to the device how the command is to be executed. The exact configuration of the modifier bits depends on the I/O device. Command codes and descriptions for the 2841/2311 are given in IBM System/360 Components Description -- 2841 and Associated DASD, Order No. GA26-5988. The basic commands for the selector channel are described under "Selector Channel Commands."

Data Address

The data address is located in word 3 of the CCW (Figure 106). For commands that transfer data (read, sense, write, and so on), the data address specifies the core storage address of the first two data bytes (two bytes per core storage word) in the input/output data field. For a transfer-in-channel command, the data address specifies the core storage address of the new (transferred to) CCW.

Selector Channel Commands

Figure 107 shows the bit configurations of the basic selector channel commands.

Test I/O

This command causes the addressed device to send its current status to the selector channel. After the channel has received the unit status, a unit status pending interrupt is given to the P-C.

A test I/O terminates command chaining even if the CC flag is on. Therefore, it should not be included within a chain of CCW's that specify command chaining.

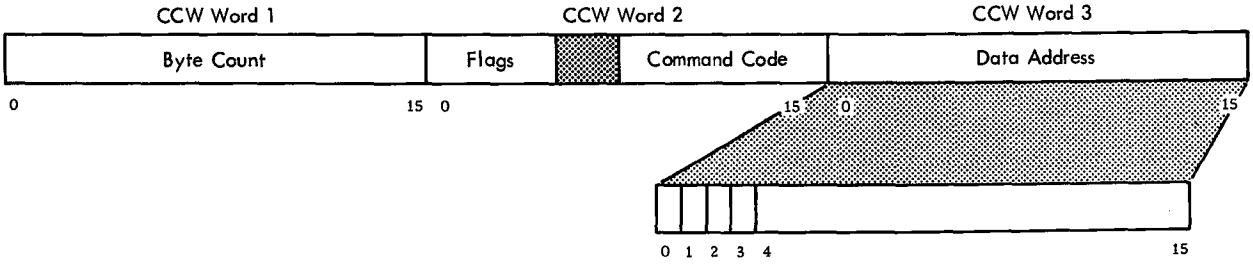
A test I/O need not be given prior to initiating a start I/O with a specific device. The selector channel automatically checks the unit status when initiating a start I/O operation. If the status is not acceptable, it is presented to the program by means of an interrupt.

Note that a test I/O does not place the unit status into the accumulator, but makes it available in the selector channel. An XIO sense device that specifies word 2 of the channel status word must be given to read the unit address-status into the accumulator.

Read

This command causes data to be transferred from the device specified in the XIO initialize write (start I/O) modifier bits to core storage. Data is read (two bytes per word) into ascending core storage locations beginning with the address specified in the CCW data address field. The number of bytes transferred during the operation is specified by the byte count in the CCW.

The read operation continues until the specified number of bytes are transferred, or until the I/O device terminates the operation. If the byte count is odd, the last byte transferred is placed in bit



Bit	Indication
0	Used only with 65,536 word core storage
1	Used with 24,576 word core storage and above
2	Used with 16,384 word core storage and above
3	Used with 8,192 word core storage and above
4-15	Used with bits 0-3 (if applicable) and specify the address of the first byte of data in an input or output data field (for transfer-in-channel commands, contains the address of a new CCW)

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Figure 106. Data Address (CCW Word 3)

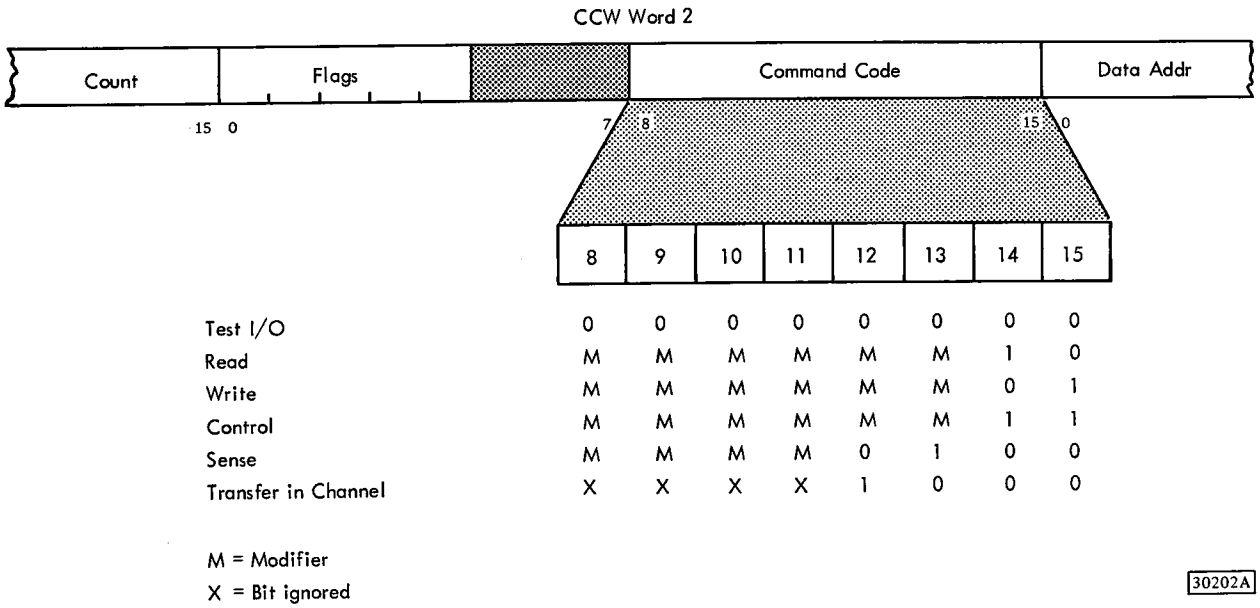

Figure 107. Command Code Assignment

positions 0 through 7 of the last core storage word. Bit positions 8 through 15 in this word are all reset to 0's.

Write

This command causes data to be transferred from core storage to the device specified in the XIO initialize write (start I/O) modifier bits. Data is transferred (two bytes per word) from ascending core storage locations beginning with the address specified in the CCW data address field. The number of bytes transferred during the operation is specified by the CCW byte count field.

The write operation continues until the specified number of bytes are transferred, or until the I/O device terminates the operation. If the byte count is odd, the last byte transferred is obtained from bit positions 0 through 7 of the last core storage word. Bit positions 8 through 15 in this word are ignored.

If an incorrect length condition occurs during a write operation, the incorrect length indication is given to the program with the ending status unless the suppress length indication (SLI) flag is on in the CCW.

Control

This command causes the device specified by the XIO initialize write modifier bits to initiate a control operation. The operation proceeds similar to a write, except that the command code modifier bits received by the control unit are decoded to determine the specific control function to be performed.

In cases where the particular control function can be performed without any data transfer (immediate command), the control unit signals channel end as soon as it receives the command. The device signals device end after it has completed the control function.

A control command in which all six of the modifier bits in the command code are off performs as a no-op (no operation). A no-op causes the control unit to respond with channel end and the device to respond with device end without causing any action. This ending status causes a unit status pending interrupt to be generated. The unit address-status portion (word 2) of the channel status word (CSW) is available in the selector channel and may be read by an XIO sense device.

Sense

This command performs in the same manner as a read, except that the data is obtained from status indicators rather than from a record source.

The status information is transferred to ascending core storage locations beginning with the address specified by the CCW data address field. Two bytes of status information are placed in each core storage word. The number of sense bytes transferred is specified by the CCW byte-count and should be

limited to the number of sense bytes available in the particular I/O device.

Data transferred during a sense operation provides information concerning unusual conditions detected during the last operation and the current status of the I/O device. The device status provides a more detailed definition of the conditions that may cause a unit check indication in the unit status portion of the CSW. For example, Figure 108 shows the four basic sense bytes provided by the 2841/2311 combination. The functions of the individual indicators are described in the IBM System/360 Components Description -- 2841 and Associated DASD, Order No. GA26-5988.

Transfer—In—Channel (TIC)

This command causes the selector channel to automatically fetch the next CCW from three contiguous core storage locations beginning with the address specified by the data address field in the TIC CCW. TIC does not initiate any I/O operations, and the control unit is not aware of the command. The byte count portion of the CCW is not used.

TIC provides a means of chaining between CCW's not located in adjacent three-word areas of core storage. TIC performs as an unconditional branch regardless of the status of the chain data (CD) flag in the CCW.

Data Chaining

Data transfers between core storage and an I/O device may be chained by turning on the chain data flag (bit 0 of the second CCW word). Data chaining permits blocks of data to be transferred to or from noncontiguous areas of core storage, thus allowing rearrangement of data as it is transferred. Data chaining may also be used in conjunction with the skip function to enable the program to place selected portions of the block of data into core storage.

When data chaining is specified, the selector channel fetches a new CCW upon completion of data transfer for the current CCW. Unless the new CCW command code specifies transfer-in-channel, it is ignored while data chaining.

The selector channel requires approximately 12-μs to complete a data chaining function on a 2-μs system. If a device either requests or presents another byte of data during the data chaining function, an overrun condition occurs.

Therefore, the device data rate must be considered when using data chaining. Because of the data rate of the 2311, for example, data chaining is permitted only during the gap between the defined data fields on a track.

Sense Byte 0	Sense Byte 1	Sense Byte 2	Sense Byte 3
Command Reject	Data Check in Count Area	Unsafe	Ready
Intervention Required	Track Overrun	not used	On Line
Bus-Out Parity	End of Cylinder	Serializer Check	Unsafe
Equipment Check	Invalid Sequence	not used	not used
Data Check	No Record Found	ALU Check	On Line
Overrun	File Protected	Unselected File Status	End of Cylinder
Track Condition Check	Missing Address Marker	not used	not used
Seek Check	Overflow Incomplete	not used	Seek Incomplete

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Figure 108. 2841/2311 Sense Bytes

Data Chaining Termination

If the device sends channel end after exhausting the count of the current CCW, but before transferring any data to or from the storage area designated by the new CCW, the CSW associated with the termination will indicate incorrect length. Unless a program check is detected in an intervening transfer-in-channel command, the contents of the CSW pertain to the new CCW.

If a parity error is detected in the new CCW or during its fetching, a program check condition is generated and the channel terminates the operation. This combination of events results in an overrun condition, which requires a halt I/O to clear.

Self—Describing Blocks

When a channel program data-chains to a CCW placed in core storage by the CCW specifying data chaining, the input block is said to be self-describing. A self-describing block contains one or more CCW's that specify storage locations and counts for subsequent data in the same input block.

Use of self-describing blocks is equivalent to use of unchecked data. A data transfer malfunction that affects the validity of a block of data normally does not prematurely terminate or otherwise affect execution of the operation, and the malfunction is not signaled until data transfer is completed. Thus, there is no assurance that a CCW read as valid data actually is valid until the operation is completed.

If a data transfer error occurs while reading a self-describing CCW, data can be placed into the wrong core storage locations, causing destruction of data when the CCW is executed. If an error in a CCW is capable of causing subsequent command chaining, it may cause chaining to a write command; the result can be alteration of data at the I/O device.

Skip

Skipping suppresses transfer of data to core storage during a read or sense operation. Skipping is initiated by turning on the skip flag in the CCW (bit 4 of the second word).

The skip function affects only the handling of data by the channel. The operation at the control unit and device proceeds normally, and data is transferred to the channel. The channel keeps updating the byte count, but does not transfer the data to core storage. If the chain data flag is on, a new CCW is fetched when the byte count reaches 0. Normal operation is resumed if the skip flag in the new CCW is off.

Skipping is normally used in conjunction with data chaining to place only selected portions of data from an I/O device into core storage. To accomplish this, the ability to data-chain within a data field is required. Therefore, the skip function is negated with devices, such as the 2311, with data rates that restrict data chaining within data fields.

Channel Status Word

The channel status word (CSW) provides a means for the program to determine the status of an I/O device or the conditions under which an I/O operation has been terminated. The CSW is formed, or parts of it replaced, in the process of I/O interrupts and during execution of an XIO initialize write (start I/O).

The CSW consists of four 16-bit words:

Word 1 -- Selector channel status.
Word 2 -- Unit address-unit status.
Word 3 -- Command address.
Word 4 -- Byte count.

Selector Channel Status (CSW Word 1)

An XIO sense device with modifier bits 13 and 14 both off reads the selector channel status portion of the CSW into the accumulator. Whether an indicator bit will be on or off is determined by conditions existing at the channel, control unit, or device as a result of processing an I/O instruction.

Channel status is updated as it occurs and may be sensed by the program at any time. Figure 109 shows the various channel status indicators and denotes those indicators that cause interrupts.

NOT OPERATIONAL: This indicator turns on, causing an interrupt, if: (1) the control unit addressed by an XIO is not attached to the system, or (2) the device address specified by an XIO exceeds the number that the control unit is designed to handle.

UNIT STATUS PENDING: This indicator turns on, causing an interrupt, when the channel accepts status presented by a control unit or device. The conditions causing status to be presented to the channel depend on the control unit and device.

Once status is accepted by the channel, polling is suppressed (preventing overrun of status from another control unit or device) until it is reinitiated by the program. This allows the program to (1) determine the cause of the interrupt, (2) sense the unit address-status, and (3) reset the unit status pending indicator prior to reinitiation of polling.

The unit status pending indicator can be reset only by sensing the unit address-status portion of the CSW with an XIO sense device with reset (modifier bits 13, 14, and 15 equal 011).

It should be noted that the unit address-status portion of the CSW is valid only when sensed in response to a unit status pending interrupt.

PROGRAM CONTROL INTERRUPT: This indicator turns on, causing an interrupt, when the channel fetches a channel command word (CCW) in which the program control interruption flag is on.

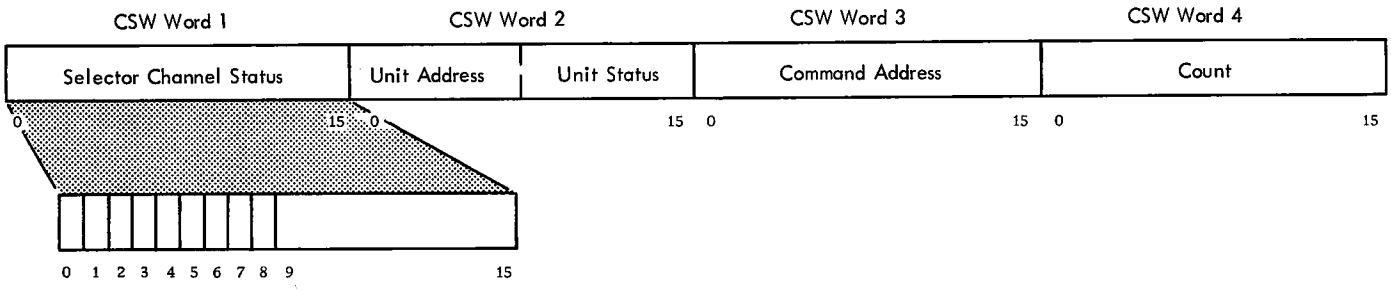
PROGRAM CHECK: This indicator turns on, causing an interrupt, if either of the following conditions is detected:

1. An input/output control command (IOCC) has a function code that is invalid for the selector channel. Valid function codes are: control (halt I/O) 100, initialize write (start I/O) 101, sense device 111, and sense interrupt level 011.
2. An IOCC or CCW has incorrect parity.

If a program check occurs during initiation of an operation, execution of the operation is suppressed. If a program check is detected after a device has been started, the device is signaled to terminate the operation.

A program check condition causes command chaining to be suppressed.

CHANNEL DATA CHECK: This indicator turns on if:



Bit	Indication	Interrupt
0	Not Operational	Yes
1	Unit Status Pending	Yes
2	Program Control Interrupt	Yes
3	Program Check	Yes
4	Channel Data Check	No
5	Interface Control Check	No
6	Incorrect Length	No
7	Adapter Busy	No
8	Unit Operational	No
9-15	Not Used	

Note: Bits 0, 2, and 3 are reset only if modifier bit 15 is on in the XIO sense device.
Bit 1 is reset by an XIO sense device with modifier bits 13, 14, and 15 set to 011 (sense CSW word 2 with reset).

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Figure 109. Selector Channel Status (CSW Word 1)

1. The P-C detects a parity error in a data word transferred from the channel to core storage. In this case, the P-C does not correct parity before placing the data word in core storage.
2. The channel attempts to store data in a storage protected core storage location. The data in the storage protected location is not altered.

A channel data check does not terminate the current operation. However, transfer of the remaining data is suppressed and the channel attempts to place 0's in the remaining core storage locations. This operation continues until the byte count specified in the current CCW reaches 0.

A channel data check suppresses command chaining and the program is interrupted when the device presents channel end at the completion of the current operation.

INTERFACE CONTROL CHECK: This indicator turns on if the channel detects an invalid signal on the channel to control unit interface. This check usually indicates a malfunction in a I/O device. An interface control check condition is detected if:

1. A device responds with an address other than the address specified by the channel during initiation of an operation.
2. An "in" tag signal from a device occurs simultaneously with another "in" tag signal.

Detection of an interface control check causes immediate termination of the current operation.

INCORRECT LENGTH: This indicator is used to inform the program if an incorrect length condition is detected. An incorrect length condition occurs if the number of bytes designated by the byte count in a CCW is not equal to the number of bytes requested or offered by an I/O device. This condition may occur due to any one of the following reasons:

1. Long block on input -- A device attempts to transfer one or more bytes of data to core storage after the byte count has reached 0 during a read or sense operation.
2. Short block on input -- The number of bytes transferred during a read or sense operation is insufficient to reduce the byte count to 0.

3. Short block on output -- The device terminates a write or control operation before the byte count reaches 0.
4. Long block on output -- The device requests another byte from the channel after the byte count has reached 0 during a write or control operation.

Indication of a incorrect length condition may be suppressed as described under "Suppress Length Indication."

Note that if an incorrect length condition occurs and the suppress length indication (SLI) flag in the CCW is not on, command chaining (if specified) is suppressed.

ADAPTER BUSY: This indicator is on when the channel is executing a previous XIO, servicing, a device request, or servicing a control unit request. Adapter busy indicates that the channel cannot initiate a new operation because a previously initiated operation is being executed or status conditions exist. Therefore, an XIO initialize write (start I/O) is ignored if given while adapter busy is on. However, an XIO control (halt I/O) or XIO sense device is executed.

UNIT OPERATIONAL: This indicator turns on when the data transfer portion of a start I/O operation begins and remains on until ending status is received. Unit operational is turned on only by commands requiring data transfer. Test I/O and immediate commands do not turn on this indicator.

Unit Address–Status (CSW Word 2)

An XIO sense device with modifier bit 13 off and modifier bit 14 on reads the unit address-status portion of the CSW into the accumulator. If modifier bit 15 is on, the unit status pending bit in word 1 of the CSW is reset.

The unit address portion of the word identifies the control unit and device specified in the last XIO executed or rejected. The unit status portion of the word identifies conditions detected in the control unit and device. Unit status indicators are presented to the channel by the control unit and device. The channel does not modify these status indicators and they appear in the CSW as received from the control unit and device.

The unit address-status portion of the CSW is valid only when sensed in response to a unit status pending interrupt.

Figure 110 shows the format of the unit address-status portion of the CSW. The individual indicators are described in the following paragraphs.

CONTROL UNIT ADDRESS: These four bits (0 through 3) indicate the control unit specified in the last XIO executed or rejected.

DEVICE ADDRESS: These four bits (4 through 7) indicate the device specified in the last XIO executed or rejected.

ATTENTION: When on, attention indicates that the device has detected an asynchronous condition that is significant to the program. Attention is not associated with initiation, execution, or termination of an I/O operation.

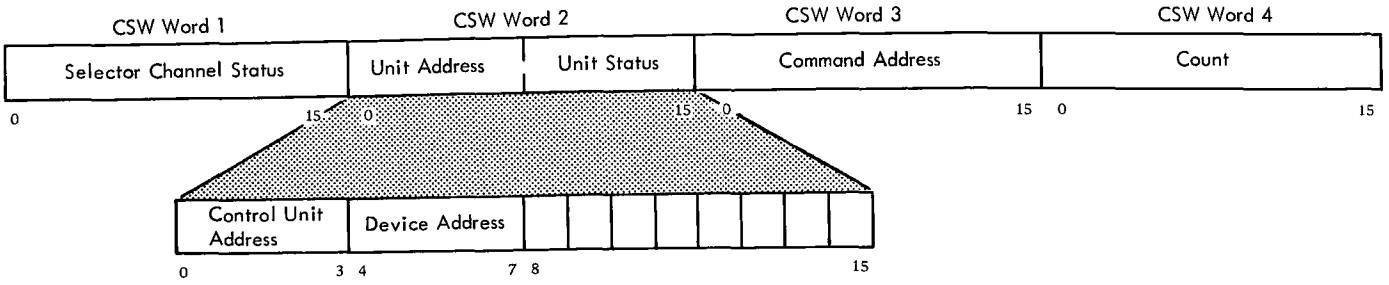
Attention cannot be presented to the channel while an operation is in progress at the device, control unit, or channel. Otherwise, the handling and presentation of attention to the channel depends on the type of device.

If attention is presented to the channel during initiation of an operation, the operation is not started. Attention presented with device end causes command chaining to be suppressed.

STATUS MODIFIER: Status modifier is generated by the device when the normal sequence of commands must be modified or when the control unit, during initial selection, detects that it cannot execute the command or instruction as specified.

The status modifier and busy may both be on in the CSW. This combination indicates that the busy condition pertains to the control unit associated with the addressed device. The control unit appears busy while it is executing a type of operation, or is in a state, that precludes acceptance of any command. A typical example is a 2311 seek command, during which the control unit may remain busy after it has signaled channel end. A status modifier and busy combination may be presented in response to any command.

Once execution of a command has started, the status modifier indication can occur only with device end. If command chaining is specified in the current CCW when device end and status modifier are indicated, the channel will fetch and chain to the CCW whose core storage location is 6 higher than that of the current CCW. Since the core storage location of the next CCW in a chain is normally 3 storage locations higher than the current CCW, the status modifier condition effectively provides a branching capability for the program.



Bit	Indication
0-7	Identifies the control unit and I/O device specified in the last I/O operation executed or rejected
8	Attention
9	Status Modifier
10	Control Unit End
11	Busy
12	Channel End
13	Device End
14	Unit Check
15	Unit Exception

25438B

Figure 110. Unit Address-Status (CSW Word 2)

CONTROL UNIT END: This status indicator is generated only by control units shared by I/O devices, and only when one or both of the following conditions occur:

1. The control unit is interrogated while executing an operation. The control unit is considered to be interrogated when, during a previous initial selection sequence, the control unit responded with busy and status modifier in the unit status portion of the CSW.
2. The control unit detects an unusual condition while busy, but after channel end is accepted by the channel.

Control unit end is not signaled if the control unit remains busy after signaling channel end, unless the control unit detects an unusual condition or is interrogated by the program.

If the control unit is in temporary busy state when interrogated, control unit end is included with busy and status modifier even though the control unit is not yet free. A busy condition is considered temporary if its duration is less than 2 ms.

A pending control unit end causes the control unit to appear busy and any new start I/O operation is ignored.

The device address posted with control unit end is determined as follows:

1. If control unit end is presented with channel end and/or device end, the address of the selected device is used.
2. If control unit end is presented without channel end or device end during a control-unit-initiated selection sequence, the device address may be any legitimate address associated with the control unit. (A legitimate address is any address the control unit is capable of recognizing, regardless of whether the device is actually attached.)
3. If control unit end is presented during an initial selection sequence, the device address is the same as the device address specified for the operation.

BUSY: When on, busy indicates that the I/O device or control unit cannot accept another start I/O operation because a previously initiated operation is in progress or status conditions exist. (An operation is considered to be in progress from the time status is accepted during initial selection until device end is accepted.) Busy is presented only during initial selection sequence. Status conditions, if any, accompany the busy condition.

If a busy condition applies to the control unit, busy is accompanied by status modifier.

CHANNEL END: This status indicator is generated when the portion of an I/O operation involving transfer, if any, of data or control information between the I/O device and channel is completed.

Each I/O operation causes only one channel-end signal. Channel end is not signaled unless the operation is initiated. The exact time during an I/O operation that channel end occurs depends on the operation and type of device. For control operations, channel end usually occurs after the control information is transferred to the control unit. For data transfer operations such as writing, channel end occurs after the block of data has been written. For immediate operations that do not involve transfer of control information or data, channel end can occur during the initial selection sequence.

When command chaining is specified, only the channel end following the last operation of the chain is presented to the program. Channel end is not presented to the program if a chain of commands is prematurely terminated by presentation of an unusual condition with control unit end or device end.

DEVICE END: This status indicator is generated when an I/O operation at the device is completed or, on some devices, when the device is manually changed from a not ready to a ready state. Device end is presented only once for each I/O operation and normally indicates that the I/O device has completed the current operation. Device end is not presented unless the operation is initiated.

Device end associated with an I/O operation may be presented either simultaneously with channel end or later. For data transfer operations, the device terminates the operation at the time channel end is generated, and device end is presented together with channel end. For control operations, device end is presented when the operation at the device is completed. The operation may be completed at the time channel end is generated or later.

When command chaining is specified, only the device end for the last operation of the chain is presented to the program. During command chaining, the channel initiates a new operation upon receipt of device end without unusual status conditions.

UNIT CHECK: When on, unit check indicates that the I/O device or control unit requires programming or manual intervention, but does not necessarily indicate an error condition. The conditions causing a unit check are identified by data available to a sense command, which should normally follow acceptance of unit check status. Unit check is a summary indication of the conditions indicated by the sense data.

An error condition causes unit check only when it occurs during execution of a command or during activity associated with an I/O operation. Unless an error pertains to the activity initiated by a command and is of immediate significance to the program, unit check is not presented to the program once device end is cleared. If the device becomes not ready when it is not executing an operation and does not have a pending interrupt condition, unit check is signaled to the program the next time the device is selected.

If, during the initial selection sequence, the I/O device detects that the command cannot be executed, unit check is presented to the channel without channel end, control unit end, or device end. This condition indicates that no action has been taken at the device in response to the command. If the condition precluding proper execution of the operation occurs after execution has begun, unit check is accompanied by channel end, control unit end, or device end, depending on when the condition is detected.

Invalid command codes or command codes with incorrect parity do not cause unit check if the I/O device is busy or holding status at the time of selection. Under these circumstances, the device responds with busy and indicates the pending status. Command code validity is ignored.

Termination of an operation with a unit check indication causes command chaining to be suppressed.

UNIT EXCEPTION: Unit exception indicates that the I/O device detected an unusual condition such as end of file. Unit exception has only one meaning for any particular command and type of I/O device. A sense command is not required as a response to acceptance of unit exception.

Unit exception can be generated only when the I/O device is executing an I/O operation, or when the device is involved with some activitiy associated with an I/O operation and the condition is of immediate significance. If a device detects a unit-exception condition during the initial selection sequence, unit exception is presented to the channel without channel end, control unit end, or device end. This condition indicates that no action has been taken at the device in response to the command. If a unit exception condition which precludes normal execution of an operation is detected after execution has started, unit exception is accompanied by channel end, control unit end, or device end, depending on when the condition is detected.

Any unit exception condition associated with an operation, but detected after device end is cleared, is indicated by presenting unit exception with attention.

Termination of an operation with a unit exception indication causes command chaining to be suppressed.

Command Address (CSW Word 3)

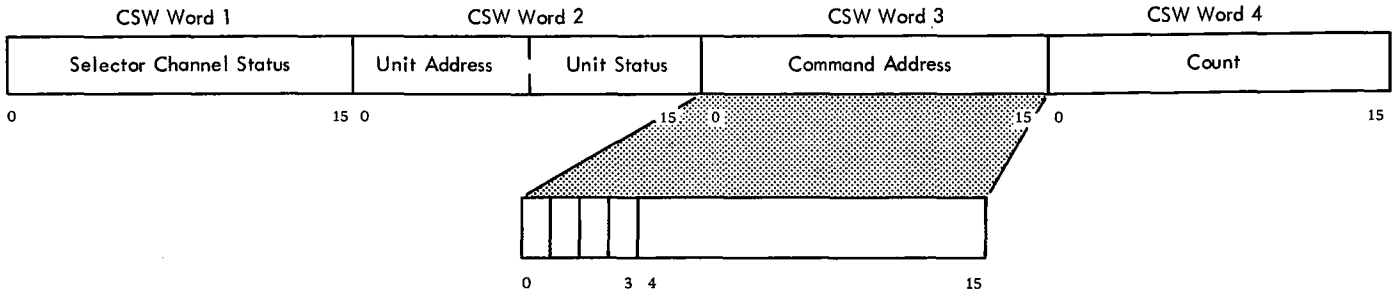
An XIO sense device with modifier bit 13 on and modifier bit 14 off reads the command address portion of the CSW into the accumulator. The significance of the bits in this word is shown in Figure 111.

Command address may be sensed at any time and indicates a core storage address 3 higher than the address of the CCW being executed or just completed.

Count (CSW Word 4)

An XIO sense device with modifier bits 13 and 14 both on reads the count portion of the CSW into the accumulator. The significance of the bits in this word is shown in Figure 112.

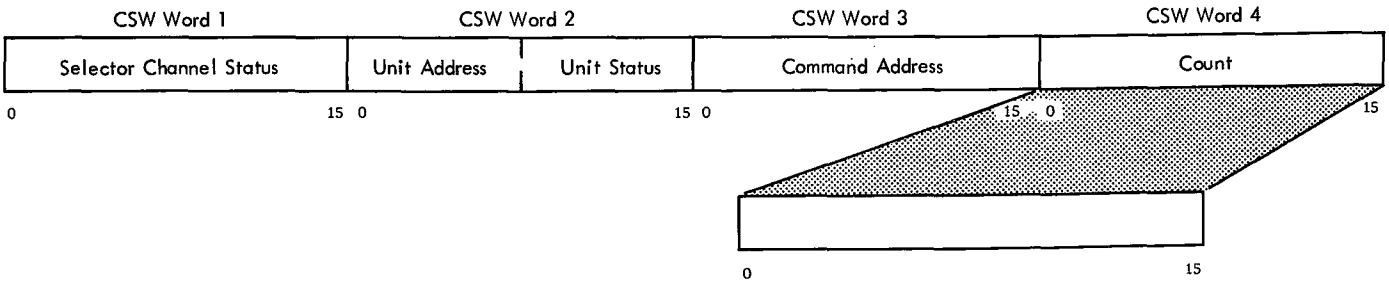
The count represents the residual byte count for the last CCW used and may be sensed only when the adapter busy indicator in word 1 of the CSW is off, or when no channel-initiated operation is in progress. If the count is sensed at any other time, the information is unpredictable.



Bit	Indication
0	Used only with 65,536 word core storage
1	Used with 24,576 word core storage and above
2	Used with 16,384 word core storage and above
3	Used with 8,192 word core storage and above
4-15	Used with bits 0-3 (if applicable) and specifies an address three higher than the address of the last CCW used

30207A

Figure 111. Command Address (CSW Word 3)



Bit	Indication
0-15	Forms the residual count (expressed in two's complement form plus one) for the last CCW used.

25440A

Figure 112. Count (CSW Word 4)

INITIATION OF SELECTOR CHANNEL OPERATIONS

The operation specified by an XIO initialize write (start I/O) is initiated only when the channel, control unit, and device are in the available state. Prior to giving a start I/O, the program must interrogate the channel status to determine that the channel is not busy. If a start I/O is given while the channel is busy, it is ignored and no indication of this is given to the program.

A start I/O given to a channel that is in the available state is accepted by the channel. This acceptance initiates an initial selection sequence during which the status conditions of the control unit and I/O devices are examined. These status conditions determine whether the operation proceeds or is terminated, according to the following rules:

1. If either the control unit or I/O device is busy, the channel is presented with busy status, the command is not executed, and a unit status pending interrupt is given to the program. The program must then execute an XIO sense device with modifier bit 13 off and modifier bit 14 on to read the unit address status into the accumulator for interrogation. (Unit status pending is not reset until the unit address-status is sensed with an XIO sense device with reset; that is, with modifier bit 15 on.)
2. If either the control unit or I/O device addressed is not operational, the address is not recognized during the initial selection sequence, the command is not executed, and a not operational interrupt is given to the program.
3. If the control unit and I/O device are both available, the operation specified by the start I/O is executed.

TERMINATION OF SELECTOR CHANNEL OPERATIONS

Normally, an I/O operation at the channel lasts until the device signals channel end. Channel end can be signaled during the sequence initiating the operation or later. If the channel detects an equipment malfunction, or a system reset is performed, the channel disconnects the device without receiving channel end.

Termination During Initiation

A data transfer operation is initiated at the I/O device only when no programming or equipment errors are detected by the channel, and the device responds with 0 status (available) during the initiation of the command. When the channel detects, or the device signals any unusual condition during the initiation of an operation, and channel end is off, the command is rejected.

If a command is rejected during execution of a start I/O, the device is not started, an interrupt condition is generated, and the channel becomes available immediately after the initiation sequence. The conditions that precluded the initiation are detailed in the channel status and unit address-status portions of the CSW.

Unless the command was rejected because the I/O device was busy or not operational, the device is immediately available for initiation of another operation.

If an unusual condition causes a command to be rejected during initiation of an I/O operation by command chaining, an interrupt condition is generated and the device is not available until the condition is cleared. The unusual conditions are indicated to the program by means of the corresponding status bits in the CSW.

The new operation at the I/O device is not started.

Termination Without Data Transfer

Immediate Operations

Instead of accepting or rejecting a command, the I/O device can signal channel end immediately upon receipt of the command code. An I/O operation causing channel end to be signaled during the initiation sequence is called an immediate operation.

If command chaining is not specified, receipt of channel end causes unit status pending to turn on in the CSW. (The CSW also contains channel end and any other indications provided by the channel or I/O device.) Unit status pending causes the channel to interrupt the program. However, the I/O operation is initiated and the channel is immediately made available to the program. If channel end is not accompanied by device end, the device remains busy.

Device end, when subsequently provided by the device, causes an interrupt condition to be generated.

When command chaining is specified after an immediate operation and no unusual conditions have been detected during the execution of the command, no interrupt condition is generated. The subsequent commands in the chain are handled normally, and channel end for the last operation in the chain causes the program to be interrupted. The non-0 byte count required for immediate operations does not result in a program check, incorrect length indication, or suppression of command chaining.

Pending Interruption

If a start I/O addresses an I/O device having a pending interrupt condition due to device end or attention, or if a start I/O addresses a control unit having a pending channel end or device end for the device, then the channel status and unit address-status portions of the CSW are set. The unit status field contains the busy indicator, identifies the interrupt, and may contain other indicators provided by the control unit or I/O device. The pending interrupt condition is cleared and unit status pending in the channel status field is turned on, causing an interrupt to the program. The remaining indicators in the channel status field are off.

The operation is not initiated, and the channel is free as soon as the initiation sequence is completed. Thus the channel and I/O device are immediately available for initiation of another operation.

Device or Control Unit Busy

If a start I/O addresses an I/O device that is busy, a control unit that is busy, or a control unit that has a pending channel end or control unit end for a device other than the one addressed, then the channel status and unit address-status portions of the CSW are set. The unit status field contains the busy indicator or, if the control unit is busy, the busy and status modifier indicators. Unit status pending in the channel status field is turned on, causing an interrupt to the program. The remaining indicators in the channel status field are off.

The operation is not initiated, and the channel is free immediately after the initiation sequence.

Termination With Data Transfer

For operations involving data transfer, either the channel or I/O device can control the timing of the channel end condition. If command chaining is not specified, or if chaining is suppressed because of unusual conditions, channel end causes termination of the operation at the channel. The status indicators in the associated CSW indicate channel end and unusual conditions, if any.

The I/O device can signal channel end any time after the initiation of the operation. Channel end may occur prior to any actual data transfer.

The channel signals the device to terminate data transfer whenever any of the following conditions occur:

1. The storage areas specified for the operation are exhausted or filled. This condition occurs when the channel has decreased the count in the last CCW associated with the operation to 0. A count of 0 indicates that the channel has transferred all information specified by the program.
2. A program or unit check condition is detected. This condition is due to errors and causes premature termination of the operation.
3. An XIO control (halt I/O) is executed. Execution of a halt I/O automatically disconnects the device from the channel.

If command chaining is specified, the device executing the operation remains connected to the channel until the last command of the chain has been executed. Any unusual conditions cause command chaining to be suppressed and a terminating condition to be generated. The unusual conditions can be detected by the channel or the I/O device. If the channel is aware of the unusual condition by the time channel end is signaled for the operation, the chain is terminated as if the operation in which the unusual conditions occurred were the last operation in the chain.

Termination With Halt I/O

Execution of a halt I/O terminates the current I/O operation at the addressed selector channel, control unit, or I/O device. If the channel is not busy, modifier bits 8 through 15 of the halt I/O identify the control unit and I/O device to which the halt I/O applies.

When the channel is available, and the control unit is busy, the addressed device is signaled to terminate the current operation. Halt I/O does not affect the state of the control unit when both channel and control unit are available.

If halt I/O is issued when the channel is executing a data transfer, the data transfer is terminated and the device performing the operation is immediately disconnected from the channel. In this case,

modifier bits 8 through 15 of the halt I/O are ignored.

Termination of an operation as a result of a halt I/O causes the channel and control unit to be placed in the interrupt pending state. When the channel is in interrupt pending state or available, and the control unit is in the interrupt pending state, execution of halt I/O does not affect the state of either the channel or the control unit.

The CSW set during halt I/O pertains only to the execution of halt I/O. It does not describe under what conditions the I/O operation at the addressed device was terminated. If the addressed device has been selected and signaled to terminate the current operation, the unit status field of the CSW is 0 unless an equipment error is detected. If an equipment error is detected, the status indicators in the CSW identify the error condition. The state of the channel and the progress of the I/O operation are unpredictable.

When halt I/O causes a data transfer operation to be terminated, the control unit associated with the operation remains busy until the data handling portion of the operation in the control unit is terminated. Termination of data handing in the control unit is signaled by channel end. Channel end may occur at the normal time or earlier or later, depending upon the operation and type of device.

If the control unit is shared, all devices attached to the control unit appear busy until channel end is accepted by the P-C. The I/O device executing the terminated operation remains busy until termination of the operation. At this time the device signals the channel with device end.

System/360 Adapter

INTRODUCTION

The System/360 adapter (located within an 1826 Data Adapter Unit) permits communication between the 1800 and System/360. Each system regards the other as an I/O device capable of requesting service on a random basis. The System/360 adapter is functionally equivalent to the System/360 channel-to-channel adapter.

The System/360 adapter provides the ability to transfer blocks of data and/or programs at rates up to 250, 000 bytes per second between the System/360 and 1800 system.

Addressing

The System/360 adapter has two device addresses: one which responds to the System/360, and one which responds to the 1800. The System/360 device address is assigned during installation of the system. The 1800 device address is fixed; that is, area code 01101. Each assignment conforms to the channel requirements of the respective system

Mode of Operation

To the System/360 channel, the adapter appears as a control unit operating in burst mode. To the 1800 system, the adapter appears as an I/O device operating on a data channel.

The priority of the System/360 adapter is selected for the 1800 by assigning a particular interrupt level and a particular data channel priority to the adapter. Adapter priority for the System/360 is governed by its position on the System/360 channel.

Data Transfer

Data transfer between the two systems is initiated only when the System/360 adapter has received complementary commands from both systems; that is, an 1800 XIO initialize read and a System/360 write, or an 1800 XIO initialize write and a System/360 read.

Data is transferred between the 1800 and System/360 adapter two 8-bit bytes at a time; data is transferred between the System/360 and System/360 adapter one 8-bit byte at a time. The System/360 adapter contains an 18-bit buffer register (16 data bits and 2 parity bits) for serializing the bytes to the System/360 and deserializing the bytes received from the System/360. The byte located is bit positions 0 through 7 of an 1800 word is loaded or transferred first over the System/360 channel.

A word count (1800) and byte count (System/360) must be specified for a data transfer operation. Whichever count is least will terminate the data transfer. (One word count equals two byte counts.) If the word count and byte count read zero simultaneously, the 1800 terminates the operation. If the System/360 terminates the operation with an odd byte count, the last byte from the 1800 is lost.

Power On/Off Considerations

Care should be used when turning power to the 1800 system on or off to ensure that the System/360 adapter is off-line and that the off-line switch for the adapter is in the bypass/gated position. Failure to place the adapter off-line switch in the bypass/gated position before the power transition may force System/360 channel failures.

SYSTEM/360 COMMANDS

The System/360 adapter decodes and responds to the System/360 command codes shown in Figure 113.

The read, read backward, write, and control command bytes, after being accepted by the adapter, are available to the 1800 system program by use of an XIO sense device. Since the modifier bits (M) in

Command	Bit Configuration
Test I/O	0 0 0 0 0 0 0 0
Write	M M M M M S 0 1
Read	M M M M M S 1 0
Control	M M M M M 1 1 1
Sense	M M M M 0 1 0 0
Read Backward	M M M M 1 1 0 0
No Operation	M M M M M 0 1 1

17894

Figure 113. System/360 Commands

these command bytes are ignored by the adapter, they may be used for communication purposes to the 1800 program.

The suppress bit (S) being on in a read or write command byte suppresses the interrupt to the 1800 normally generated when the System/360 adapter accepts either of these commands. This enables use of a two-command sequence from the System/360 to initiate a data transfer operation and yet cause only one interrupt to the 1800 program. For example, the System/360 may issue a control that causes an interrupt to the 1800 program and identifies the desired operation by means of the command byte modifier bits. The control is then followed by a read or write command to complete the operation. These commands may or may not be chained. The 1800 responds to the interrupt generated by the control with an XIO sense device, and with a subsequent XIO initialize read or XIO initialize write, as required, to complete the operation indicated by the control modifier bits. Because the control informs the 1800 program of the type of command pending from the System/360, another interrupt to the 1800 when the System/360 adapter receives the read or write command is unnecessary. Therefore, the read or write command with the suppress bit on can be given, thus eliminating an unnecessary interrupt.

The following descriptions of System/360 commands include statements regarding the resulting condition code. For definition and application of the condition codes, refer to IBM System/360 Principles of Operation, Order No. GA22-6821. For clarity, all 1800 commands in this section are prefixed with XIO. No prefix is included with System/360 commands.

Control (System/360)

When accepted by the System/360 adapter, this command is treated as an immediate command; that is, channel end is sent to the System/360 in response to the initial selection. This immediately releases the channel if command chaining is not specified.

The modifier bits in the command byte are ignored by the adapter and may be used to communicate the particular type of transfer requested by the System/360. A control command used for this purpose normally is command-chained to a subsequent read or write command, depending on the operation necessary to complete the transfer.

The response to a System/360 control depends on the status of the adapter, according to the following rules.

IDLE ADAPTER: An idle adapter accepts a control command by responding to initial selection with channel end (thus releasing the System/360 channel), by saving the complete command byte (including modifiers), and by generating a 360 command stored interrupt for the 1800 system. The System/360 condition code resulting from the command is 1, status stored. The 1800 program responds to the interrupt by issuing an XIO sense device to read the adapter device status word (DSW) into the accumulator. The DSW contains the System/360 command byte from the adapter. The XIO sense device causes the adapter to signal the System/360 with device end.

BUSY ADAPTER: A System/360 control command may be rejected because of any one of the following adapter busy conditions.

1. A second System/360 control command is issued before a previous control command is cleared by an XIO sense device from the 1800. In this case, the adapter responds with busy. This response results in a condition code of 2, busy.
2. A second System/360 control command is issued after a previous control command has been cleared, but before device end has been accepted by the System/360. In this case, the adapter responds with busy and device end. This response results in a condition code of 1, status stored and clears device end from the adapter, leaving the adapter idle.
3. A System/360 control command is issued after the adapter has previously accepted an XIO initialize read or XIO initialize write from the 1800. In this case, the adapter responds with busy and attention. This response results in a condition code of 1, status stored. If the attention status generated by the XIO initialize read or XIO initialize write was not previously accepted, this response clears it and it no longer attempts to interrupt the System/360. If another control, no-operation, or noncomplementary read or write command is given, the adapter responds again with busy and attention.

Sense (System/360)

This command is normally given in response to attention status, which indicates that the 1800 is attempting to initiate a transfer operation. When accepted by the adapter, a System/360 sense command causes one or two bytes of sense data to be placed into core storage starting at the address

specified by the channel command word (CCW). The number of bytes is determined by the CCW byte count. Status returned by the adapter during initial selection will be 0, and ending status will be channel end and device end. If the adapter has previously accepted an XIO initialize read or XIO initialize write from the 1800 and the System/360 has not yet issued the complementary command, attention is also given with ending status.

The contents of the two bytes of sense data stored depend on the conditions in the adapter, as shown in Figure 114.

The only exception to the sense operation described in the preceding paragraphs occurs when the System/360 issues a sense command before a previous control command has been cleared and device end accepted for the control command. If the control has not been cleared by an XIO sense device from the 1800, the adapter responds with busy, which results in a condition code of 2, busy. If the control has been cleared, but device end has not yet been accepted or has been stacked by the System/360, the adapter responds with busy and device end. This response results in a condition code of 1, status stored and clears device end from the adapter, leaving the adapter idle.

Read or Read Backward (System/360)

The primary function of a read or read backward command is transmission of data from the 1800 to the System/360. The adapter recognizes no difference in the function to be performed by these two commands. However, the suppress interrupt bit (S) is not available in the read backward command. Therefore, the interrupt to the 1800 cannot be suppressed when using the read backward command. Either a read or a read backward command may be used as the complementary command to an XIO initialize write from the 1800. The adapter response

Condition	High-Order Buffer BYTE 1	Low-Order Buffer BYTE 2
Adapter Idle	Undefined	Undefined
1800 Previously Issued:		
XIO Initialize Read	Area/Function	Modifier
XIO Initialize Write	Area/Function	Modifier
XIO Control	Zero	Zero

17446B

Figure 114. Sense Bytes Presented to System/360

to a System/360 read or read backward command depends on the status of the adapter, according to the following rules.

IDLE ADAPTER: An idle adapter accepts a read command by responding during initial selection with 0 status. This response results in a condition code of 0, operation initiated. System/360 channel operation is then suspended until the adapter receives the complementary command (an XIO initialize write) from the 1800. Unless suppressed by the S-bit being on in the command byte, a 360 command stored interrupt is generated by the adapter to signal the 1800 of the pending operation. The complete command byte (including modifiers) is saved by the adapter and is available to an XIO sense device from the 1800.

WAITING XIO INITIALIZE WRITE: An adapter holding a previously accepted XIO initialize write from the 1800 accepts a System/360 read command by responding to initial selection with 0 status. This response results in a condition code of 0, operation initiated. (The adapter responds with 0 status regardless of whether or not the System/360 has accepted the attention status generated by the XIO initialize write.) Both the XIO initialize write and System/360 read operations are initiated. The data transfer operation continues until the System/360 byte count for the read or the 1800 word count for the XIO initialize write is decreased to 0, or until an error condition is detected. If neither channel is data chaining when the byte count or word count reaches 0, channel end and device end is given to the System/360. Acceptance of the ending status by the System/360 releases the adapter and returns it to idle. The 1800 system is signaled by a transfer end interrupt. If the System/360 terminated the operation, the halt indicator will also be on in the device status word (DSW).

BUSY ADAPTER: A System/360 read command may be rejected because of any one of the following adapter busy conditions:

1. A System/360 read command is issued before a previous control command is cleared by an XIO sense device from the 1800. In this case, the adapter responds with busy. This response results in a condition code of 2, busy.
2. A System/360 read command is issued after a previous control command has been cleared, but before device end has been accepted by the System/360. In this case, the adapter responds with busy and device end. This response results

in a condition code of 1, status stored and clears device end from the adapter leaving the adapter idle.

3. A System/360 read command is issued after the adapter has previously accepted an XIO initialize read from the 1800. In this case, the adapter responds with busy and attention. This response results in a condition code of 1, status stored. If the attention status generated by the XIO initialize read was not previously accepted, this response clears that status. As a result, attention status no longer attempts to interrupt the System/360. However, attention still appears as a response to any read command until the previously accepted XIO initialize read has been satisfied.

Write (System/360)

The primary function of a write command is transmission of data from the System/360 to the 1800. Write is the complementary command to an XIO initialize read from the 1800. The adapter response to a System/360 write command depends on the status of the adapter, according to the following rules.

IDLE ADAPTER: An idle adapter accepts a write command by responding during initial selection with 0 status. This response results in a condition code of 0, operation initiated. System/360 channel operation is then suspended until the adapter receives the complementary command (an XIO initialize read) from the 1800. Unless suppressed by the S-bit being on in the command byte, a 360 command stored interrupt is generated by the adapter to signal the 1800 of the pending operation. The complete command byte (including modifiers) is saved by the adapter and is available to an XIO sense device from the 1800.

WAITING XIO INITIALIZE READ: An adapter holding a previously accepted XIO initialize write from the 1800 accepts a System/360 write command by responding to initial selection with 0 status. This response results in a condition code of 0, operation initiated. (The adapter responds with 0 status regardless of whether or not the System/360 has accepted the attention status generated by the XIO initialize read.) Both the XIO initialize read and System/360 write operations are initiated. The data transfer operation continues until the System/360 byte count for the write or the 1800 word count for the XIO initialize read is decreased to 0, or until an error condition is detected. If neither channel is data chaining when the byte count or word count reaches 0, channel end and device end are given to the System/360. Acceptance of the ending status by the System/360 releases the adapter and leaves it idle. The 1800 system is signaled by a transfer end interrupt. If the System/360 terminated the operation, the halt indicator will also be on in the device status word.

BUSY ADAPTER: A System/360 write command may be rejected because of any one of the following adapter busy conditions:

1. A System/360 write command is issued before a previous control command is cleared by an XIO sense device from the 1800. In this case, the adapter responds with busy. This response results in a condition code of 2, busy.
2. A System/360 write command is issued after a previous control command has been cleared, but before device end has been accepted by the System/360. In this case, the adapter responds with busy and device end. This response results in a condition code of 1, status stored and clears device end from the adapter, leaving the adapter idle.
3. A System/360 write command is issued after the adapter has previously accepted an XIO initialize write from the 1800. In this case, the adapter responds with busy and attention. This response results in a condition code of 1, status stored. If the attention status generated by the XIO initialize write was not previously accepted, this response clears that status. As a result attention no longer attempts to interrupt the System/360. However, attention still appears as a response to any write command until the previously accepted XIO initialize write has been satisfied.

Test I/O (System/360)

A test I/O may be used to obtain the status of the adapter any time the System/360 channel is available. The status received indicates the condition of the adapter as follows:

ZERO STATUS: This status indicates that the adapter was idle at the time of response and results in condition code of 0, available.

BUSY: This status indicates that a control command previously issued by the System/360 was not accepted by the adapter and results in a condition code of 2, busy.

ATTENTION: This status indicates that the adapter has accepted an XIO initialize read or XIO initialize write from the 1800 and results in a condition code of 1, status stored.

DEVICE END: This status in response to a test I/O indicates that a System/360 control command accepted by the adapter has been cleared by an XIO sense device from the 1800, but that device end has not yet been accepted by the System/360. The resulting condition code is 1, status stored. The test I/O clears device end from the adapter and leaves it idle.

CHANNEL END AND DEVICE END: This status in response to a test I/O indicates that a data transfer operation has been terminated, but that channel end and device end have not yet been accepted by the System/360. The resulting condition code is 1, status stored. The test I/O clears channel end and device end from the adapter and leaves it idle.

No-Operation (System/360)

This command is handled by the adapter as an immediate command. The adapter response to this command depends on the adapter status according to the following rules.

IDLE ADAPTER: An idle adapter accepts a no-operation command by responding to initial selection with channel end and device end. This response results in a condition code of 1, status stored. The adapter does not save the command byte, nor does it generate an interrupt to the 1800. Any command byte currently being saved by the adapter is not altered by a no-operation command.

BUSY ADAPTER: A System/360 no-operation command may be rejected because of any one of the following adapter busy conditions:

1. A System/360 no-operation command is issued before a previous control command is cleared by an XIO sense device from the 1800. In this case, the adapter responds with busy. This response results in a condition code of 2, busy.
2. A System/360 no-operation is issued after a previous control command has been cleared, but before device end has been accepted by the System/360. In this case, the adapter responds with busy and device end. This response results in a condition code of 1, status stored and clears device end from the adapter, leaving the adapter idle.
3. A System/360 no-operation command is issued after the adapter has previously accepted an XIO initialize read or XIO initialize write from the 1800. In this case, the adapter responds with busy and attention. This response results in a condition code of 1, status stored. If the attention status was not previously accepted, this response clears that status. As a result, attention no longer attempts to interrupt the System/360. However, attention still appears as a response to any no-operation command until the previously accepted XIO initialize read or XIO initialize write has been satisfied.

Halt I/O (System/360)

A halt I/O issued while the adapter is executing a System/360 read, read backward, write, or sense command causes immediate termination of the operation. The adapter responds with channel end and device end. This response results in a condition code of 2, burst operation terminated. If the 1800 is operating with the adapter, it is signaled by a transfer end and halt interrupt.

A halt I/O will be busy-rejected by the adapter if it is issued before a previous System/360 control command has been cleared by an XIO sense device from the 1800.

A halt I/O issued to an idle adapter results in a 0 status response to the System/360 (condition code 1, status stored).

1800 SYSTEM COMMANDS

System/360 adapter operations are initiated by the 1800 system by means of execute I/O (XIO) instructions. The input/output control command (IOCC) referenced by an XIO must have an area code of 01101 to address the System/360 adapter. Figure 115 shows the IOCC's that may be used to control adapter operation. All other IOCC's are considered invalid and will be rejected by the adapter.

After an XIO initialize read or XIO initialize write has been accepted by the adapter, the control word (area, function, and modifier) is available to the System/360 by use of the sense command. Since the modifiers in these commands are ignored by the adapter, they may be used for communication with the System/360 program.

Sense Device (1800)

This command causes the adapter device status word (DSW) or word count to be read into the

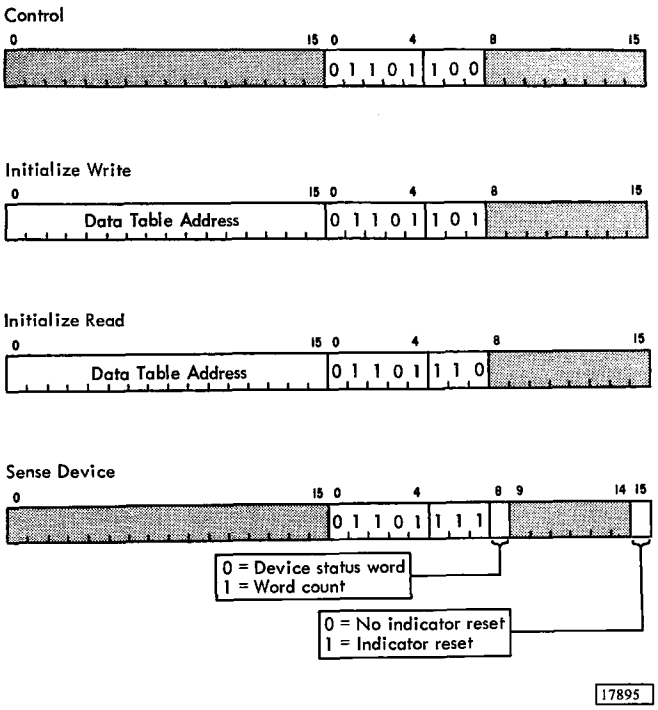


Figure 115. 1800 Commands (System/360 Adapter)

accumulator. The word read into the accumulator is specified by modifier bit 8 as described next.

SENSE DEVICE STATUS WORD: If modifier bit 8 is off in the XIO sense device, the adapter DSW is read into the accumulator. This should be the normal 1800 program response to an adapter interrupt and must be the complementary command response to a System/360 control command.

DSW bit positions 0 through 7 always contain the device status indicators. DSW bit positions 8 through 15 always reflect the contents of the low-order byte in the adapter buffer. The contents of the low-order byte in the adapter buffer vary depending on the conditions in the adapter as shown in Figure 116.

Modifier bit 15 is an XIO sense device controls reset of the program resettable indicators in the DSW. If modifier bit 15 is off when sensing the DSW, the indicators are not reset; if modifier bit 15 is on, the program resettable indicators are reset. Individual indicators in the DSW are described under "System/360 Adapter Device Status Word."

SENSE WORD COUNT: If modifier bit 8 is on in the XIO sense device, the current adapter word count is read into the accumulator. The word count appears in true binary form. After a reset, the word count is at the maximum value; that is, bit positions 2 through 15 are all on.

Initialize Read (1800)

The primary function of an XIO initialize read is transmission of data from the System/360 to the 1800. XIO initialize read is the complementary command to a System/360 write command. The adapter response to an XIO initialize read depends on the status of the adapter according to the following rules.

IDLE ADAPTER: An idle adapter accepts an XIO initialize write by saving the control word (area, function, and modifier), loading the adapter word count, and generating attention status to notify the System/360 of the pending operation. The adapter then waits until it receives the complementary System/360 command (write).

WAITING SYSTEM/360 WRITE: An adapter holding a previously accepted System/360 write command accepts an XIO initialize read by initiating data transfer, thus satisfying both commands. The data transfer operation continues until either of two events occurs: (1), the System/360 byte count for the write or 1800 word count for the XIO initialize read is decreased to 0, or (2) an error condition is detected. Termination of the operation is signaled to the 1800 by a transfer end interrupt. If the System/360 terminated the data transfer, the halt indicator will also be on in the DSW. Termination of the operation is signaled to the System/360 by channel end and device end.

BUSY ADAPTER: An XIO initialize read may be rejected because of either of the following adapter busy conditions:

Condition	High-Order Accumulator	Low-Order Accumulator
Adapter Idle	Device status	Undefined
System/360 has previously issued:		
Control, Read backward, Read, Write	Device status	Command byte
Halt I/O	Device status	Zero
Transfer of data	Device status	Data byte from low-order buffer byte
1800 has previously issued:		
XIO initialize read, XIO initialize write	Device status	IOCC modifiers

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Figure 116. Sense Data Presented to 1800 System

1. An XIO initialize read causes a command reject interrupt if given before the adapter has completed execution of a previous XIO from the 1800. The DSW will indicate command reject and 1800 command stored; 360 command stored will also be on if data transfer is in progress.
2. An XIO initialize read causes a command reject interrupt if given after the adapter has previously accepted any System/360 command, other than write. The DSW will indicate command reject and 360 command stored.

Initialize Write (1800)

The primary function of an XIO initialize write is transmission of data from the 1800 to the System/360. XIO initialize write is the complementary command to a System/360 read command. The adapter response to an XIO initialize write depends on the status of the adapter according to the following rules.

IDLE ADAPTER: An idle adapter accepts an XIO initialize write by saving the control word (area, function, and modifier), loading the adapter word count, and generating attention status to notify the System/360 of the pending operation. The adapter then waits until it receives the complementary System/360 command (read).

WAITING SYSTEM/360 READ: An adapter holding a previously accepted System/360 read command accepts an XIO initialize write by initiating data transfer, thus satisfying both commands. The data transfer operation continues until either of two events occurs: (1) the System/360 byte count for the read or 1800 word count for the XIO initialize write is decreased to 0, or (2) an error condition is detected. Termination of the operation is signaled to the 1800 by a transfer end interrupt. If the System/360 terminated the data transfer, the halt indicator will also be on in the DSW. Termination of the operation is signaled to the System/360 by channel end and device end.

BUSY ADAPTER: An XIO initialize write may be rejected because of either of the following adapter busy conditions:

1. An XIO initialize write causes a command reject interrupt if given before the adapter has completed execution of a previous XIO from the 1800. The DSW will indicate command reject and 1800 command stored; 360 command stored will also be on if data transfer is in progress.
2. An XIO initialize write causes a command reject interrupt if given after the adapter has previously accepted any System/360 command, other than read. The DSW will indicate command reject and 360 command stored.

Control (1800)

XIO control is used to cause an unconditional reset of the adapter. This reset causes immediate termination of adapter operations, and the adapter is not available to either system for the duration of the reset. If the System/360 is using the adapter when an XIO control is given, an interface control check may occur in the System/360.

If the 1800 system is reset by any means, the System/360 adapter goes off-line. The STOP button in the System/360 must be pressed to establish a WAIT condition before the System/360 adapter can get back on-line.

ADAPTER STATUS

System/360 Status Byte

The System/360 adapter presents the following status information to be included in the System/360 status byte:

Status Condition	Status Byte Bit Position
Attention	0
Busy	3
Channel end	4
Device end	5

Definitions of the remaining status indicators in the status byte are given in IBM System/360 Principles of Operation, Order No. GA22-6821. Figure 117 summarizes the status information presented to the System/360 during initial selection.

ATTENTION: Attention being on indicates that the adapter has accepted an XIO initialize read or XIO initialize write, but has not yet received the required complementary command from the System/360.

BUSY: Busy being on indicates that the adapter has been selected by the System/360 and that one of the following is also true: (1) an operation is pending, (2) a transfer is in progress, or (3) ending status has not yet been accepted by the System/360. Busy is off when the adapter is idle.

CHANNEL END: The adapter presents channel end to the System/360 during initial selection for control and no-operation commands, or with device end

360 Issues	Initial Status Presented			
	Idle	360 Control	1800 Read	1800 Write
Read or Read Backward	Zero	Busy and Device End*	Busy and Attention	Zero
Write	Zero		Zero	Busy and Attention
Control	Channel End		Busy and Attention	Busy and Attention
No-Operation	Channel End and Device End		Busy and Attention	Busy and Attention
Sense	Zero		Zero	Zero
Test I/O	Zero	Busy or Device End*	Attention	Attention
* Device End is conditional				

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Figure 117. System/360 Status Summary

during the ending sequence for all other commands.

DEVICE END: The adapter presents device end to the System/360 during initial selection for a no-operation command, after an XIO sense device from the 1800 in response to a control command, or with channel end at the end of data transfer for all other commands.

Adapter Device Status Word (1800)

Figure 118 shows the format of the adapter device status word (DSW) read into the accumulator by an XIO sense device with modifier bit 8 off. Interrupt indicators and program resettable indicators are also defined.

COMMAND REJECT: This indicator turns on, causing an interrupt, if the adapter rejects an 1800 XIO for any one of the following reasons:

1. The input/output control command referenced by the XIO has an invalid function code.
2. An XIO initialize read or XIO initialize write is given before a previous XIO initialize read or XIO initialize write is cleared.
3. An XIO initialize read is given after the adapter has accepted a read, read backward, or control command from the System/360.
4. An XIO initialize write is given after the adapter has accepted a write or control command from the System/360.

If command reject occurs while the adapter does not have an 1800 command stored, the adapter word count is reset to its maximum value. Such a reset can occur when transfer end has been generated but not yet accepted by the 1800.

1800 COMMAND STORED: This indicator turns on when the adapter accepts an XIO initialize read or XIO initialize write from the 1800, and remains on until reset by transfer end.

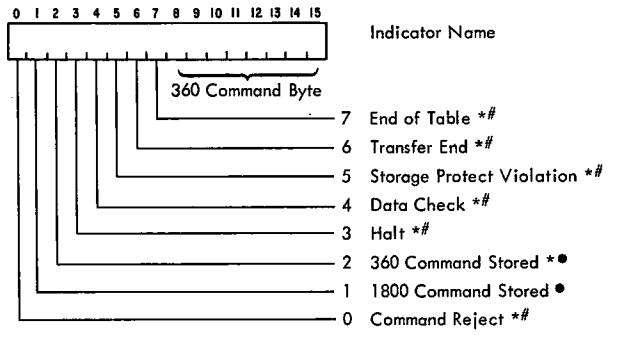
360 COMMAND STORED: This indicator turns on when the adapter accepts a read, read backward, write, or control command from the System/360.

If the command is read or write, this indicator causes an interrupt to the 1800 unless suppressed by the S-bit being on in the command byte or a complementary command from the 1800 waiting in the adapter. The interrupt condition can be reset by an XIO sense device with modifier bit 8 off and modifier bit 15 on. However, the 360 command stored indicator remains on until transfer end occurs.

If the command is read backward, the response is identical to a read command described in the preceding paragraph, except that the interrupt to the 1800 cannot be suppressed by the S-bit in the command byte.

If the command is control, the 360 command stored indicator causes an interrupt to the 1800. In this case, the indicator is reset by an XIO sense device with modifier bit 8 off and modifier bit 15 on.

The 360 command stored indicator can be on at the same time as transfer end. This indicates that the adapter has accepted a new command from the System/360.



* Interrupt

\# Indicator reset by an XIO sense device with reset

• Indicator reset by transfer end. 360 command stored reset by XIO sense device with reset if command is a control command

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Figure 118. System/360 Adapter Device Status Word

HALT: This bit turns on, causing an interrupt, if the System/360 terminates data transfer either with a normal stop or interface disconnect sequence. Transfer end will also be on.

DATA CHECK: This indicator turns on, causing an interrupt, if a parity error is detected during a data channel (cycle steal) operation or the adapter detects a System/360 bus out parity error.

If a parity error is detected while loading the word count via the data channel and the adapter does not have a complementary System/360 command, the adapter is reset and the 1800 can reinitialize the data transfer operation.

If a parity error is detected while loading the word count via the data channel and the adapter has a complementary System/360 command, or if a parity error is detected during any subsequent data channel operation, an immediate ending procedure is initiated. The adapter presents channel end and device end to the System/360, and data check along with transfer end to the 1800.

If a parity error is detected by the 1800 while an XIO is being initiated, the adapter ignores the operation and does not initiate an interrupt. This type of error causes an internal interrupt in the 1800.

STORAGE PROTECT VIOLATION: This indicator turns on, causing an interrupt, if an attempt is made to store data in a protected core storage location in the 1800. This could only occur during a System/360 write and XIO initialize read data transfer operation. Storage protect violation cause the adapter to initiate an ending procedure by presenting channel end and device end to the System/360, and storage protect violation along with transfer end to the 1800.

TRANSFER END: This indicator turns on, causing an interrupt, when any one of the following conditions occurs:

1. The 1800 word count is decreased to 0, and chaining is not specified.
2. The System/360 byte count is decreased to 0.
3. The System/360 issues a halt I/O or executes an interface disconnect sequence.
4. A parity error is detected.
5. A storage protect violation occurs.

Any XIO initialize read or XIO initialize write given while transfer end is on is rejected by the adapter.

END OF TABLE: Unless suppressed by the scan control bit in the 1800 word count, this indicator turns on when the word count is decreased to 0. The on condition causes an interrupt.

360 COMMAND BYTE: If the 360 command stored indicator is on and the 1800 command stored indicator is off, these DSW bit positions contain the System/360 command byte accepted by the adapter. These bits can be assumed to be 0 only after an adapter reset.

2790 Adapter

INTRODUCTION

The 2790 adapter provides the facilities that enable the 1801/1802 Processor-Controller to perform the system controller functions for an IBM 2790 Data Communications System. This 1800/2790 combination enables implementation of a two-way, in-house data communication and production reporting system. This system is capable of recording, processing, and analyzing information collected from many reporting stations located throughout an industrial complex.

The various components of the 2790 system provide the facilities for:

- Transaction selection.
- Key entry with visual display.
- Card or badge data entry.
- Time-of-day display.
- Visual output display.
- Operator guidance display.
- External alarm.
- Pulse counting.
- Printer output.
- Card or badge and rotary switch numeric data entry by means of unique data entry units.
- Attachment of digital OEM devices.

The devices that may be used at the various reporting stations include:

- IBM 2791 Area Station (Model 1 or 2).
- IBM 2793 Area Station.
- IBM 2795 Data Entry Unit.
- IBM 2796 Data Entry Unit.
- IBM 2797 Data Entry Unit.
- IBM 1035 Badge Reader.
- IBM 1053 Printer.

For additional information regarding the 2790 system components, refer to the IBM 2790 Data Communications System Component Description, Order No. GA27-3015.

Transmission Loop

Data communications are achieved over a two-wire transmission line that functionally appears as a two-wire loop, beginning and ending at the 2790 adapter. The area stations are connected in series with the transmission loop. As information is transmitted serially by the adapter, each area station, in sequence, has access to the information and may modify the information or return its own data. Since the transmission loop ends at the adapter, the modified information or area station data returns to the adapter for processing.

The transmission loop is divided into four segments (A, B, C, and D) to enhance installation reliability. Each segment has its own connections to the adapter. Information is normally passed from one segment to the next segment in the loop. However, any combination of segments may be bypassed under program control. When a segment is bypassed, the area stations and devices on the segment do not receive information from the loop and cannot transmit information to the loop. Any segment that becomes inoperable can be bypassed, thus allowing operation to continue on the other segments of the transmission loop.

The adapter divides transmission and processing of information to and from the transmission loop into 13 time periods called loop channels. Eight of these time-multiplexed loop channels operate at an effective data rate of approximately 100 characters per second; the other five loop channels operate at an effective data rate of approximately 20 characters per second. All 13 loop channels operate concurrently.

Configuration and Data Flow

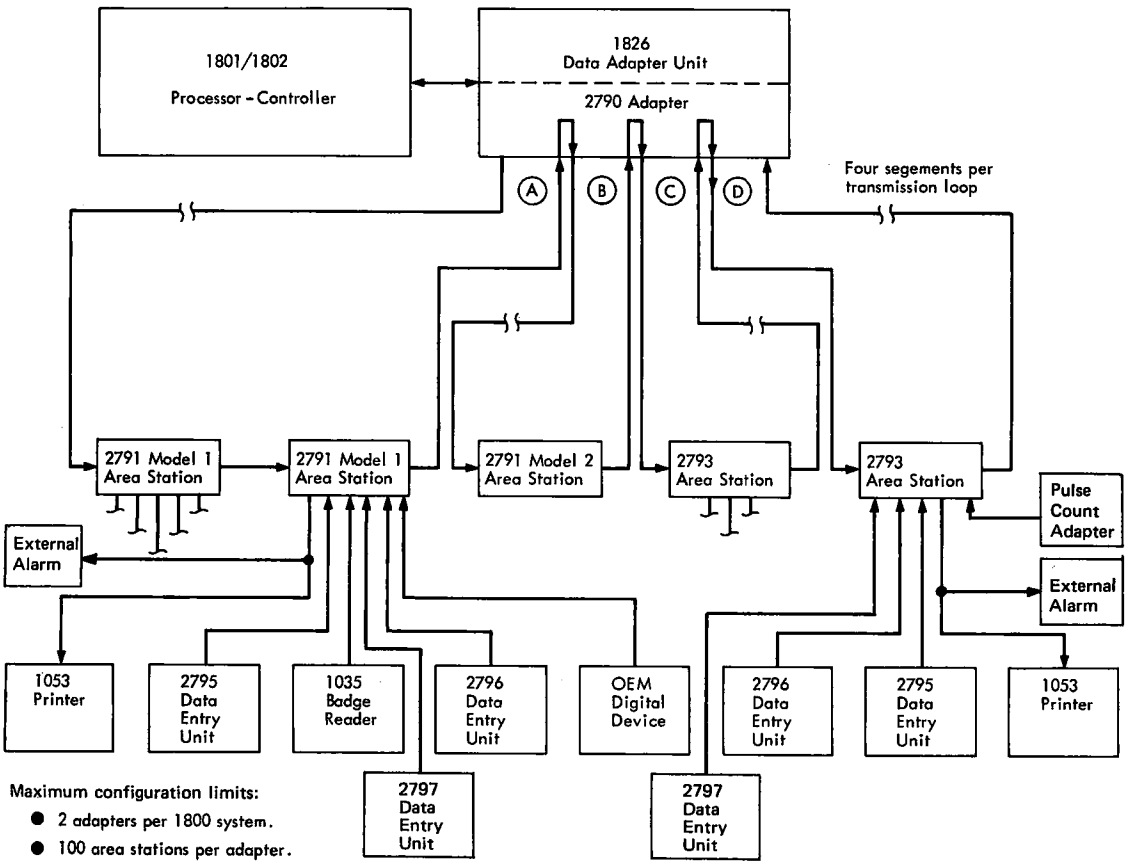
The adapter is housed in an IBM 1826 Data Adapter Unit (Model 2 or 3). Two adapters may be included in the 1800 system configuration. Each adapter requires a data channel for operation.

One adapter can control as many as 100 area stations and subsequently up to 1,024 data entry units.

The 1,024 data entry units may be assigned to area stations as desired up to a total of 32 per area station. In addition, IBM 1035 Badge Readers (remotely located), IBM 1053 Printers, and digital OEM devices can be included in the system configuration. Figure 119 summarizes the system configuration and illustrates basic data flow.

Data Transfer Concept

Although the adapter uses a data channel, overall data transfer concepts are different from other devices on the 1800 system that use data channels. After being initialized, other devices implement data transfer to or from a data table in core storage



Maximum configuration limits:

- 2 adapters per 1800 system.
- 100 area stations per adapter.
- 1,024 data entry units per adapter.
- 32 data entry units per 2791 Area Station Model 1 or 2793 Area Station.
- Three 1035 Badge Readers per 2791 Area Station Model 1.
- One 1053 Printer per 2791 Area Station Model 1 or 2793 Area Station.
- 63 Contact Sense Counters per 2793 AS. (Pulse Count Adapter feature).
- 1 External Alarm Contact per 1053 attachment.
- 1,000 feet of two-wire communications line (No.22 AWG twisted pair) between data entry units and area stations.
- 1,000 feet of two-wire communications line (No.22 AWG twisted pair) between area stations, and between area stations and the 2790 adapter.
- 2790 Extended Distance Repeater (EDR) features can be applied between area stations, but EDR is not available for installation in an 1826.

(See IBM 2790 Data Communications System Installation Manual—Physical Planning, Order No. GA27-3017 for distances with other wire sizes or for information on EDR features.

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Figure 119. 1800/2790 Configuration

via data channel operations as required. The 2790 adapter uses the data channel for control purposes, as well as data transfer, by communicating with a control table in core storage.

The control table contains one 16-word loop channel control block (LCCB) for each of the 13 loop channels, and one loop channel interrupt block (LCIB). The LCCB's contain control and status information while the LCIB contains interrupt status for all 13 loop channels. Detailed descriptions of these control blocks are found under "Loop Channel Control Block" and "Loop Channel Interrupt Block."

To implement data transfer, the program initializes the LCCB for the particular channel by specifying the type of operation (read or write), the core storage address of the table containing the data, and the number of bytes of data. The program activates the channel by turning on a control bit in the LCCB. The adapter then performs the data transfer operation on the active channel, using data channel operations to communicate with the LCCB. The program is released for other processing.

During a write operation, the adapter uses the data buffer address and byte count in the LCCB to fetch data (one byte at a time) from the data buffer for subsequent transmission to a device on the transmission loop. Once initiated, a write operation continues until the byte count is decreased to 0, or an error occurs.

During a read operation, the adapter uses the data buffer address and byte count in the LCCB to store incoming data in the data buffer (one byte at a time). Normally, a read operation is terminated by a request from the input device. However, a read operation is also terminated if the byte count is decreased to 0, or an error occurs.

LOOP CHANNELS

Each adapter cycle, used in transferring information around the transmission loop, is divided into nine basic time periods of equal duration. The adapter utilizes these nine time periods to implement a channel concept for data transfer.

High-Speed Loop Channels

The first eight time periods of an adapter cycle are used as loop channels 1 through 8 and are known as high-speed loop channels. Each of these eight loop channels has an effective data rate of approximately 100 characters per second. All eight high-speed channels are sequentially selected for service during each adapter cycle.

Low-Speed Loop Channels

The ninth time period of an adapter cycle is used to accommodate five additional loop channels (9 through 13). This is accomplished by sequentially selecting each of the five loop channels (9 through 13) for service during the ninth time period in five consecutive adapter cycles. During the first cycle, for example, channels 1 through 9 are serviced; during the next cycle, channels 1 through 8 and 10 are serviced. This sequence continues until channel 13 is serviced, and is then repeated.

Because each one of channels 9 through 13 is selected only once during each five adapter cycles, the effective data rate for these five channels is approximately 20 characters per second. Therefore, channels 9 through 13 are known as low-speed loop channels.

Both high- and low-speed channels may be used for read and write operations. However the data rate of the input or output device must be considered during an operation. For example, printer output to the 1053 Printer must be transmitted via a low-speed channel and the card reader or DEU input must be transmitted via a high-speed channel.

Data Transmission Format

Information is transmitted serially by bit around the transmission loop at an approximate rate of 514 kHz as long as the adapter is in active mode. The information bits are segregated into bytes containing eight bits plus parity. During each channel time frame, a sequence of 30 bytes (called a channel frame) is transmitted to the loop. The first byte (byte 0) in a channel frame always contains a start character. If the channel is inactive, the remaining 29 bytes contain sync characters. If the channel is active, bytes 1 through 4 are used to carry information, and the remaining bytes (5 through 29) contain sync characters.

The channel frame format and its relationship to sequential channel transmission are shown in Figure 120. Each byte except the start byte should contain odd parity. The information bytes of the active channel frame are described in the following paragraphs.

START BYTE: The start byte (byte 0) is the first byte transmitted in a channel frame and always contains a start character (/39 with even parity). The start character is automatically generated by the adapter at the beginning of each channel frame. The start byte is used to indicate start of frame and to maintain byte synchronization.

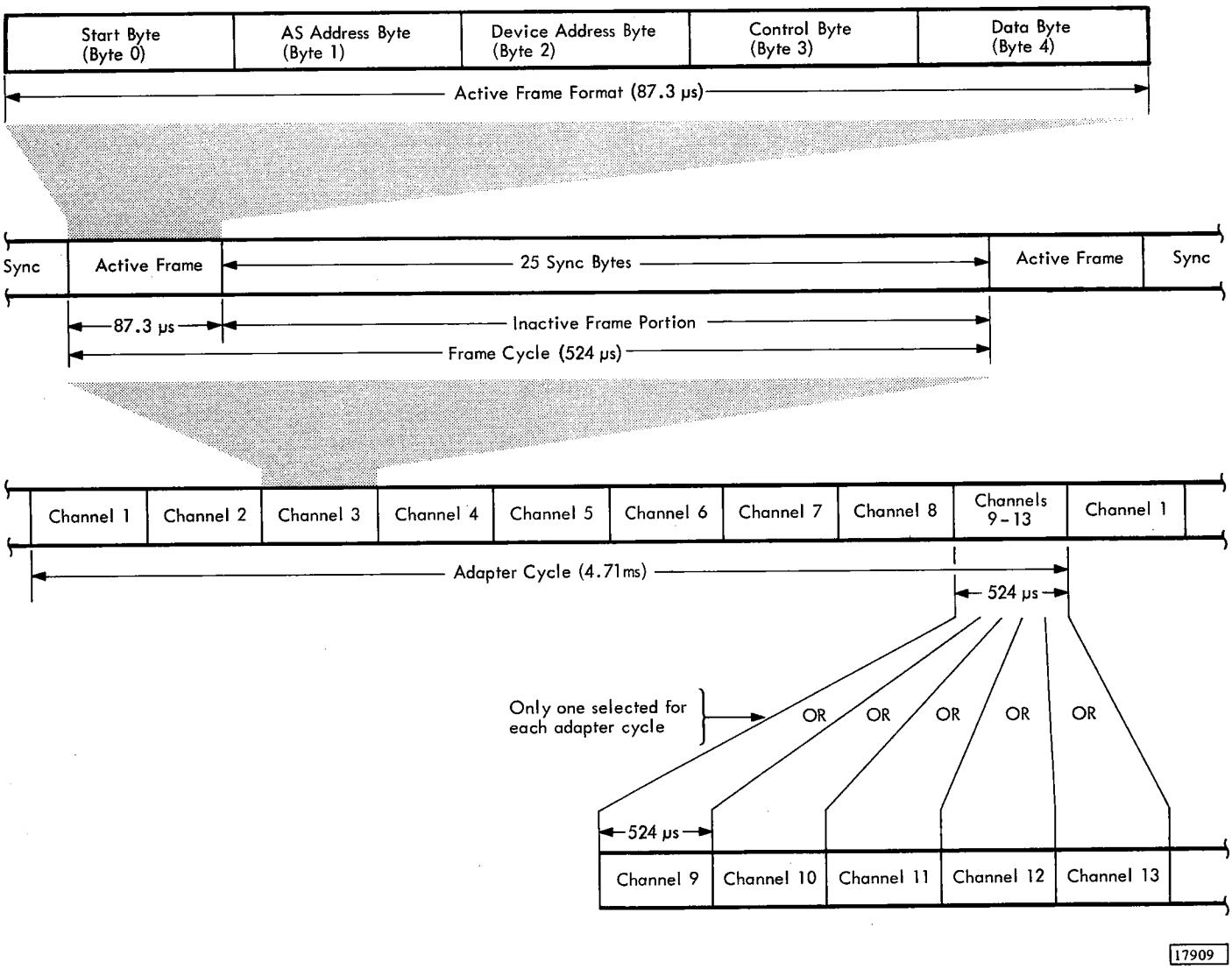

Figure 120. Data Transmission Format

AS ADDRESS BYTE: The AS (area station) address byte (byte 1) is the second byte transmitted in the channel frame if the channel is active. This byte is used to carry an AS address code which selects the area station(s) to receive the channel frame. (See "Area Station Addressing" for details.)

DEVICE ADDRESS BYTE: The device address byte (byte 2) is the third byte transmitted in the channel frame if the channel is active. This byte is used to carry the device address code, which specifies a particular device controlled by the selected area station. (See "Device Addressing" for details.)

CONTROL BYTE: The control byte (byte 3) is the fourth byte transmitted in the channel frame if the channel is active. This byte is divided into two hexadecimal digits for information transfer. The low-order hexadecimal digit (bit positions 4 through 7) is used to carry a command code to the selected area station (AS) and device. The high-order hexadecimal digit (bit positions 0 through 3) is used to carry the AS or device response to the command back to the adapter.

DATA BYTE: The data byte (byte 4) is the fifth byte transmitted in the channel frame if the channel is

active. This byte is used as the data carrier for the channel frame. The data byte may contain a data character, a guidance character (AS local I/O only), or the status of the AS or device. The contents of the data byte depends on the command and the AS or device response to the command. (Refer to "Commands and Responses" for details.)

AREA STATION ADDRESSING

The adapter uses an area station (AS) addressing scheme that allows each loop channel to:

1. Communicate with an individual AS.
2. Communicate with all area stations.
3. Poll all area stations, thus enabling any area station to request data transfer.

To accomplish this, three types of AS address codes are used, as described in the following paragraphs.

Discrete AS Address

Each AS is assigned a discrete address during installation. This address is the means by which communication is directed to a specific AS. Area stations may be assigned any address within the range of /80 to /FF. All other codes are invalid.

> Note: If the MPX Operating System is being used, IBM recommends that area stations be assigned sequential addresses. This address assignment sequence does not restrict physical placement of the area stations around the loop.

Every channel frame transmitted to a specific AS has the discrete AS address in the AS address byte. Any time an AS receives a channel frame with its address, it replaces the address received in the AS address byte with its assigned address. This address replacement provides the ability to detect an AS that is responding to an address other than its own.

All AS Address

The all-AS-address code is /09. This address code is used to enable transmission of data to all area stations via a single loop channel. This mode of operation is known as broadcast mode. When an AS receives a channel frame with the all-AS-address code, the complete channel frame is passed on unmodified and, if possible, the AS performs the function specified by the control byte.

Any AS Address

The any-AS-address code is /11. This address code is used to poll the area stations on the loop for service requests. When an AS requiring service receives a channel frame with the any-AS-address code, it replaces the any-AS-address code received in the AS address byte with its assigned address. Thus, the AS address returning to the adapter is the address of the requesting AS. This replacement captures the loop channel for a data transfer operation. While captured, the discrete address of the requesting AS is placed in the AS address byte of each channel frame transmitted for the captured channel. The channel remains captured until it is deactivated during an ending sequence.

DEVICE ADDRESSING

Each device controlled by an AS is preassigned a specific device address as follows:

Diagnostic controls	/00
Pulse Count Adapter	/01 through /3F
1053 Printer	/40
AS badge reader (read operation)	/80
AS display (write operation)	/80
1035 Badge Reader	/81 through /83
AS card reader	/84
AS keyboard	/88
AS OEM digital service	/8C
Data entry units	/C0 through /DF

Note that the AS badge reader and display have the same address. In this case, the type of operation (read or write) determines which device is selected. Diagnostic controls are usually addressed by /00. However, a diagnostic command is executed regardless of the device address specified. The test pulse counter device address is also /00. The diagnostic or pulse counter operation is determined by the code in the command byte of the frame.

Any channel frame addressed to a specific AS is also addressed to a particular device. When an AS is selected by a channel frame, the device address byte is used to select the particular device. (The external alarm feature uses a character in the 1053 character set, and is addressed by selecting the 1053 adapters device address.) The preassigned address of the selected device then replaces the

device address received in the channel frame. When an AS captures a channel frame containing an any-AS-address code, the preassigned address of the device requesting service is placed in the device address byte. Thus, the channel frame returning to the adapter contains the AS address and the address of the device requesting service. This device address replacement provides the ability to detect a device that is responding to an address other than its own.

COMMANDS AND RESPONSES

Area stations are basically controlled on a command-response basis; that is, for each command transmitted by the adapter, the area station accepting the command acknowledges by returning a response to the adapter.

The command and response codes appear as two hexadecimal digits in the control byte of each channel frame. The command digit is located in bit positions 4 through 7 of the control byte, and the response digit is located in bit positions 0 through 3 of the control byte. The control byte transmitted by the adapter always contains some command code digit and a response digit of /0. When the area station accepts the command, it inserts the proper response code into the response digit for return to the adapter. Therefore, a control byte containing a /0 response digit is considered to be a command, whereas a control byte containing any other response digit is considered to be a response.

Figure 121 shows the various area station (AS) commands and responses. There are several commands in each of three major categories -- read, write, and control. One or more valid AS responses are possible with each of these commands.

Read Commands

READ: This command (/06) is generated by the adapter and transmitted to any AS returning a read request response to a previous read null command. A read command may also be generated by the program to read out a particular pulse count adapter counter. In either case, a read command places the device designated by the device address byte in data mode and allows the device to begin reading its data source. The only valid response is read command acknowledge.

If the read command is sent to a pulse count adapter that is performing a previous read or write command, busy status (/80) is returned with read command acknowledge.

READ NULL: This command (/02) transmitted in a channel frame indicates to the AS that the channel is available for any read-type request. Read null may be generated by the program and used as the first command transmitted when activating a channel. This dedicates the channel to a read operation. The channel remains dedicated until a read end request is received from a device using the channel for a read operation.

After a channel is dedicated to a read operation, but before the channel is captured by an AS, the read null command and any AS address code initially set up by the program are transmitted by the adapter in each channel frame for the channel. After the

Code Name	Hex	Bit Pattern	
		Response 0123	Command 4567
Read Commands			
Read	06	0000	0110
Read Null	02	0000	0010
Read Data	0A	0000	1010
Read End	0E	0000	1110
Read Responses			
Read Request	12	0001	0010
Read Cmd Acknowledge	46	0100	0110
Read Data Request	62	0110	0010
Read Data Acknowledge	6A	0110	1010
Read End Request	72	0111	0010
Read End Acknowledge	3E	0011	1110
Read Null Acknowledge	42	0100	0010
Write Commands			
Write	05	0000	0101
Write Null	01	0000	0001
Write Data	09	0000	1001
Write End	0D	0000	1101
Write Responses			
Write Data Request	51	0101	0001
Write Data Acknowledge	69	0110	1001
Write End Request	71	0111	0001
Write End Acknowledge	3D	0011	1101
Write Null Acknowledge	41	0100	0001
Write Cmd Acknowledge	45	0100	0101
Control Commands			
Bypass	0B	0000	1011
Restore	03	0000	0011
Send Sync	04	0000	0100
Begin Diagnostic	08	0000	1000
End Diagnostic	0C	0000	1100
Control Responses			
Bypass Acknowledge	6B	0110	1011
Restore Acknowledge	63	0110	0011
Response to Send Sync Cmd	47	0100	0111
Begin Diagnostic Acknowledge	68	0110	1000
End Diagnostic Acknowledge	4C	0100	1100

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Figure 121. Commands and Response Codes

channel is captured by an AS, the adapter automatically generates a read null command, for transmission to the AS, whenever no other command is required.

Read null has four valid responses: read null acknowledge, read request, read data request, and read end request. A read data request in response to a read null is accompanied by a data character in the data byte of the channel frame. This is the first transmission of the data character. A second transmission of the same character occurs in response to a subsequent read data command. The two data characters are compared for validity, bit by bit.

READ DATA: This command (/0A) is automatically generated by the adapter and transmitted to any AS returning a read data request response to a previous read null command. Read data causes the data character previously transmitted with read data request to be retransmitted with read data acknowledge response to the command. This allows the adapter to perform a validity check on the transmitted character. Read data also releases the device so it can accept the next character from its data source.

The only valid response to read data is read data acknowledge.

READ END: This command (/0E) removes the addressed device from data mode, thus terminating the operation is progress. Read end is generated by the program as a result of receiving a read end request from the AS or as a result of detecting an error that requires termination of the read operation. The AS interrogates the channel frame data byte for a new guidance character (AS local I/O only) or terminating status. Therefore, the program should ensure that the proper guidance or status is transmitted with read end. (See "Guidance Characters" and "Status Characters" for details.)

If the data byte contains terminating status, the addressed device OR's its status, along with bit positions 0 and 1 of the status received, back into the returning data byte. The device also inserts its diagnostic mode status in bit position 3 of the returning data byte. Because the adapter compares the transmitted data byte with the returning data byte for validity, terminating status sent with a read end command must reflect the device status received (if other than /00) with the read end request. For example, terminating status of /80 and device status of /40 results in a returning status of /C0. This status results in a data check. However, terminating status indicating a bad end (/40, /80, or /C0) may be sent by the program if the device status indicates normal end (/00). In this case, no data check occurs. Device status received with read end request is automatically transmitted with the subsequent read end unless it is modified by the program before activating the channel for the read end. This automatic status transmission occurs only if the channel used to transmit read end is the same channel over which read end request was received.

The only valid response to read end is read end acknowledge.

To maintain count integrity, the response to a pulse counter read end request must be as fast as possible. The reason is the way additional counts during the read are handled. These counts are inhibited from updating the counter being read and are stored in a three-count hold buffer. The read end command must be received at the AS before the fourth increment to that counter, or the count will be lost. For example, a counter counting at the maximum rate of 30 counts per second must receive the read end command within 96 ms after the read command started the operation.

Read Responses

READ REQUEST: This response (/12) is returned by any AS that captures a channel frame containing (1) a read null in the command byte, and (2) the any-AS-address code in the AS address byte. Read request indicates that a device controlled by the AS has data to be transferred to the 1800 and needs the captured channel to implement data transfer. The AS inserts the address of the device requesting service in the device address byte of the channel frame.

To initiate data transfer after receiving a read request, the adapter automatically generates and transmits a read command to the requesting AS and device.

READ COMMAND ACKNOWLEDGE: This response (/46) is returned by an AS in response to a read command. Read command acknowledge indicates that the AS has received the read command and has initiated a read operation at the addressed device.

READ DATA REQUEST: This response (/62) is returned by the AS in response to a read null when the device specified by the channel frame device address byte has a data character ready for transfer to the 1800. When an AS returns read data request, it also inserts the data character from the device into the returning channel frame data byte. This is the first of two transmissions of the data character; the second occurs with read data acknowledge.

Read data request causes the adapter to automatically generate and transmit a read data command to the requesting device.

READ DATA ACKNOWLEDGE: This response (/6A) is returned by the AS in response to a read data command. When the AS returns read data acknowledge, it also inserts the data character from the addressed device into the returning channel frame data byte. This is the second transmission of this data character; the first occurs with read data request. The adapter compares the received data characters for validity.

READ END REQUEST: This response (/72) is returned by the AS in response to read null when the device has determined that data transfer has come to normal completion or when the device has detected an error condition. The status of the operation is returned in the data byte of the channel frame. An all-0 status byte indicates normal end.

Read end request causes the adapter to deactivate the channel and generate a channel interrupt to the program. The interrupting condition is posted in the channel sense word.

Normal program response to a read end request is read end command.

READ END ACKNOWLEDGE: This response (/3E) is returned by the AS in response to a read end command. It indicates that the device will terminate the operation according to the guidance/status returned in the data byte of the channel frame. The adapter compares the returning data byte with the one transmitted to ensure that the operation was terminated according to the status transmitted or that the guidance character was transmitted correctly around the transmission loop.

The program may have previously assigned a new data buffer to the channel over which read end and read end acknowledge are transmitted. In that case, the adapter automatically rededicates the channel to another read operation. It does so by generating read null and any-AS-address codes and transmitting them in the next channel frame for that channel.

If, on the other hand, a new data buffer was not previously assigned to the channel, the adapter generates another channel interrupt to the program and deactivates the channel.

READ NULL ACKNOWLEDGE: This response (/42) is returned by the AS in response to read null if the addressed device is in data mode, but does not currently have a character ready for transfer to the 1800. Read null acknowledge causes the adapter to retransmit the read null command and to increase the channel timer count.

Write Commands

Write commands are used to transfer data from the 1800 to a specific 1053 Printer, a specific pulse counter, a specific AS display, or to all AS displays using broadcast mode (all-AS-address code). When using broadcast mode, no AS responses are returned for any write-type commands.

WRITE: This command (/05) is generated by the program and used to initiate a write operation. If the write command is to a specific AS display or 1053, the only valid response is write command acknowledge. In broadcast mode, the valid response is the write command itself and the all-AS-address code.

If a specific AS display or pulse counter is addressed and it is busy, a /80 status character is returned in the channel frame data byte associated with write command acknowledge. This status causes the adapter to increase the channel timer count by 1 and retransmit the write command. This exchange continues until all-0 status is returned with write command acknowledge, or until the channel timer count reaches overflow condition (count of 32, 768).

If a 1053 is addressed and is unable to perform a print operation (out of paper), it returns a write end request in response to the next command -- a write null command.

WRITE NULL: This command (/01) transmitted in a channel frame indicates that the channel is available for any write-type request from the device specified in the device address byte. Write null is automatically generated and transmitted by the adapter if no other command is required, provided the channel is in an active write sequence.

A write null to the 1053 Printer causes printing to occur if a character was previously sent to the 1053 with a write data command.

The three valid responses to write null are: write null acknowledge, write data request, or write end request.

WRITE DATA: This command (/09) is automatically generated and transmitted by the adapter under the following two conditions:

1. A write data request is returned in response to a previous write null. In this case, the only valid response is write data acknowledge.
2. An unmodified write command is returned to the adapter, and the AS address byte indicates broadcast mode (all-AS-address code). In this case, the response is the unmodified command itself and the all-AS-address code.

Write data is always accompanied by a data character in the channel frame data byte. The returning data byte is compared with the transmitted data byte for validity.

WRITE END: This command (/0D) removes the addressed device from data mode, thus terminating the write operation. Write end is automatically generated and transmitted by the adapter under the following three conditions:

1. A write data request is received in response to a previous write null and the byte count is 0 (data transfer complete). Write end acknowledge is the valid response to write end generated in this manner. The data byte associated with write end will contain terminating status of /00 (normal end).
2. A write end request is received in response to a previous write null. The data byte associated with write end generated in this manner will contain the same status as received with write end request. Write end acknowledge is the valid response.
3. An unmodified write data command is returned to the adapter, the AS address indicates broadcast mode (all-AS-address code), and the byte count is 0. The data byte associated with write end generated in this manner will contain terminating status of /00 (normal end). The only valid response to a write end command generated in this manner is the write end command itself and the all-AS-address code.

Write Responses

Area stations do not return responses to write-type commands if the AS address byte of a channel frame indicates broadcast mode (all-AS-address code). When addressed to a specific area station, this response of /0X will cause a control check; however, the adapter automatically detects broadcast mode from the AS address and generates the proper command to continue the broadcast write operation.

The following write responses are those returned when not using broadcast mode of operation.

WRITE DATA REQUEST: This response (/51) is returned in response to write null if the addressed device is ready to receive another data character.

WRITE DATA ACKNOWLEDGE: This response (/69) is returned in response to write data and indicates that the addressed device received the data character associated with the write data command. The data byte is returned unmodified with write data acknowledge. The adapter checks the returning data byte with the transmitted one for validity.

WRITE END REQUEST: This response (/71) is returned in response to write null if the addressed device has detected an abnormal condition that requires termination of the operation. The data byte returned with write end request reflects the status of the device.

WRITE END ACKNOWLEDGE: This response (/3D) is returned in response to write end. The data byte returned with write end acknowledge reflects the status under which the operation was terminated and is compared for validity with the status transmitted with write end.

Receipt of write end acknowledge causes the adapter to deactivate the channel and generate a channel interrupt to the program.

WRITE NULL ACKNOWLEDGE: This response (/41) is returned by an AS in response to write null if the addressed device is in data mode but does not currently require another character from the 1800. Write null acknowledge causes the adapter to retransmit read null and increase the channel timer count by 1.

WRITE COMMAND ACKNOWLEDGE: This response (/45) is returned in response to write command. It indicates that the addressed device has received the command.

If a specific AS display or pulse counter is addressed by the write command, the data byte returning with write command acknowledge contains the current status of the AS display. All-0 status indicates the write operation can be executed; nonzero status (/80) indicates busy and the write operation cannot be performed. Receipt of busy status causes the adapter to increase the channel timer count by 1 and retransmit the write command. This sequence continues until all-0 status is returned, or until the channel timer count reaches overflow condition (count of 32,768).

If a 1053 Printer is addressed by the write command, the data byte returned with write command acknowledge does not contain status. If the 1053 is unable to perform the write operation, it returns write end request and its status in response to the next command -- a write null.

Control Commands

Control commands are provided to permit program control of AS diagnostic functions. The adapter does not automatically process returning control command channel frames as it does in a read or write sequence. Therefore, the program must turn on the unconditional interrupt bit in word 2 of the loop channel control block prior to activating a channel to send a control command. The unconditional interrupt bit causes the adapter to store the returning control command channel frame in words 6 and 7 of the loop channel control block for that channel. Processing of the returning information (correct response, status, and so on) must then be accomplished by the program.

Control commands can be sent using broadcast mode (all-AS-address code). However, the area stations do not return any control responses in broadcast mode.

BYPASS: This command (/0B) must be generated by the program. It causes the AS selected by the AS address byte to enter bypass mode after processing the data byte (byte 4) of the channel frame. This bypass eliminates the sync character following the channel frame data byte. Therefore, the frame returning to the adapter has only 29 bytes. However, the start character in the following channel frame allows the adapter to regain frame synchronization.

While bypassed, the AS still monitors information received from the transmission line, but it cannot respond or insert information. A broadcast mode write operation can still be performed because the AS is not required to respond during this operation. The only other command that is accepted by an AS in bypassed state is a restore command.

Bypass acknowledge is the valid response to a bypass command. The bypass command is returned unmodified if the AS is already in bypassed state.

RESTORE: This command (/03) must be generated by the program. It causes the addressed AS to be restored from bypassed state after the restore control byte has been processed. This restore causes a second control byte, containing the restore command digit and the AS response digit, to be returned to the adapter. The first control byte contains only the restore command digit. The data byte now contains the second control byte in the returning channel frame. Because a byte was added to the channel frame, a skip character (/00) is returned in the byte following the second control byte (byte 5). This character allows the adapter to skip that byte and regain frame synchronization.

An AS not bypassed responds to a restore command with bypass acknowledge in the normal manner. The difference between the two responses enables the program to determine whether or not the AS was previously bypassed and if the restore function was actually performed.

SEND SYNC: This command (/04) must be generated by the program. It affects AS operation only in diagnostic mode. Once an AS is in diagnostic mode, a send sync command causes the AS to begin sending a continuous stream of sync characters. The AS continues to send sync characters until it receives at least two /FF characters in succession. This can be achieved by transmitting a channel frame with /FF in the AS and device address bytes. The only response to send sync is the continuous stream of sync characters.

Send sync allows the selected AS to transmit sync characters without transmitting what it is receiving. This type of transmission provides the ability to detect intermittent transmission line failures between two consecutive area stations.

When send sync is being used, active channel frames returning to the adapter must be checked with the program (UI bit on for all active channels). Sync character transmission during bytes 5 through 29 of an active channel frame or bytes 1 through 29 of an inactive channel frame can be checked by monitoring the sync fill error indicator in the adapter device status word 1.

BEGIN DIAGNOSTIC: This command (/08) must be generated by the program. It causes the addressed AS to enter diagnostic mode, While in diagnostic mode, the AS responds only to commands addressed to it. Begin diagnostic acknowledge is the valid response to this command.

END DIAGNOSTIC: This command (/0C) must be generated by the program. It causes the addressed AS to return to normal mode. End diagnostic acknowledge is the valid response to this command.

Control Responses

The following are AS responses that are returned when the control commands are not transmitted in broadcast mode.

BYPASS ACKNOWLEDGE: This response (/6B) is returned in response to bypass command. It indicates that the AS executed the command.

RESTORE ACKNOWLEDGE: This response (/63) is returned in response to restore command. If the AS was in bypassed state, the response is located in the data byte location of the channel frame. The control byte contains only the restore command. If the AS was not in bypassed state, the response is located in the control byte.

BEGIN DIAGNOSTIC ACKNOWLEDGE: This response (/68) is returned in response to begin diagnostic. It indicates that the AS entered diagnostic mode.

END DIAGNOSTIC ACKNOWLEDGE: This response (/4C) is returned in response to end diagnostic. It indicates that the AS has returned to normal mode.

ADAPTER CONTROL TABLE

The 2790 adapter utilizes a 224-word control table in core storage to communicate with the program, implement data transfer, and maintain control and status information. The control table can be located anywhere in core storage, but must be located on a 256-word boundary. Before an execute I/O (XIO) is issued to activate the adapter, the control table must be initialized by the program. Once initialized, the control table is assigned to the adapter by placing the control table address (256-word boundary) into bit positions 0 through 7 of the XIO control (start loop) address word used to activate the adapter. The control table address is saved in the adapter table address register and used in all subsequent communication with the table.

The control table is divided into 14 blocks of 16 words each. The first block contains the interrupt indicators for the 13 loop channels and is called the loop channel interrupt block (LCIB). The remaining 13 blocks are assigned to loop channels 1 through 13, respectively. Each of these blocks is called a loop channel control block (LCCB). Figure 122 illustrates the format of the adapter control table and the various blocks within the table.

When the adapter is communicating with the control table, the contents of the table address register are used as the two high-order hexadecimal digits of the core storage address. These digits select the 256-word boundary at which the control table begins. The third hexadecimal digit of the address is generated by the adapter and reflects the loop channel number currently being serviced. This digit selects a

Control Table Contents			Core Address In Hex *
LCIB		(16 words)	XX00 ↑ 0F
LCCB	Channel 1	(16 words)	10 ↓ 1F
LCCB	Channel 2	(16 words)	20 ↓ 2F
LCCB	Channel 3	(16 words)	30 ↓ 3F
LCCB	Channel 4	(16 words)	40 ↓ 4F
LCCB	Channel 5	(16 words)	50 ↓ 5F
LCCB	Channel 6	(16 words)	60 ↓ 6F
LCCB	Channel 7	(16 words)	70 ↓ 7F
LCCB	Channel 8	(16 words)	80 ↓ 8F
LCCB	Channel 9	(16 words)	90 ↓ 9F
LCCB	Channel 10	(16 words)	A0 ↓ AF
LCCB	Channel 11	(16 words)	B0 ↓ BF
LCCB	Channel 12	(16 words)	C0 ↓ CF
LCCB	Channel 13	(16 words)	D0 ↓ XXDF

* Hex XX00 is loaded into table address register to set the 2790 adapter on a 256-word boundary. XX = any valid hex character.

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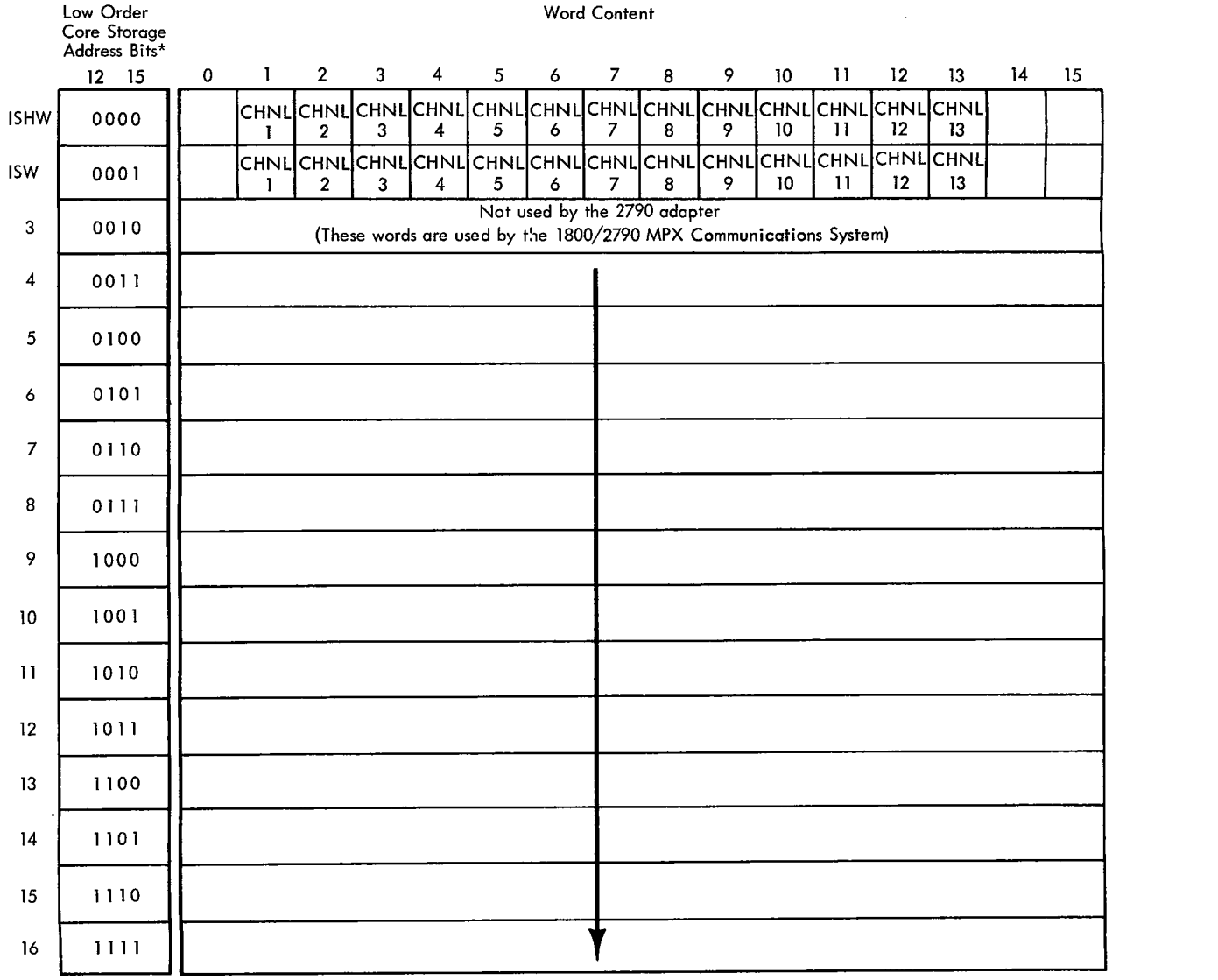
Figure 122. 2790 Adapter Control Table Format

specific 16-word block within the control table. The fourth (low-order) hexadecimal digit of the address is also generated by the adapter; it selects the specific word within the 16-word block.

Communication between the control table and adapter is performed by means of data channel (cycle steal) operations. The adapter communicates with the control table only while in active mode; that is, after being activated by an XIO control (start loop). While active, the adapter communicates with each of the LCCB's to determine what action, if any, is required as each of the loop channels is sequentially serviced by the adapter. While inactive, the adapter does not communicate with the control table, Thus, no interrupts or data channel operations occur.

Loop Channel Interrupt Block

The loop channel interrupt block (LCIB) is the first block in the adapter control table. It is used to stack channel interrupts and to store channel interrupt status for program interrogation. The LCIB format is shown in Figure 123.



* Address bits 0 through 7 reflect 256-word boundary table address.
Address bits 8 through 11 must be 0's.

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Figure 123. Loop Channel Interrupt Block Format

Only the first 2 words of the block are used by the adapter; the remaining 14 words are not used by the adapter, but are used by the 1800/2790 MPX Communications System. The words used by the adapter are described in the following paragraphs.

Interrupt Status Hold Word

The interrupt status hold word (ISHW) is used by the adapter to stack channel interrupt status. This is accomplished by storing an interrupt indicator for those channels requesting an interrupt while the program is servicing previous channel interrupts. ISHW bit positions 1 through 13 are turned on to reflect interrupt requests from channels 1 through 13, respectively. After the program has finished servicing previous channel interrupts, it issues an XIO sense device with modifier bit 15 on (reset). If any channel interrupts have been stacked in the ISHW, they are transferred to the interrupt status word (ISW), and another interrupt to the program is generated.

The first channel interrupt request to be stacked and stored in the ISHW always causes the ISHW to be cleared when stacking is initiated. Therefore, the program need not clear the ISHW.

Interrupt Status Word

The interrupt status word (ISW) is used to store the channel interrupt indicators for those channels requesting interrupts at the time the adapter generates a channel interrupt to the program. Once the program interrupt is generated, the contents of the ISW remain unchanged until after the adapter is given an XIO sense device with modifier bit 15 on (reset). Thus the program has time to interrogate the ISW to determine which channels to service during the program interrupt. ISW bit positions 1 through 13 reflect interrupt request status from channels 1 through 13, respectively.

The ISW is automatically cleared when new channel interrupt indicators are stored or transferred to it from the ISHW. Therefore, the program need not clear the ISW.

Loop Channel Control Block

The adapter control table contains 13 loop channel control blocks (LCCB's), one associated with each of the 13 channels. Each LCCB contains the status of the associated channel as well as the information required by the adapter to transmit channel frames and to process returning channel frames for the channel. The LCCB is also the means by which information relative to the specific channel is transferred between the adapter and program.

The LCCB format is shown in Figure 124. Only the first eight words of each LCCB are used by the adapter; the remaining words are not used by the adapter, but are used by the 1800/2790 MPX Communications System. The words used by the adapter are described in the following paragraphs.

LCCB Address Word (Active Frame)

This is the first word in the LCCB. It contains area station (AS) and device address information. If the adapter is active, the address word is transferred to the adapter each time either of two events occurs: (1) the assigned channel is sequentially selected for channel frame transmission to the loop, or (2) that channel is selected for processing of a channel frame returning from the loop.

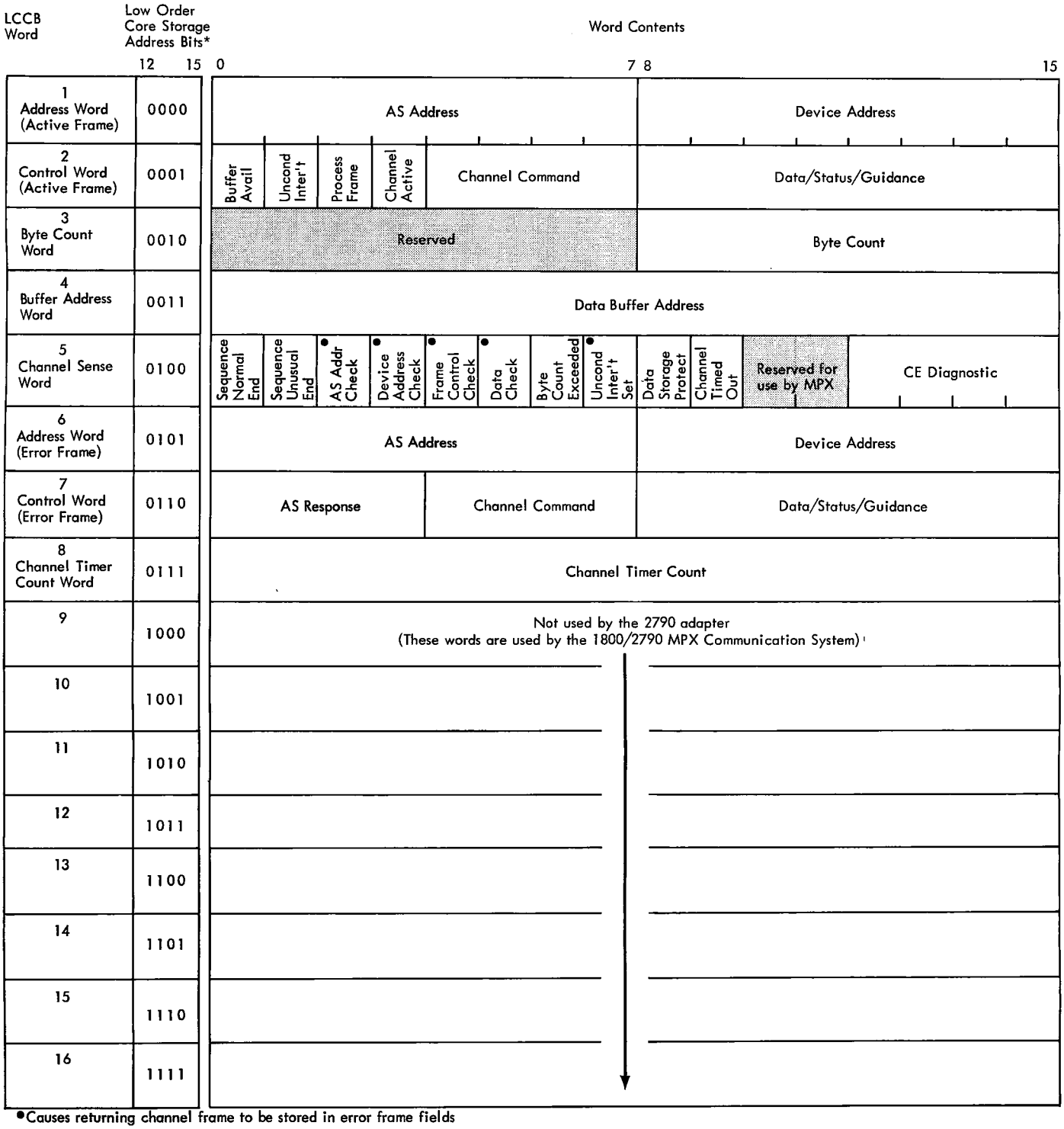
The two fields of the address word are described next.

AS ADDRESS: This eight-bit field contains the AS address code that can be transmitted in the channel frame for this channel. When processing a returning channel frame, the adapter uses this field to compare the returning AS address with the one transmitted. If the two do not compare equal and the AS address field does not contain the any-AS-address code, an AS address check occurs. If the AS address field contains the any-AS-address code, but the returning channel frame contains a specific AS address, the adapter proceeds as though the channel frame were captured. Consequently, the returning AS address is stored in the AS address field for future communication with the AS.

When initializing a channel for a read operation, the program normally places the any-AS-address code in the field prior to activating the channel. The any-AS-address code essentially performs a polling function by indicating to each AS that the channel is available for data transfer to the 1800.

When initializing a channel for a write operation, the program normally places a specific AS address or the all-AS-address code in this field prior to activating the channel. The all-AS-address code results in broadcast mode operation.

DEVICE ADDRESS: This eight-bit field contains the device address code that can be transmitted in the channel frame for this channel. When processing a returning channel frame, the adapter uses this field to compare the returning device address with the one transmitted. If the two do not compare equal and an AS did not capture the channel frame, a device address check occurs. If an AS captured an any-AS-address channel frame, the returning device address byte is stored in this field for use in future communication with the device.



●Causes returning channel frame to be stored in error frame fields

* Address bits 0 through 7 reflect 256-word boundary table address

Address bits 8 through 11 should reflect particular channel number being serviced (0001 through 1101)

Figure 124. Loop Channel Control Block Format

When initializing a channel for a read operation, the program need not specify a device address, as the AS automatically returns the device address when it captures a channel frame.

When initializing a channel for a write operation, the program must place the desired device address in this field prior to activating the channel. The device address may be /00 through /3F for pulse count adapter, /80 for the AS display, or /40 for the 1053 Printer.

LCCB Control Word (Active Frame)

The control word (active frame) is the second word in the LCCB. This word provides a channel control field; command code field; and a field for data, status, or guidance characters.

If the adapter is active, the control word is always transferred to the adapter whenever either of two events occurs: (1) the assigned channel is sequentially selected for channel frame transmission to the loop, or (2) that channel is selected for processing of a channel frame returning from the loop. The adapter interrogates the channel control bits to determine whether or not to transmit an active channel frame, or whether or not to process the returning channel frame.

The various fields of the control word are described next.

BUFFER AVAILABLE: If this bit is on, the adapter can automatically reinitiate another read operation with this channel (after read end acknowledge is received) without causing an interrupt to the program. The new read operation is automatically initiated with read null and any-AS-address codes, provided normal ending status is received with read end acknowledge. If unusual status is received with read end acknowledge, a channel interrupt to the program is generated (even if buffer available is on), sequence unusual end is posted in the channel sense word, and the channel is deactivated. If buffer available is off when read end acknowledge is received, then a channel interrupt to the program is generated, the type of ending (normal or unusual) is posted in the channel sense word, and the channel is deactivated.

Buffer available is fully controlled by the program; that is, the adapter interrogates buffer available but does not change its status. The status of buffer available is normally set by the program during the interrupt routine in which the read end command is placed in the LCCB to terminate a previous read operation. If the program chooses to make the channel immediately available for another read operation without being interrupted again, it places a new data buffer address, byte count, and channel timer count in the LCCB and turns on buffer available. If the program does not choose to immediately reinitiate another read operation, it must ensure that buffer available is off before activating the channel for the read end command.

UNCONDITIONAL INTERRUPT: This channel control bit is not usually used during normal channel operation. However, it may be used by the program to implement diagnostic control sequences. Unconditional interrupt being on causes the adapter to alter the method of processing returning channel frame for the specific channel, providing the frame process bit is on. The following events occur: (1) the returning channel frame is stored in the LCCB error frame words (6 and 7) instead of updating the active frame words (1 and 2), (2) a channel interrupt to the program is generated, (3) unconditional interrupt is posted in the channel sense word, and (4) the channel is deactivated.

Once unconditional interrupt is turned on, it remains on until turned off by the program.

Unconditional interrupt must be used by the program when any of the control-type commands are transmitted. This enables the adapter to process the returning channel frames for the control commands.

PROCESS FRAME: This bit is used by the adapter to determine whether a returning channel frame for the channel is to be processed or ignored. Process frame being on causes the adapter to take one of two actions: (1) process the returning channel frame, byte by byte, and set up the next channel frame to be transmitted for the channel, or (2) generate a channel interrupt to the program. Process frame being off causes the adapter to ignore the channel returning from the transmission loop.

The status of process frame is automatically controlled by the adapter and should not be changed by the program. Process frame is turned on when the next channel frame is transmitted after the channel is activated by the program. This timing ensures that the adapter does not attempt to process returning channel frames until an active channel frame has been transmitted for the channel. Once turned on, process frame remains on until the channel is deactivated and a channel interrupt to the program is generated.

CHANNEL ACTIVE: This channel control bit is used by the adapter to determine whether or not the channel is active. Each time the adapter sequentially selects the channel for transmission to the loop,

channel active is interrogated. If channel active is on, the contents of the AS address, device address, channel command, and data/status/guidance fields in LCCB words 1 and 2 are transmitted to the loop in the channel frame. If this is the first channel frame transmitted after the channel was activated, process frame is turned on to permit processing of the returning channel frame. If channel active is off when interrogated, an active channel frame is not transmitted. A channel frame consisting of a start byte and all sync bytes is transmitted in place of the active channel frame.

Channel active must be turned on by the program, but it is turned off automatically by the adapter. Turning on channel active is similar to issuing an XIO start to the channel; that is, it causes the adapter to perform the sequence of operations necessary to complete the operation specified by the channel command. Therefore, before turning on channel active, the program must initialize the LCCB for the specific operation desired. (For initialization details, see "LCCB Initialization.")

Once channel active is turned on, it remains on until a channel interrupt to the program is generated. At this time, channel active is automatically turned off by the adapter.

CHANNEL COMMAND: This field is used to store the channel command that is to be transmitted in the channel frame. If channel active is on, the channel command is transmitted in bit positions 4 through 7 of the channel frame control byte.

When processing a returning channel frame, the adapter uses the channel command field to determine: (1) whether the proper response was returned by the AS, (2) what command, if any, is to be generated for transmission in the next channel frame, (3) whether a channel interrupt to the program should be generated, and (4) whether the returning channel frame data byte should or should not be checked or processed.

To initialize the channel for a read operation, the program should place a read null command in the channel command field prior to activating the channel. To initialize the channel for a write operation, the program should place a write command in the channel command field prior to activating the channel.

DATA/STATUS/GUIDANCE: The adapter uses this field to control the flow of information to and from the transmission loop. When the channel is active, the contents of this field are transmitted in the active channel frame data byte.

During a read operation, the first transmission of each data character from an AS to the adapter is stored in this field until the second transmission of the data character is received. The two data characters are then compared to determine whether the transmission was correct before placing the data character in the data buffer.

During a write operation, each data character to be transferred to a device is fetched from the data buffer and placed in this field for subsequent transmission in a channel frame data byte. The returning channel frame data byte is then compared with this field to determine if the transmission was correct.

During an ending sequence, this field is used to store the status received from the AS or device. If the status is not changed by the program, it is transmitted (unmodified) as terminating status with the subsequent end command. However, the program can interrogate this status to determine whether or not to generate new terminating status or a new guidance character (AS local I/O only) for transmission with the end command.

LCCB Byte Count Word

The byte count word is the third word in the LCCB. It is used to initially specify the number of data bytes (two bytes per core storage word) located in the data buffer assigned to the channel for a specific operation. Only bit positions 8 through 15 may be used to specify the byte count. The byte is specified by the program when initializing the LCCB prior to activating the channel. The adapter decreases the byte count each time a data byte is transferred to or from the data buffer.

During a write operation, the byte count being decreased to 0 causes the adapter to automatically terminate the operation with a write end command accompanied by normal end status (/00).

Termination of a read operation is normally initiated by the AS or device. If the byte count reaches 0 and an attempt is made to transfer another data byte, then a channel interrupt to the program is generated, byte count exceeded is posted in the channel sense word, and the channel is deactivated.

During data transfer operations, the byte count is used to determine which core storage bit positions the data byte is to be transferred to or from. When the byte count is even, the data byte is transferred to or from bit positions 0 through 7 of the core storage word; when the byte count is odd, the data byte is transferred to or from bit positions 8 through 15 of the core storage word.

LCCB Data Buffer Address Word

The data buffer address word is the fourth word in the LCCB and is used to store the core storage address to or from which the next data character is to be transferred. When initializing the LCCB prior to activating the channel, the program places the starting address of the data buffer associated with the operation in the data buffer address word. Each time the byte count is increased to an even number, the data buffer address is increased by 1. This procedure allows packing of two data bytes per core storage word.

LCCB Channel Sense Word

The channel sense word is the fifth word in the LCCB and is used by the adapter to store indicators that define the cause of a channel interrupt to the program. Whenever a channel interrupt is generated, the adapter posts the interrupt condition(s) in the channel sense word and deactivates the channel. While the channel is inactive, the contents of the LCCB are not modified by the adapter and are available for program interrogation.

The individual indicators in the channel sense word are described next.

SEQUENCE NORMAL END: This status indicator is turned on when a read or write sequence initiated by the program reaches an ending point, and the AS or device status associated with the end indicates normal end status.

SEQUENCE UNUSUAL END: This status indicator is turned on when a read or write sequence initiated by the program is prematurely terminated as a result of a request from the AS or device. The reason for the termination is defined by the AS or device status stored in the data/status/guidance field in word 2 of the LCCB. If the AS or device status indicates diagnostic mode, sequence unusual end is also turned on.

AS ADDRESS CHECK: This status indicator is turned on if an error is detected in a returning channel frame AS address byte. An AS address check causes the returning channel frame in which the error is detected to be stored in the error frame fields (LCCB words 6 and 7) for use in error recovery.

DEVICE ADDRESS CHECK: This status indicator is turned on if an error is detected in a returning channel frame device address byte. A device address check causes the returning channel frame in which the error is detected to be stored in the error frame fields (LCCB word 6 and 7) for use in error recovery.

FRAME CONTROL CHECK: This status indicator is turned on if an error is detected in a returning channel frame control byte. A frame control check causes the returning channel frame in which the error is detected to be stored in the error frame fields (LCCB words 6 and 7) for use in error recovery.

DATA CHECK: This status indicator is turned on if an error is detected in a returning channel frame data byte. A data check causes the returning channel frame in which the error is detected to be stored in the error frame fields (LCCB words 6 and 7) for use in error recovery. The AS response and channel command fields in the error frame are not valid when a data check occurs; that is, they do not reflect the contents of the returning channel frame control byte.

BYTE COUNT EXCEEDED: This status indicator is turned on during a read operation if an attempt is made to store an additional data byte after the byte count has been decreased to 0. Byte count exceeded indicates that the input data buffer assigned is too small for the incoming data.

UNCONDITIONAL INTERRUPT: This status indicator is turned on if the unconditional interrupt control bit in word 2 of the LCCB is on when a returning channel frame arrives for processing. Unconditional interrupt causes the returning channel frame to be stored in the error frame fields (LCCB words 6 and 7).

DATA STORAGE PROTECT: This status indicator is turned on if an attempt is made to store a data byte in a data buffer location that is storage protected.

CHANNEL TIMED OUT: This status indicator is turned on if a channel timer count overflow condition is indicated. The overflow condition is indicated by bit 0 of the LCCB channel timer count word being on. Channel timed out indicates that the channel has been unsuccessfully attempting to complete a data transfer operation for a period of time longer than allotted by the program.

CE DIAGNOSTIC: These four indicators are used by customer engineers (CE's) for diagnostic purposes. The indicators are active only when wired by a CE and do not represent interrupt conditions nor cause interrupts to the program. Therefore, one of the other ten interrupting conditions must occur to cause an update of the channel sense word, and thus storing of the CE diagnostic indicators. The CE diagnostic indicators are always off unless wired for use by a CE.

LCCB Address Word (Error Frame)

The address word (error frame) is the sixth word in the LCCB. This word is used by the adapter to store the AS address byte and device address byte of a returning channel frame if an error is detected in any portion of the channel frame, or if unconditional interrupt is on in the channel control field (LCCB word 2). The address word (error frame) contains the following fields:

AS ADDRESS: This field is used to store the returning channel frame AS address byte.

DEVICE ADDRESS: This field is used to store the returning channel frame device address byte.

LCCB Control Word (Error Frame)

The control word (error frame) is the seventh word in the LCCB. This word is used by the adapter to store the control byte and data byte of a returning channel frame if an error is detected in any portion of the channel frame, or if unconditional interrupt is on in the channel control field (LCCB word 2). The control word (error frame) contains three fields, described next.

AS RESPONSE: This field is used to store the AS response digit (bit positions 0 through 3) from the returning channel frame control byte. If a data check causes the returning channel frame to be stored in the error frame field, the AS response field is not valid; that is, it does not contain the AS response digit from the returning channel frame.

CHANNEL COMMAND: This field is used to store the channel command digit (bit positions 4 through 7) from the returning channel frame control byte. Unless a transmission error occurs, this field should be identical to the transmitted channel command located in word 2 of the LCCB. If a data check causes the returning channel frame to be stored in the error frame field, the channel command field is not valid; that is, it does not contain the channel command digit from the returning channel frame.

DATA/STATUS/GUIDANCE: This field is used to store the contents of the returning channel frame data byte. The returning channel frame data byte may contain data, status, or guidance, depending on the channel command transmitted and the AS response to the command.

LCCB Channel Timer Count Word

The channel timer count word is the eighth word in the LCCB. This word is used to specify the number of times the channel can attempt data transfer to complete an operation before a channel interrupt to the program is generated. The channel timer count is initially set by the program while initializing the LCCB and is then increased by 1 for each unsuccessful data transfer attempt after the channel is activated. An unsuccessful data transfer attempt is recognized when a read command acknowledge with busy status, read null acknowledge, a write command acknowledge with busy status, or a write null acknowledge is received in the returning channel frame.

Bit position 0 of the channel timer count word is used to determine when a channel interrupt to the program is to be generated. This bit position is interrogated each time the channel timer count is increased. If bit position 0 is on, a channel timer count overflow is indicated which causes the adapter to generate a channel interrupt to the program, post the condition in the channel sense word, and deactivate the channel. Thus, the maximum count the timer may reach before an interrupt is generated is 32,767.

DATA ENTRY FORMATS

The format of data entry, as it appears in the assigned input data buffer, depends on which device enters the data. Figure 125 shows the data format that appears in the data buffer for each type of device.

Three special characters -- transaction code, guidance, and status -- may be used during a data entry. They are described in the following paragraphs.

2796 Data Entry

0 7	8 15
Upper LH Sw *	Monitor Key **
Upper RH Sw	Data 1
Data 2	Data 3
Data 10	Lower LH Sw
Lower RH Sw	Thumbwheel 1
Thumbwheel 2	Thumbwheel 3
Thumbwheel 4	

* This character is normally used as a transaction code.

** Value may be /F1, /F2, or /F3.

Pulse Count Adapter

0 7	8 15
Transaction **	H.O. Counter No.*
2nd Counter No.	3rd Counter No.
4th Counter No.	L.O. Counter No.

*=Bit 12, count/no count test bit.
** Bits 4-7 = Overflow Ind.

Keyboard Entry

0 7	8 15
Transaction	Old Guidance
Data 1	Data 2
Data 3	Data 4
Data 5	Data 6

AS Badge or OEM Digital Entry

0 7	8 15
Transaction	Old Guidance
Data 1	Data 2
Data 9	Data 10

2795 Data Entry

0 7	8 15
LH Rotary Sw *	Model Code **
RH Rotary Sw	Data 1
Data 2	Data 3
Data 8	Data 9
Data 10	

* This character is normally used as a transaction code.

** Value is /F0 for 2795.

2797 Data Entry

0 7	8 15
LH Sw *	Monitor Key**
RH Sw	Data 1
Data 2	Data 3
Data 10	Visual Display 1
Visual Display 2	Visual Display 3
Visual Display 4	Visual Display 5
Visual Display 6	

* This character is normally used as a transaction code.

** Value may be /F4, /F5,/ or /F6.

AS Card Entry

0 7	8 15
Transaction	Old Guidance
Data 1	Data 2
Data N-1	Data N *

* Message length may vary up to 80 characters.

1035 Badge Entry *

0 7	8 15
Transaction	Data 1
Data 2	Data 3
Data 8	Data 9
Data 10	

* 1035 badge entry shown above is modified in ouput files provided by MPX so that the output file agrees with the AS badge or OEM digital entry format.

Next Guidance or Transaction Select

0 7	8 15
Transaction	Old Guidance

Note:
Data buffers will begin in bit positions 8 through 15 if an odd byte count is initially specified.

17897B

Figure 125. 2790 Adapter Data Buffer Formats

Transaction Code Character

The transaction code character is the first character placed in the data buffer during each data entry. The program uses this character in determining what action is necessary to complete a transaction. Figure 126 shows the contents of the transaction code characters for the various devices.

Guidance Character

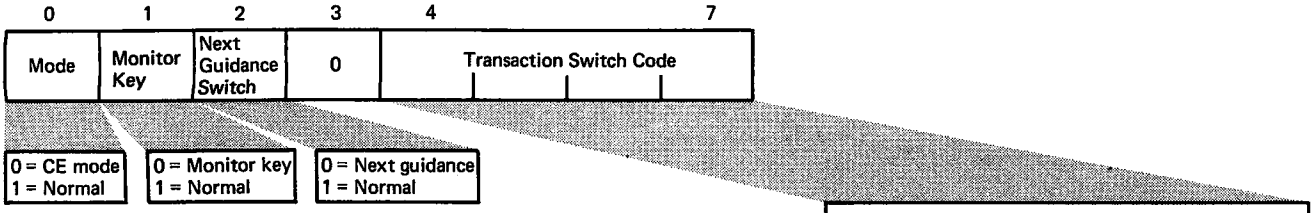
Data entry from any AS local input device (except 1035) results in transmission of the current guidance character as the second character of the data entry. This character is the source of the information displayed to the operator by the guidance lights, and it is also the means by which an AS local input device is enabled to perform an input function.

The guidance character is transmitted to the AS with a read end command. The AS uses it as the current guidance character until a new guidance character is transmitted with a subsequent read end command. Figure 127 shows how the contents of the guidance character are used.

Status Character

Status characters are associated with each data entry but do not appear in the data buffer. Status received with an end request from an AS indicates the conditions under which termination of the operation is requested. Status transmitted to an AS indicates the conditions under which the operation is to be terminated and, if required, results in the proper indication or action at the AS or device. Figure 128 provides a summary of status characters.

AREA STATION LOCAL I/O TRANSACTION CODE BYTE



0 = CE mode
1 = Normal

0 = Monitor key
1 = Normal

0 = Next guidance
1 = Normal

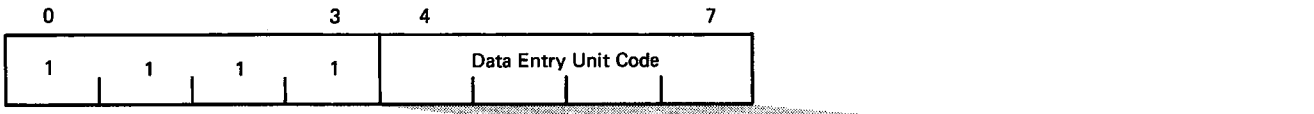
0000 = No transaction
0001 = Switch 1
0010 = Switch 2
0011 = Switch 3
0100 = Switch 4
0101 = Switch 5
0110 = Switch 6
0111 = Switch 7
1000 = Switch 8
1001 = Switch 9
1010 = 1035 Badge Readers
1111 = CE transaction

This transaction code is the first data character transmitted in any message from the AS local I/O devices.

These devices include:

AS badge reader
AS card reader
AS keyboard
1035 Badge Readers
AS transaction and next guidance switches
OEM digital device

DATA ENTRY UNIT TRANSACTION CODE BYTE

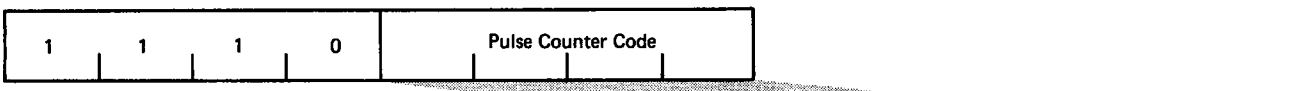


This transaction code is the first data character transmitted in a message from a data entry unit.

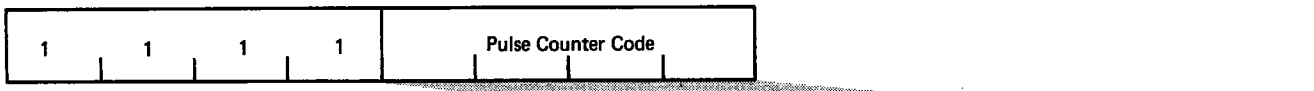
0000 ↓ 1001 — Indicates the setting of the left-hand rotary switch (upper left-hand for 2796)

1111 = AS CE transaction switch is on (2793 only)

PULSE COUNT ADAPTER TRANSACTION CODE BYTES



1100 = not overflow
1101 = overflow

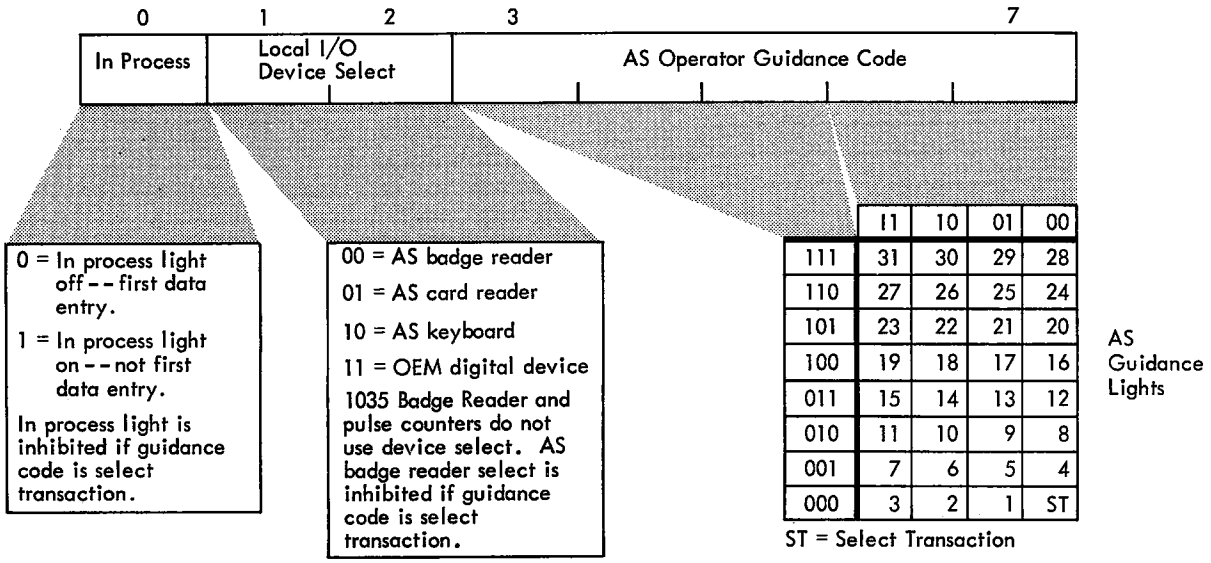


1100 = Read command with a device address other than 00 sent, while pulse count adapter was reporting a power interruption.
1101 = Power interruption occurred.

17898A

Figure 126. 2790 Transaction Codes

AS Local I/O Guidance Character



The guidance character is the second character transmitted in any message from the AS local I/O devices (except 1035 Badge Reader and pulse counters). In this case, the the guidance character reflects the "old guidance"--that is, the previous guidance character sent with a read end command to a local I/O device. A guidance character sent with a read end command to a local I/O device is considered to be "new guidance". It becomes "old guidance" when a new message is initiated.

17899A

• Figure 127. Operator Guidance Codes

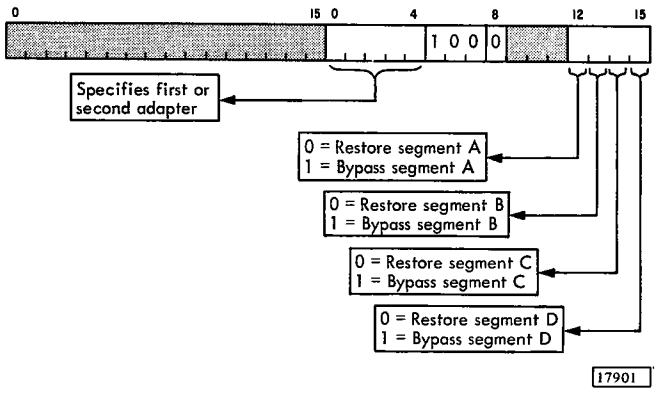
2790 ADAPTER PROGRAMMING

Overall control of each 2790 adapter is accomplished by means of the execute I/O (XIO) instruction. Input/output control commands (IOCC's) referenced by an XIO provide a means for activating or deactivating the adapter and for identifying interrupt status during operation. While the adapter is active, individual loop channel control is achieved by interrogation and manipulation of the various fields in the individual loop channel control blocks (LCCB's).

IOCC's referenced by an XIO must have an area code of 00111 to address the first adapter, or an area code of 10011 to address the second adapter. The following IOCC's are used with adapter operation.

2790 Adapter IOCC's

Control (Stop Loop)



17901

STATUS CHARACTER CODES

Status Char in Hex	Status Associated with End Request from AS					Status Associated with End Command to AS				
	AS Local I/O	1035 Badge Reader	1053 Printer	Data Entry Unit	Pulse Count Adapter	Note 1: AS Local I/O	1035 Badge Reader	1053 Printer	Data Entry Unit	Pulse Count Adapter
00	Normal End	Normal End		Normal End	Normal End			Normal End	Release	Normal End
01										Reset Counter
02										Reset Count / No Count Bit
04										Reset Overflow Bits
05										Reset Counter to 00000
07										Reset Counter to 00000 Reset Count/ No Count Bit
08										Toggle Diag. Contact 3 times
Note 4 10										Intrpt. Trans. Code
20	Diagnostic Mode		Diagnostic Mode	Diagnostic Mode		No Action		No Action	No Action	
40	Release in Data Mode			Overrun		Turn on Repeat/ Clear			Error Indication	
60	Release in Diagnostic & Data Mode			Overrun in Diagnostic Mode		Turn on Repeat/ Clear			No Action	
80	Note 2 Invalid Character	Invalid Character	Out of Paper	Timeout	Note 3 Busy	Turn on Repeat/ Clear	Turn on Repeat	No Action	Error Indication	Unusual End—No Action
A0	Invalid Character Diag Mode		Out of Paper Diag Mode	Timeout Diagnostic Mode	Count Buffer Full	Turn on Repeat/ Clear		No Action	No Action	
C0	Overrun (Card Reader)				No Contact Sense Card	Turn on Repeat/ Clear				
E0	Overrun in Diagnostic Mode					Turn on Repeat/ Clear				

Note 1. All other hexadecimal codes are accepted as guidance characters by the AS local I/O devices. (See "AS Local I/O Guidance Character.")

Note 2. This status character (/80) indicates that the display is busy when returned with write command acknowledge.

Note 3. This status character (/80) indicates that other than 5 characters were received by the adapter when returned with write command acknowledge.

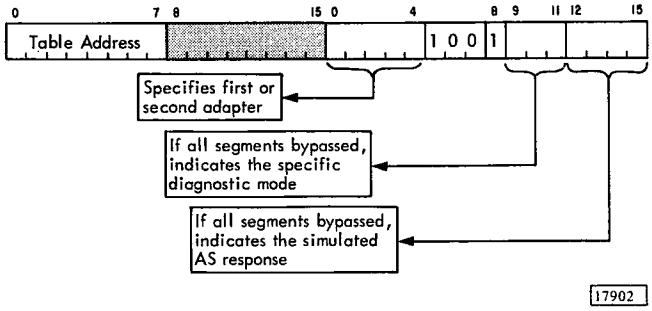
Note 4. This status character (/10) may be combined with /04 to reset counter /00 overflow for a power interruption report.

17900A

• Figure 128. Status Characters

This command removes the adapter from active mode, if active, and conditions the segment bypass control according to modifier bits 12 through 15 as shown in the preceding illustration. When deactivated, the adapter ceases to sequentially select each loop channel for service, stops all communication with the adapter control table, and halts all further interrupts or data channel operations. Any data transfer operations in progress when an XIO control (stop loop) is given are immediately halted and are not allowed to continue to completion. Therefore, this command should not normally be used to deactivate the adapter until all data transfer operations in progress are completed and all loop channels are deactivated. However, XIO control (stop loop) may be used at any time for implementing error recovery.

Control (Start Loop)



This command provides an initial reset to the adapter and then places the adapter in active mode. When activated, the adapter begins transmitting and processing channel frames and sequentially selects each channel for service.

Address word bit positions 0 through 7 are transferred to the adapter and used as the base address of the adapter control table in all subsequent communication.

If all segments are bypassed (as used for diagnostic functions), modifier bits 9 through 11 are used to specify a particular diagnostic function, and modifier bits 12 through 15 may be used to simulate area station response digits. Diagnostic functions provided are:

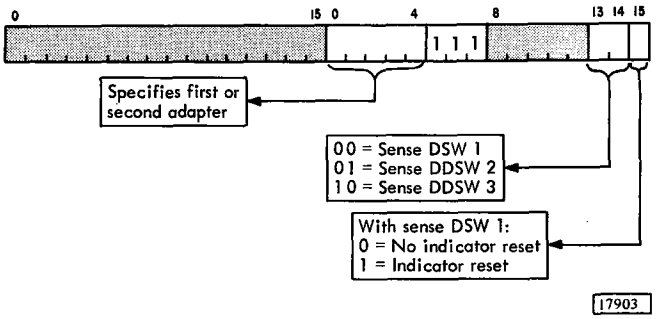
000 = Normal transmission
011 = Inhibit start character
100 = Single-step mode
101 = Force all zeros
110 = For all ones
111 = Force start character

These functions are further defined under "Diagnostic Functions."

Prior to issuing an XIO control (start loop), the program must ensure that each loop channel control block (LCCB) has been properly initialized for a data transfer operation, or that channel active is off in the LCCB's not initialized for data transfer. This requirement ensures that no error conditions are caused by transmission of channel frames containing invalid information.

Form GA26-5918-8
Page Added 10/1/70
By TNL GN26-0263

Sense Device



This command is used to load one of three adapter device status words (DSW's) into the accumulator. Modifier bits 13 and 14 specify the status word to be sensed as follows:

00 = Device status word 1 (DSW1)
01 = Diagnostic device status word 2 (DDSW2)
10 = Diagnostic device status word 3 (DDSW3)

When used with DSW1, modifier bit 15 controls reset of the program resettable indicators and transfer of channel interrupts presently stacked in the interrupt status hold word (ISHW) to the interrupt status word (ISW). If modifier bit 15 is on, program resettable indicators are reset and the ISHW is transferred to the ISW; if modifier bit 15 is off, program resettable indicators are not reset and the ISHW is not transferred to the ISW.

2790 Adapter DSW1 Interrupt Indicators

Figure 129 shows the format of DSW1 and defines the indicators that cause interrupts. Program resettable indicators are also defined.

ADAPTER ERROR INTERRUPT: This indicator turns on, causing an interrupt, when any one of the following error conditions occurs:

1. Command reject.
2. No frame.
3. Storage protect violation.
4. P-C parity error.
5. Adapter parity error.

These error conditions are indicated by DSW1 indicators 1 through 5, respectively.

LOOP CHANNEL INTERRUPT: This indicator turns on, causing an interrupt, when any of the 13 loop channels requests an interrupt. The channels requesting interrupt are defined by the indicators in the ISW.

2790 Adapter DSW1 Noninterrupt Indicators

Figure 129 shows the format of DSW1 and defines noninterrupt and program resettable indicators.

COMMAND REJECT: This indicator turns on if:

1. An invalid XIO is given to the adapter.
2. An XIO control (start loop) is issued while the adapter is in active mode and all segments are not bypassed.

Command reject turning on also turns on adapter error interrupt, which causes an interrupt to the program.

NO FRAME: This indicator turns on if the adapter fails to receive start or sync bytes from the transmission loop for a period of 100 ms. This indicates that channel frame transmission has been interrupted. No frame turning on removes the adapter from active mode and turns on adapter error interrupt, causing an interrupt to the program.

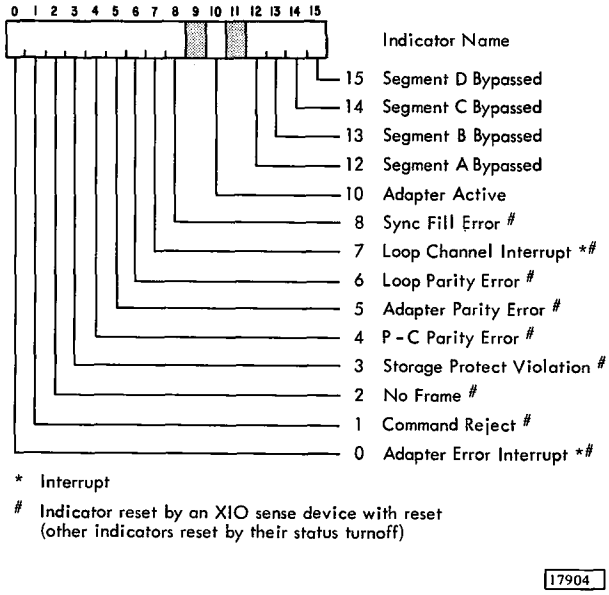


Figure 129. 2790 Adapter Device Status Word 1

STORAGE PROTECT VIOLATION: This indicator turns on if the adapter attempts to store information in the LCIB or any LCCB and the location is storage protected. Storage protect violation turning on removes the adapter from active mode and turns on adapter error interrupt causing an interrupt to the program.

P-C PARITY ERROR: This indicator turns on if the P-C detects a parity error while storing in or fetching from core storage during adapter operations. P-C parity error turning on removes the adapter from active mode and turns on adapter error interrupt, causing an interrupt to the program.

ADAPTER PARITY ERROR: This indicator turns on if the parity generated by the adapter for transmission on the loop differs from the parity received from the P-C. Adapter parity error turning on removes the adapter from active mode and turns on adapter error interrupts, causing an interrupt to the program.

LOOP PARITY ERROR: This indicator turns on if the parity generated during data transfer to core storage differs from the parity received from the transmission loop. Loop parity error turning on does not remove the adapter from active mode.

SYNC FILL ERROR: This indicator turns on if the adapter detects loss of a sync byte while receiving bytes 5 through 29 of a channel frame. Sync fill error may be used for analyzing intermittent transmission errors. By interrogating this indicator while transmitting send sync commands to successive area stations, the program can isolate the failure to a link connecting two area stations.

ADAPTER ACTIVE: This indicator is on while the adapter is in active mode. It is turned on by an XIO control (start loop) and turned off by an XIO control (stop loop) or one of the adapter error conditions.

SEGMENT A BYPASSED: This indicator is on while segment A of the transmission loop is bypassed. The bypass status of segment A is controlled by modifier bit 12 in an XIO control (stop loop).

SEGMENT B BYPASSED: This indicator is on while segment B of the transmission loop is bypassed. The bypass status of segment B is controlled by modifier bit 13 in an XIO control (stop loop).

SEGMENT C BYPASSED: This indicator is on while segment C of the transmission loop is bypassed. The bypass status of segment C is controlled by modifier bit 14 in an XIO control (stop loop).

SEGMENT D BYPASSED: This indicator is on while segment D of the transmission loop is bypassed. The bypass status of segment D is controlled by modifier bit 15 in an XIO control (stop loop).

2790 Adapter DDSW2 Indicators

Diagnostic DSW2 (DDSW2) is generally used for diagnostic purposes in conjunction with single-step mode. However, DDSW2 may be sensed at any time during adapter operation.

The format of DDSW2 is shown in Figure 130. The indicators in DDSW2 bit positions 5 through 15 indicate the functional sequence being performed by the adapter by means of data channel (cycle steal) operations. Only one of these indicators will be on during any data channel sequence. DDSW2 bit positions 1 through 3 are used to define the specific steps within the data channel sequence indicated by bit positions 5 through 15.

DDSW2 is used in implementing single-step mode, as described under "Diagnostic Functions."

2790 Adapter DDSW3 Indicators

Diagnostic DSW 3 (DDSW3) is generally used for diagnostic purposes in conjunction with single-step mode. However, DDSW3 may be sensed at any time during adapter operation. The format of DDSW3 is shown in Figure 131.

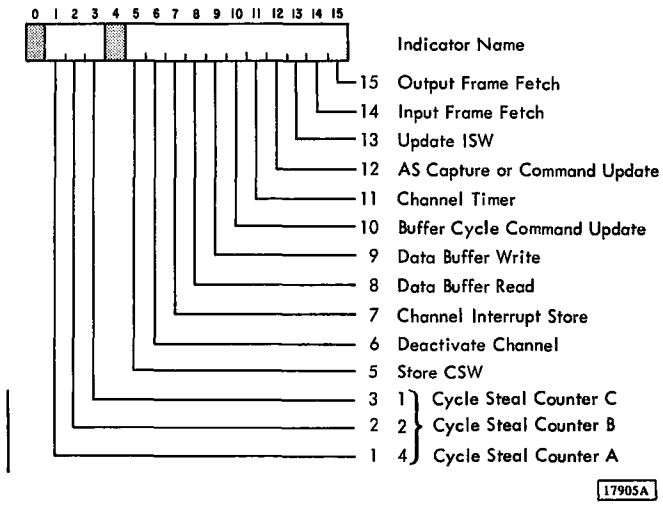


Figure 130. 2790 Adapter Diagnostic Device Status Word 2

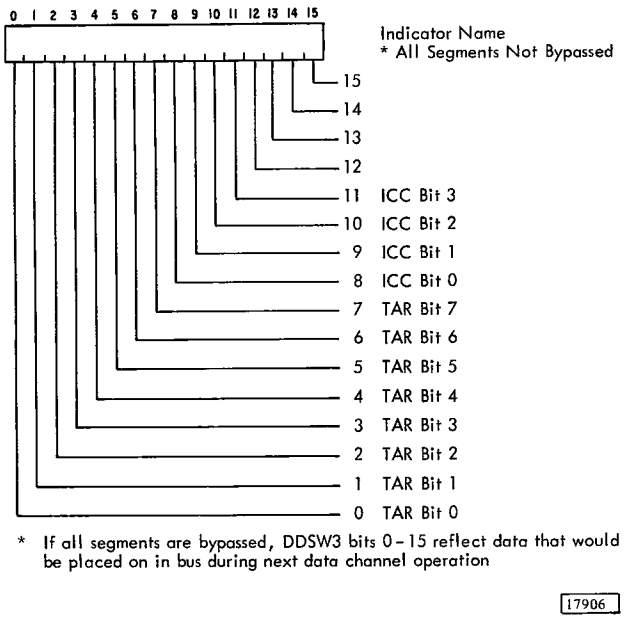


Figure 131. 2790 Adapter Diagnostic Device Status Word 3

When the adapter is not in diagnostic mode (all segments not bypassed), DDSW3 bit positions 0 through 7 reflect the adapter control table address held in the adapter table address register (TAR). DDSW3 bit positions 8 through 11 reflect the contents of the input channel counter, which defines the loop channel for which a channel frame is currently being processed from the loop. Collectively, DDSW3 bit positions 0 through 11 identify the LCCB with which the adapter is communicating at the time DDSW3 is sensed.

When the adapter is in diagnostic mode, DDSW3 reflects the data that would be placed on the in bus by the adapter during the next data channel operation. In diagnostic mode, DDSW3 is used in implementing single-step mode, as described under "Diagnostic Functions."

LCCB INITIALIZATION

The LCCB's (one for each of the 13 loop channels) contain the information required by the adapter to control loop channel operation. Before the program issues an XIO control (start loop) or activates a specific channel, some of the LCCB information must be initialized to a prescribed state. This requirement ensures that no erroneous channel frames are inadvertently transmitted to the loop, where they would cause error conditions.

Start Loop LCCB Initialization

Prior to issuing an XIO control (start loop), the program must ensure that each of the 13 LCCB's is properly initialized for an active or inactive state. If immediate channel operation is desired after activating the adapter and without further program intervention, the LCCB for the channel should be initialized as described under "Channel Active LCCB Initialization," and channel active should be turned on. If immediate operation is not desired for a specific channel, the program should ensure that channel active is off in the LCCB for the channel.

Channel Active LCCB Initialization

Turning on channel active for a specific channel is equivalent to issuing an XIO start to that channel. Therefore, before channel active is turned on, the information in the LCCB must be initialized to prepare for transmitting a channel frame to the loop.

> Note: A store double (STD) instruction should not be used to initialize the active frame address and control words in the LCCB at the same that channel active is turned on. With an STD instruction, the control word is placed in the LCCB before the address word is placed there. If channel active is on in the control word, the channel is immediately considered active even though the address word has not yet been stored. This condition may result in a channel frame being transmitted with incorrect AS and device addresses.

Which information of the LCCB must be initialized depends on the operation, as indicated in the following paragraphs. It is recommended that all other fields and bits not specified for initialization in the first eight LCCB words be set to 0. This allows a true indication of any change in these fields even if an interrupt condition is not generated.

INITIAL READ OPERATION: To ready an LCCB for an initial read operation, it should be set up as follows prior to activating the channel:

LCCB Field	Information
AS address	Any-AS-address code (Discrete device address for pulse counters.)
Channel command	Read null (Read command for system-initiated pulse counter read operations.)
Byte count	Data buffer byte count.

LCCB Field	Information
Data buffer address	Data buffer address
Channel timer count	Set as desired

CONTINUED READ OPERATION: To ready an LCCB so that another read operation is automatically initiated after sending a read end command, the LCCB should be set up as follows prior to activating the channel for read end.

LCCB Field	Information
AS address	AS address to receive read end
Device address	Device to receive read end
Channel command	Read end
Data/status/guidance	Terminating status or guidance character
Byte count	New data byte count
Data buffer address	New data buffer address
Channel timer count	Set as desired
Buffer available	Turned on

WRITE OPERATION: To ready an LCCB for a write operation, it should be set up as follows prior to activating the channel:

LCCB Field	Information
AS address	All-AS-address code for broadcast mode or discrete AS address for normal mode
Device address	Device to receive data
Channel command	Write command
Byte count	Data buffer byte count
Data buffer address	Data buffer address
Channel timer count	Set as desired

CHANNEL SEQUENCES

Once the LCCB for a channel has been initialized and activated, the adapter automatically steps the channel through a command-response sequence to complete the operation without further specification from the program. The adapter can automatically perform three sequences: read, write, and broadcast.

Any of the three sequences can be performed with any of the 13 channels. However, the variations in channel speeds and system throughput requirements must be considered. Read sequences are usually performed with channels 1 through 8 and write sequences with channels 9 through 13. It should be noted that all write sequences to 1053 Printers must be performed on low-speed channels (9 through 13). Data entry unit and AS card reader operations must be performed on high-speed channels (1 through 8).

Read Sequence

The read sequence transfers data from a requesting device to the data buffer in core storage. The read sequence can be entered by initializing an LCCB for an initial read operation or for a continued read operation prior to sending a read end command. Figure 132 shows the various command-response sub-sequences of a loop channel read operation.

Note that the program can initiate a read operation with a specific device (i.e., pulse counter) by sending a read command to that device. If the device is already in a read or write operation, busy status is returned with read command acknowledge. Otherwise the read command will start the normal read sequence.

An error condition may be detected at any time. This condition causes a channel interrupt to the program and the channel is deactivated. The error condition is indicated in the channel sense word.

The request sub-sequence of the read sequence is entered when an AS captures the channel by returning read request, its own assigned address, and the requesting device address in the channel frame. The request sub-sequence places the device in data mode and enables it to begin reading its data source.

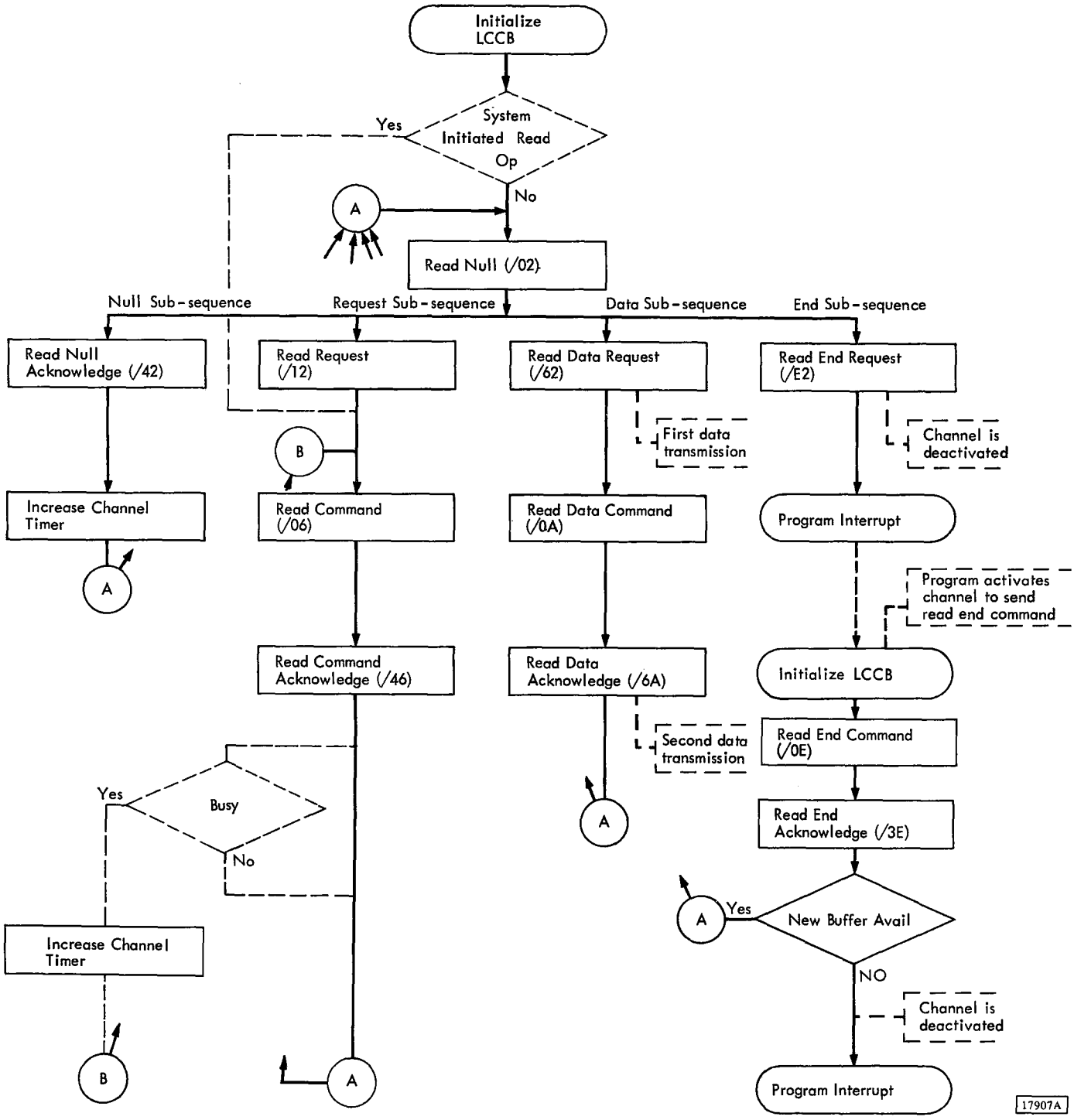
Null is the next sub-sequence of the read sequence and is performed until the device has a data character ready for transfer.

The data sub-sequence of the read sequence is entered when the device has a data character to be transferred, as indicated by returning read data request. During the data sub-sequence, the data character is transmitted twice to allow a validity check on data transmission.

After the data sub-sequence is performed, the null sub-sequence is again performed until the next data character is ready. This series of sub-sequences continues until the end sub-sequence is entered.

The end sub-sequence of a read sequence is entered when the device determines that all data has been transferred or it detects an error condition requiring termination of the operation. In either case, a channel interrupt to the program is generated and the channel is deactivated. The condition causing the interrupt is indicated in the LCCB channel sense word. Sequence normal end is indicated if data transfer is completed with normal status, and sequence unusual end is indicated if the device detects an error condition. The data/status/guidance field contains the status received from the device.

The program must initialize a channel to send read end to the requesting device. Any unused channel



• Figure 132. 2790 Adapter Read Sequence

may be used. Read end removes the device from data mode and releases it for another input operation. New guidance (AS local I/O only) or terminating status is sent with read end to inform the operator whether the message was accepted, and hence whether it must be repeated.

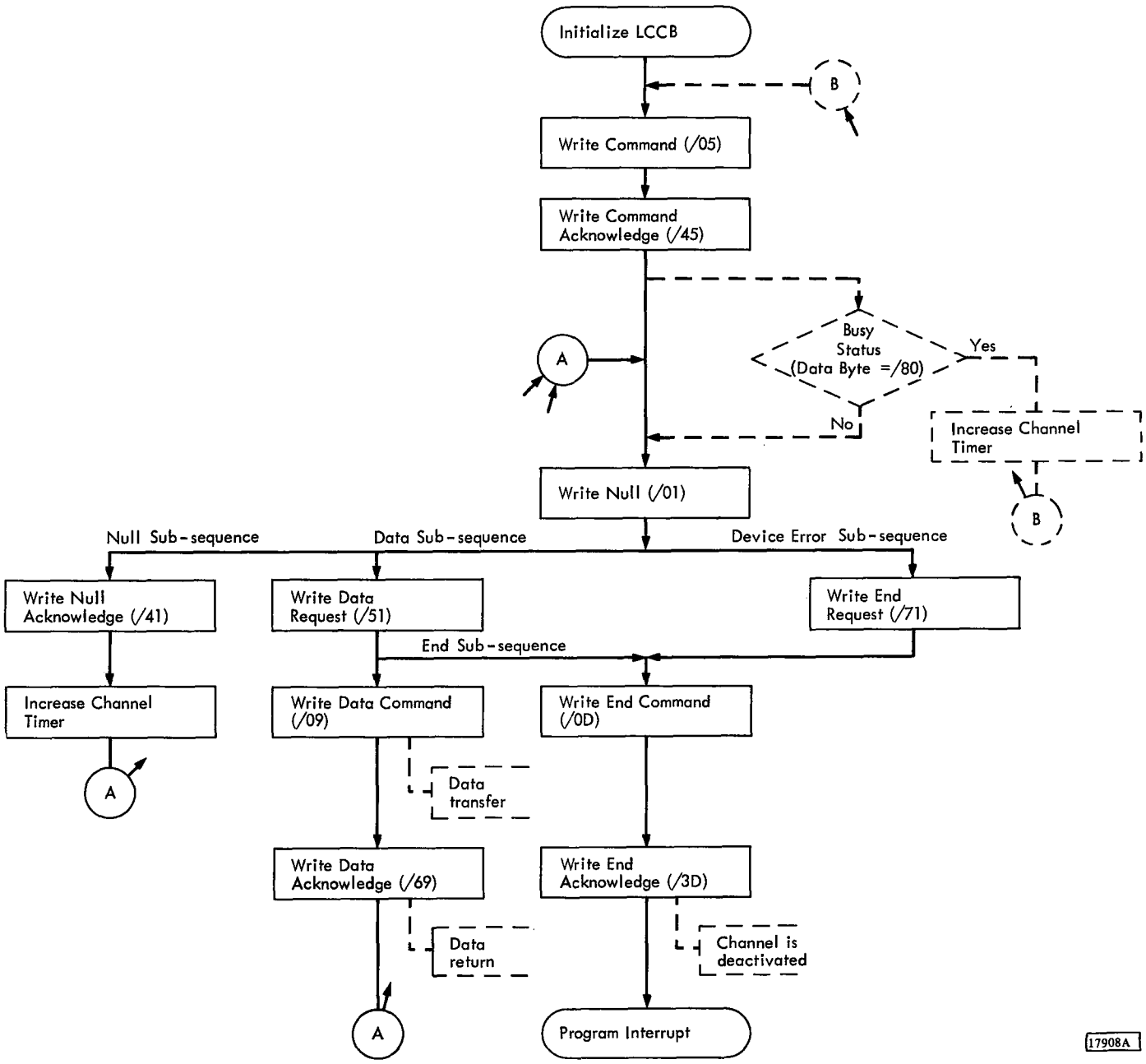
If a new data buffer was assigned while initializing the LCCB for the read end, a new read sequence is automatically initiated without an interrupt to the program, provided an error is not detected with read end acknowledge. If a new data buffer was not assigned, a channel interrupt to the program is generated upon receipt of read end acknowledge. Normal sequence end is indicated in the channel sense word unless an error is detected. If an error is detected, the appropriate error indicator is turned on in the channel sense word.

Write Sequence

The write sequence transfers data from a data buffer in core storage to a specific output device. The write sequence is entered by initializing an LCCB for a write operation. Figure 133 shows the various command-response sub-sequences of a channel write operation. Note that an error condition may be detected at any time. This condition causes a channel interrupt to the program and deactivates the channel. The error condition is indicated in the channel sense word.

The null sub-sequence of the write sequence is performed whenever two conditions exist: (1) no other sub-sequence is required, and (2) the output device is in data mode.

The data sub-sequence of a write sequence is performed each time the output device is ready to accept another data character. During the data sub-sequence, a data character is transferred to the



• Figure 133. 2790 Adapter Write Sequence

output device and then returned to the adapter for a validity check.

The device error sub-sequence of a write sequence is performed if the output device determines that it cannot perform the write operation, or if the output device detects an error condition during the write operation. In either case, sequence unusual end is posted in the channel sense word, a channel interrupt to the program is generated, and the channel is deactivated. The data/status/guidance field contains the unusual status received from the device.

The end sub-sequence of a write sequence is performed when the output device requests another data character and the byte count is 0. The end sub-sequence posts the ending condition in the channel sense word, generates a channel interrupt to the program, and deactivates the channel. The data/status/guidance field contains the terminating status of the device.

Broadcast Sequence

The broadcast sequence is a modified write sequence. It is used to transfer data, such as time display update, from core storage to all AS displays. The broadcast sequence is entered by initializing an LCCB for a broadcast write operation. During broadcast mode, no information in a channel frame is modified by any of the area stations. Therefore, no responses are returned by an AS. Each AS, if able, performs the operation.

Each channel frame in a broadcast sequence is checked by the adapter to ensure that no information has been modified during transmission around the loop. If an error is detected, the condition is posted in the channel sense word, a channel interrupt to the program is generated, and the channel is deactivated.

The broadcast sequence consists of three parts: (1) a write command to place all AS displays in data mode, (2) a series of write data commands to transfer the data characters to the AS display, and (3) a write end command (after the byte count is decreased to 0) to remove the AS displays from data mode and terminate the operation. When the operation is terminated with write end, the ending condition is posted in the channel sense word, a channel interrupt to the program is generated, and the channel is deactivated.

Control Sequences

Control sequences are used primarily for diagnostic purposes. The adapter does not automatically process control command-response sequences. Therefore, unconditional interrupt must be used in conjunction with any of the control command sequences. Unconditional interrupt causes returning channel frames to be stored in the LCCB error frame field. Analysis of each returning channel frame must be performed by the program.

INTERRUPT CONSIDERATIONS

Two types of interrupt conditions are associated with the 2790 adapter: interrupts associated with loop channel operations, and interrupts associated with overall adapter operation.

When an adapter interrupt occurs, the program should issue an XIO sense device with modifier bits 13 through 15 set to 000 to read the device status word (DSW1) into the accumulator. If the adapter error indicator (bit position 0) is on, it indicates that the interrupt is due to an error condition with overall adapter operation. The error condition is indicated in bit positions 1 through 5 of DSW1. If the channel interrupt indicator (bit position 7) is on, it indicates that the interrupt was caused by one or more of the 13 loop channels.

When a channel interrupt occurs, the interrupt status word (ISW) located in the loop channel interrupt block (LCIB) must be interrogated to determine which of the channels requires service. The channel sense word for each interrupting channel can then be interrogated to determine the cause of the channel interrupt request.

After servicing all interrupt conditions indicated in DSW1 and all channel interrupts as indicated in the ISW, the program should issue an XIO sense device specifying DSW1 with reset (modifier bits 13 through 15 set to 001). This resets the program resettable indicators in DSW1 and allows any channel interrupt requests stacked in the interrupt status hold word (ISHW) to be transferred to the ISW. Three nonconsecutive machine cycles are used to transfer the contents of ISHW to ISW by means of data channel operations. If any channel interrupt requests were stacked in the ISHW and transferred to the ISW, a new channel interrupt to the program is generated, provided the adapter is active.

DIAGNOSTIC FUNCTIONS

The 2790 adapter provides several diagnostic functions for analyzing malfunctions that may occur. Diagnostic functions are enabled only when all segments of the transmission loop have been bypassed.

When all segments are bypassed modifier bits 9 through 11 of an XIO control (start loop) are used to specify the particular diagnostic operation. Modifier bits 12 through 15 are used to simulate AS responses. The various diagnostic operations are described in the following paragraphs.

Normal Transmission

This mode of diagnostic operation is specified by a code of 000. It may be used to verify that the adapter is capable of transmitting, receiving, and processing channel frames correctly.

With this mode of operation, channel frames are transmitted in the same manner as when all segments are not bypassed. Because all segments are bypassed, each channel frame transmitted returns unmodifier to the adapter. Therefore, the AS response indicated by modifier bits 12 through 15 of the XIO control (start loop) is transmitted in each active channel frame control byte. This enables the adapter to process the returning channel frame as though an AS had responded to the channel frame.

Inhibit Start Character

This mode of diagnostic operation is specified by a code of 011. It may be used to verify correct operation of the no-frame detection circuits.

With this mode of operation, /47 is transmitted in place of all start characters.

Single-Step Mode

This mode of diagnostic operation is specified by a code of 100, it may be used to single step through the various data channel sequences performed during adapter operation. To accomplish this, the following steps must be performed after initializing the LCCB's for the desired operation:

1. Issue an XIO control (start loop) with modifier bits 9 through 11 set to 100 and modifier bits 12 through 15 set to the desired AS response.
2. Delay a minimum of 524 μs.
3. Issue an XIO sense device with modifier bits 13 through 15 set to 010. This command loads diagnostic device status word 2 (DDSW2) into the accumulator. If the contents of DDSW2 are zero, return to step 1 to initiate single step for the next loop channel. Otherwise continue with the next step.
4. Issue an XIO sense device with modifier bits 13 through 15 set to 100. This command loads diagnostic device status word 3 (DDSW3) into the accumulator and allows the adapter to initiate a data channel (cycle steal) operation. Allow sufficient time after the XIO for a data channel operation and then return to step 3.

Device status word 1 (DSW1) may be sensed within the preceding sequence to provide more information about the failure. LCCB entries may be modified as desired within the sequence to force errors or special conditions.

Force All Zeros

This mode of diagnostic operation is specified by a code of 101. It may be used to verify that 0-bits can be transmitted and received correctly by the adapter.

With this mode of operation, 0-bits are transmitted to the loop in place of all other information.

Force All Ones

This mode of diagnostic operation is specified by a code of 110. It may be used to verify that 1-bits can be transmitted and received correctly by the adapter.

With this mode of operation, 1-bits are transmitted to the loop in place of all other information.

Force Start Character

This mode of diagnostic operation is specified by a code of 111 and may be used to verify correct operation of the adapter parity detection and start decode circuits.

With this mode of operation, start characters (/39 with even parity) are transmitted in each byte of a channel frame. The even-parity start characters cause an adapter parity error.

ERROR RECOVERY

When a loop channel error occurs, consideration must be given to the effect it has on the area stations and devices on the transmission loop. Loop channel

errors are generally classified as either channel frame transmission errors or data transfer errors.

Channel Frame Transmission Errors

Any of the following frame transmission errors cause the returning channel frame to be stored in the error frame field (LCCB words 6 and 7).

AS ADDRESS CHECK: This error indicates that the AS address byte received does not compare with the one transmitted on the loop. This could be caused by: (1) a bit error on the transmission loop prior to the channel frame reaching the desired AS, or (2) a bit error on the transmission loop after the addressed AS has processed the channel frame. In both of these cases, the disturbed AS address could change to a new AS address which could select the wrong AS.

To analyze an AS address check, the AS response field in the error frame must be examined to determine whether the channel command has been executed. If the response is not valid for the command transmitted, it can be assumed that the AS whose address is in the error frame field did not respond to the command. If the response is valid for the command transmitted, it must be assumed that either the AS whose address was transmitted or the AS whose address is in the error frame field responded to the command. In this case, the program must be able to send end commands with bad status to both area stations.

DEVICE ADDRESS CHECK: This error indicates that the device address received differs from the device address transmitted on the loop. In this case, an end command with error status must be sent to the device whose address appears in the active frame field of the LCCB. If another device address check occurs, an end command must be sent to the device whose address appears in the error frame field of the LCCB.

FRAME CONTROL CHECK: This error indicates that a returning control byte does not have the proper AS response digit and command digit for the command and AS address code transmitted. This error may be caused by noise or other error recovery procedures. For example, an AS address check may result in a nonexistent AS address being returned in a channel frame. When an end command is transmitted to the nonexistent AS, no acknowledgment is returned and a frame control check occurs. This type of frame control check can be ignored.

If a frame control check occurs and the AS response digit is /0 in the returning control byte, the following conditions could exist: (1) the AS is not operational, (2) the AS does not exist, or (3) the AS is bypassed. No recovery action is required for conditions 2 and 3. For condition 1, an end command with error status should be sent.

A frame control check may also occur with an any-AS-address frame if the returning AS address is not any-AS-address code and the response digit is not read request. This error condition causes a frame control check and not an AS address check. If the returning control byte does not indicate a properly acknowledged command, the error is assumed to be a result of noise affecting the AS address byte, and the error may be ignored. If the returning control byte indicates a properly acknowledged command, an end command with error status should be sent to the AS whose address is found in the error frame AS address field. If the returning control byte indicates bypass acknowledge, a restore command must be sent to the AS involved, followed by an end command.

DATA CHECK: This error indicates that the returning data byte differs from the data byte transmitted. Error recovery for a data check (except with an end command) is to send an end command with error status to the addressed device.

A data check with an end command to an AS local I/O device indicates that the AS may have received an improper guidance character. An end command with a guidance character should be retransmitted.

Data Transfer Errors

Data transfer errors do not cause the returning channel frame to be stored in the LCCB error frame field.

SEQUENCE UNUSUAL END: This error occurs if an AS or device returns unusual status during an ending sequence. Sequence unusual end during a write operation indicates that the operation has been terminated without being completed. The program should send a write end command with error status to the AS, thus releasing the AS and device from the write operation. Sequence unusual end with a read operation indicates that the AS and device are waiting to be released. The program should send a read end command with error status.

Note that sequence unusual end is always indicated if the AS is in diagnostic mode.

BYTE COUNT EXCEEDED: This error occurs if the adapter attempts to transfer another byte of data after the byte count has been decreased to

0. It can occur only during a read operation. The program should send a read end command with error status (/80).

DATA STORAGE PROTECT: This error occurs if the adapter attempts to store a byte of data in a storage protected location. It can occur only during a read operation. The program should send a read end command with error status (/80).

CHANNEL TIMED OUT: This error occurs if a channel does not complete a data transfer operation within the time allowed by the program. The program should send an end command with error status (/80).

Appendix A. 1800 Instruction Set

Symbol	Meaning
A	Accumulator
Q	Accumulator Extension
Addr	Contents of the address portion of a two-word instruction
CSL	Core storage location
DISP	Contents of the displacement portion of a one-word instruction
EA	Effective address
EA+1	Next higher address from the effective address
I	Contents of the instruction register
V	Value
XR1	Contents of index register 1
XR2	Contents of index register 2
XR3	Contents of index register 3
X	Hexadecimal value (can be 0-F)
*	Used for hexadecimal values that have limits. See individual instruction in "Instruction Set" for limits.

Hexadecimal Value	Execute I/O (XIO)
08xx	Execute IOCC in CSL at EA (I+DISP) and EA+1
09xx	Execute IOCC in CSL at EA (XR1+DISP) and EA+1
0Axx	Execute IOCC in CSL at EA (XR2+DISP) and EA+1
0Bxx	Execute IOCC in CSL at EA (XR3+DISP) and EA+1
0C00xxxx	Execute IOCC in CSL at EA (Addr) and EA+1
0C80xxxx	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1
0D00xxxx	Execute IOCC in CSL at EA (Addr+XR1) and EA+1
0D80xxxx	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1
0E00xxxx	Execute IOCC in CSL at EA (Addr+XR2) and EA+1
0E80xxxx	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1
0F00xxxx	Execute IOCC in CSL at EA (Addr+XR3) and EA+1
0F80xxxx	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1
	Shift Left Logical A (SLA)
10*x	Shift contents of A left the number of shift counts in DISP
1100	Shift contents of A left the number of shift counts in XR1
1200	Shift contents of A left the number of shift counts in XR2
1300	Shift contents of A left the number of shift counts in XR3
	Shift Left and Count A (SLCA)
10*x	Shift contents of A left the number of shift counts in DISP
1140	Shift contents of A left the number of shift counts in XR1
1240	Shift contents of A left the number of shift counts in XR2
1340	Shift contents of A left the number of shift counts in XR3
	Shift Left Logical A and Q (SLT)
10*x	Shift contents of A and Q left the number of shift counts in DISP
1180	Shift contents of A and Q left the number of shift counts in XR1

Hexadecimal Value	Shift Left Logical A and Q (SLT) (con't)
1280	Shift contents of A and Q left the number of shift counts in XR2
1380	Shift contents of A and Q left the number of shift counts in XR3
	Shift Left and Count A and Q (SLC)
10*x	Shift contents of A and Q left the number of shift counts in DISP
11C0	Shift contents of A and Q left the number of shift counts in XR1
12C0	Shift contents of A and Q left the number of shift counts in XR2
13C0	Shift contents of A and Q left the number of shift counts in XR3
	Shift Right Logical A (SRA)
18*x	Shift contents of A right the number of shift counts in DISP
1900	Shift contents of A right the number of shift counts in XR1
1A00	Shift contents of A right the number of shift counts in XR2
1B00	Shift contents of A right the number of shift counts in XR3
	Shift Right A and Q (SRT)
18*x	Shift contents of A and Q right the number of shift counts in DISP
1980	Shift contents of A and Q right the number of shift counts in XR1
1A80	Shift contents of A and Q right the number of shift counts in XR2
1B80	Shift contents of A and Q right the number of shift counts in XR3
	Rotate Right A and Q (RTE)
18*x	Rotate contents of A and Q right the number of shift counts in DISP
19C0	Rotate contents of A and Q right the number of shift counts in XR1
1AC0	Rotate contents of A and Q right the number of shift counts in XR2
1BC0	Rotate contents of A and Q right the number of shift counts in XR3
	Load Status (LDS)
2000	Set carry and overflow indicators off
2001	Set overflow on and carry off
2002	Set overflow off and carry on
2003	Set carry and overflow indicators on
	Store Status (STS)
28xx	Store status of indicators in CSL at EA (I+DISP)
29xx	Store status of indicators in CSL at EA (XR1+DISP)
2Axx	Store status of indicators in CSL at EA (XR2+DISP)
2Bxx	Store status of indicators in CSL at EA (XR3+DISP)
2C00xxxx	Store status of indicators in CSL at EA (Addr)
2C40xxxx	Clear storage protect bit in CSL at EA (Addr)
2C41xxxx	Write storage protect bit in CSL at EA (Addr)

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Hexadecimal Value	Store Status (STS) (con't)
2C80xxxx	Store status of indicators in CSL at EA (V in CSL at Addr)
2CC0xxxx	Clear storage protect bit in CSL at EA (V in CSL at Addr)
2CC1xxxx	Write storage protect bit in CSL at EA (V in CSL at Addr)
2D00xxxx	Store status of indicators in CSL at EA (Addr+XR1)
2D40xxxx	Clear storage protect bit in CSL at EA (Addr+XR1)
2D41xxxx	Write storage protect bit in CSL at EA (Addr+XR1)
2D80xxxx	Store status of indicators in CSL at EA (V in CSL at "Addr+XR1")
2DC0xxxx	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR1")
2DC1xxxx	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR1")
2E00xxxx	Store status of indicators in CSL at EA (Addr+XR2)
2E40xxxx	Clear storage protect bit in CSL at EA (Addr+XR2)
2E41xxxx	Write Storage protect bit in CSL at EA (Addr+XR2)
2E80xxxx	Store status of indicators in CSL at EA (V in CSL at "Addr+XR2")
2EC0xxxx	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR2")
2EC1xxxx	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR2")
2F00xxxx	Store status of indicators in CSL at EA (Addr+XR3)
2F40xxxx	Clear storage protect bit in CSL at EA (Addr+XR3)
2F41xxxx	Write storage protect bit in CSL at EA (Addr+XR3)
2F80xxxx	Store status of indicators in CSL at EA (V in CSL at "Addr+XR3")
2FC0xxxx	Clear storage protect bit in CSL at EA (V in CSL at "Addr+XR3")
2FC1xxxx	Write storage protect bit in CSL at EA (V in CSL at "Addr+XR3")
	Wait (WAIT)
30XX	Wait until manual start or until an interrupt occurs
	Branch and Store Instruction Register (BSI)
40xx	Store next sequential address in CSL at EA (I+DISP) and branch to EA+1
41xx	Store next sequential address in CSL at EA (XR1+DISP) and branch to EA+1
42xx	Store next sequential address in CSL at EA (XR2+DISP) and branch to EA+1
43xx	Store next sequential address in CSL at EA (XR3+DISP) and branch to EA+1
44*xxxxx (IA=0)	If no condition is true, store next sequential address in CSL at EA (Addr) and branch to EA+1
44*xxxxx (IA=1)	If no condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and branch to EA+1
45*xxxxx (IA=0)	If no condition is true, store next sequential address in CSL at EA (Addr+XR1) and branch to EA+1
45*xxxxx (IA=1)	If no condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and branch to EA+1
46*xxxxx (IA=0)	If no condition is true, store next sequential address in CSL at EA (Addr+XR2) and branch to EA+1
46*xxxxx (IA=1)	If no condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and branch to EA+1
47*xxxxx (IA=0)	If no condition is true, store next sequential address in CSL at EA (Addr+XR3) and branch to EA+1
47*xxxxx (IA=1)	If no condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and branch to EA+1
	Branch or Skip on Condition (BSC or BOSC)
48*x	Skip the next one-word instruction if any condition is true
4C*xxxxx (IA=0)	Branch to CSL at EA (Addr) if no condition is true

Hexadecimal Value	Branch or Skip on Condition (BSC or BOSC) (con't)
4C*xxxxx (IA=1)	Branch to CSL at EA (V in CSL at Addr) if no condition is true
4D*xxxxx (IA=0)	Branch to CSL at EA (Addr+XR1) if no condition is true
4D*xxxxx (IA=1)	Branch to CSL at EA (V in CSL at "Addr+XR1") if no condition is true
4E*xxxxx (IA=0)	Branch to CSL at EA (Addr+XR2) if no condition is true
4E*xxxxx (IA=1)	Branch to CSL at EA (V in CSL at "Addr+XR2") if no condition is true
4F*xxxxx (IA=0)	Branch to CSL at EA (Addr+XR3) if no condition is true
4F*xxxxx (IA=1)	Branch to CSL at EA (V in CSL at "Addr+XR3") if no condition is true
	Load Index (LDX)
60xx	Load expanded DISP into I
61xx	Load expanded DISP into XR1
62xx	Load expanded DISP into XR2
63xx	Load expanded DISP into XR3
6400xxxx	Load Addr into I
6480xxxx	Load contents of CSL at Addr into I
6500xxxx	Load Addr into XR1
6580xxxx	Load contents of CSL at Addr into XR1
6600xxxx	Load Addr into XR2
6680xxxx	Load contents of CSL at Addr into XR2
6700xxxx	Load Addr into XR3
6780xxxx	Load contents of CSL at Addr into XR3
	Store Index (STX)
68xx	Store I in CSL at EA (I+DISP)
69xx	Store XR1 in CSL at EA (I+DISP)
6Axx	Store XR2 in CSL at EA (I+DISP)
6Bxx	Store XR3 in CSL at EA (I+DISP)
6C00xxxx	Store I in CSL at EA (Addr)
6C80xxxx	Store I in CSL at EA (V in CSL at Addr)
6D00xxxx	Store XR1 in CSL at EA (Addr)
6D80xxxx	Store XR1 in CSL at EA (V in CSL at Addr)
6E00xxxx	Store XR2 in CSL at EA (Addr)
6E80xxxx	Store XR2 in CSL at EA (V in CSL at Addr)
6F00xxxx	Store XR3 in CSL at EA (Addr)
6F80xxxx	Store XR3 in CSL at EA (V in CSL at Addr)
	Modify Index and Skip (MDX)
70xx	Add expanded DISP to I (no skip can occur)
71xx	Add expanded DISP to XR1
72xx	Add expanded DISP to XR2
73xx	Add expanded DISP to XR3
74xxxxxx	Add expanded positive or negative DISP to CSL at Addr (add to core storage)
7500xxxx	Add addr to XR1
7580xxxx	Add V in CSL at Addr to XR1
7600xxxx	Add Addr to XR2
7680xxxx	Add V in CSL at Addr to XR2
7700xxxx	Add Addr to XR3
7780xxxx	Add V in CSL at Addr to XR3

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Hexadecimal Value	Add (A)
80xx	Add contents of CSL at EA (I+DISP) to A
81xx	Add contents of CSL at EA (XR1+DISP) to A
82xx	Add contents of CSL at EA (XR2+DISP) to A
83xx	Add contents of CSL at EA (XR3+DISP) to A
8400xxxx	Add contents of CSL at EA (Addr) to A
8480xxxx	Add contents of CSL at EA (V in CSL at Addr) to A
8500xxxx	Add contents of CSL at EA (Addr+XR1) to A
8580xxxx	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8600xxxx	Add contents of CSL at EA (Addr+XR2) to A
8680xxxx	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8700xxxx	Add contents of CSL at EA (Addr+XR3) to A
8780xxxx	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
	Add Double (AD)
88xx	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89xx	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8Axx	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8Bxx	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q
8C00xxxx	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8C80xxxx	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D00xxxx	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8D80xxxx	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 to A and Q
8E00xxxx	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8E80xxxx	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q
8F00xxxx	Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8F80xxxx	Add contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 to A and Q
	Subtract (S)
90xx	Subtract contents of CSL at EA (I+DISP) from A
91xx	Subtract contents of CSL at EA (XR1+DISP) from A
92xx	Subtract contents of CSL at EA (XR2+DISP) from A
93xx	Subtract contents of CSL at EA (XR3+DISP) from A
9400xxxx	Subtract contents of CSL at EA (Addr) from A
9480xxxx	Subtract contents of CSL at EA (V in CSL at Addr) from A
9500xxxx	Subtract contents of SCL at EA (Addr+XR1) from A
9580xxxx	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9600xxxx	Subtract contents of CSL at EA (Addr+XR2) from A
9680xxxx	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A
9700xxxx	Subtract contents of CSL at EA (Addr+XR3) from A
9780xxxx	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") from A
	Subtract Double (SD)
98xx	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
99xx	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q
9Axx	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9Bxx	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00xxxx	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9C80xxxx	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q

Hexadecimal Value	Subtract Double (SD) (con't)
9D00xxxx	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q
9D80xxxx	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E00xxxx	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A And Q
9E80xxxx	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q
9F00xxxx	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q
9F80xxxx	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
	Multiply (M)
A0xx	Multiply contents of CSL at EA (I+DISP) by A
A1xx	Multiply contents of CSL at EA (XR1+DISP) by A
A2xx	Multiply contents of CSL at EA (XR2+DISP) by A
A3xx	Multiply contents of CSL at EA (XR3+DISP) by A
A400xxxx	Multiply contents of CSL at EA (Addr) by A
A480xxxx	Multiply contents of CSL at EA (V in CSL at Addr) by A
A500xxxx	Multiply contents of CSL at EA (Addr+XR1) by A
A580xxxx	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A600xxxx	Multiply contents of CSL at EA (Addr+XR2) by A
A680xxxx	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A
A700xxxx	Multiply contents of CSL at EA (Addr+XR3) by A
A780xxxx	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	Divide (D)
A8xx	Divide A and Q by contents of CSL at EA (I+DISP)
A9xx	Divide A and Q by contents of CSL at EA (XR1+DISP)
AAxx	Divide A and Q by contents of CSL at EA (XR2+DISP)
ABxx	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00xxxx	Divide A and Q by contents of CSL at EA (Addr)
AC80xxxx	Divide A and Q by contents of CSL at EA (V in CSL at Addr)
AD00xxxx	Divide A and Q by contents of CSL at EA (Addr+XR1)
AD80xxxx	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")
AE00xxxx	Divide A and Q by contents of CSL at EA (Addr+XR2)
AE80xxxx	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2")
AF00xxxx	Divide A and Q by contents of CSL at EA (Addr+XR3)
AF80xxxx	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")
	Compare (CMP)
B0xx	Compare A with contents of CSL at EA (I+DISP)
B1xx	Compare A with contents of CSL at EA (XR1+DISP)
B2xx	Compare A with contents of CSL at EA (XR2+DISP)
B3xx	Compare A with contents of CSL at EA (XR3+DISP)
B400xxxx	Compare A with contents of CSL at EA (Addr)
B480xxxx	Compare A with contents of CSL at EA (V in CSL at Addr)
B500xxxx	Compare A with contents of CSL at EA (Addr+XR1)
B580xxxx	Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")
B600xxxx	Compare A with contents of CSL at EA (Addr+XR2)
B680xxxx	Compare A with contents of CSL at EA (V in CSL at "Addr+XR2")
B700xxxx	Compare A with contents of CSL at EA (Addr+XR3)
B780xxxx	Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")

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Hexadecimal Value	Double Compare (DCM)
B8xx	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1
B9xx	Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1
BAxx	Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1
BBxx	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1
BC00xxxx	Compare A and Q with contents of CSL at EA (Addr) and EA+1
BC80xxxx	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA+1
BD00xxxx	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1
BD80xxxx	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1
BE00xxxx	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1
BE80xxxx	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1
BF00xxxx	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1
BF80xxxx	Compare A and Q with contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1
	Load Accumulator (LD)
C0xx	Load contents of CSL at EA (I+DISP) into A
C1xx	Load contents of CSL at EA (XR1+DISP) into A
C2xx	Load contents of CSL at EA (XR2+DISP) into A
C3xx	Load contents of CSL at EA (XR3+DISP) into A
C400xxxx	Load contents of CSL at EA (Addr) into A
C480xxxx	Load contents of CSL at EA (V in CSL at Addr) into A
C500xxxx	Load contents of CSL at EA (Addr+XR1) into A
C580xxxx	Load contents of CSL at EA (V in CSL at "Addr+XR1") into A
C600xxxx	Load contents of CSL at EA (Addr+XR2) into A
C680xxxx	Load contents of CSL at EA (V in CSL at "Addr+XR2") into A
C700xxxx	Load contents of CSL at EA (Addr+XR3) into A
C780xxxx	Load contents of CSL at EA (V in CSL at "Addr+XR3") into A
	Load Double (LDD)
C8xx	Load contents of CSL at EA (I+DISP) and EA+1 into A and Q
C9xx	Load contents of CSL at EA (XR1+DISP) and EA+1 into A and Q
CAxx	Load contents of CSL at EA (XR2+DISP) and EA+1 into A and Q
CBxx	Load contents of CSL at EA (XR3+DISP) and EA+1 into A and Q
CC00xxxx	Load contents of CSL at EA (Addr) and EA+1 into A and Q
CC80xxxx	Load contents of CSL at EA (V in CSL at Addr) and EA+1 into A and Q
CD00xxxx	Load contents of CSL at EA (Addr+XR1) and EA+1 into A and Q
CD80xxxx	Load contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 into A and Q
CE00xxxx	Load contents of CSL at EA (Addr+XR2) and EA+1 into A and Q
CE80xxxx	Load contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 into A and Q
CF00xxxx	Load contents of CSL at EA (Addr+XR3) and EA+1 into A and Q
CF80xxxx	Load contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 into A and Q

Hexadecimal Value	Store Accumulator (STO)
D0xx	Store contents of A in CSL at EA (I+DISP)
D1xx	Store contents of A in CSL at EA (XR1+DISP)
D2xx	Store contents of A in CSL at EA (XR2+DISP)
D3xx	Store contents of A in CSL at EA (XR3+DISP)
D400xxxx	Store contents of A in CSL at EA (Addr)
D480xxxx	Store contents of A in CSL at EA (V in CSL at Addr)
D500xxxx	Store contents of A in CSL at EA (Addr+XR1)
D580xxxx	Store contents of A in CSL at EA (V in CSL at "Addr+XR1")
D600xxxx	Store contents of A in CSL at EA (Addr+XR2)
D680xxxx	Store contents of A in CSL at EA (V in CSL at "Addr+XR2")
D700xxxx	Store contents of A in CSL at EA (Addr+XR3)
D780xxxx	Store contents of A in CSL at EA (V in CSL at "Addr+XR3")
	Store Double (STD)
D8xx	Store contents of A and Q in CSL at EA (I+DISP) and EA+1
D9xx	Store contents of A and Q in CSL at EA (XR1+DISP) and EA+1
DAxx	Store contents of A and Q in CSL at EA (XR2+DISP) and EA+1
DBxx	Store contents of A and Q in CSL at EA (XR3+DISP) and EA+1
DC00xxxx	Store contents of A and Q in CSL at EA (Addr) and EA+1
DC80xxxx	Store contents of A and Q in CSL at EA (V in CSL at Addr) and EA+1
DD00xxxx	Store contents of A and Q in CSL at EA (Addr+XR1) and EA+1
DD80xxxx	Store contents of A and Q in CSL at EA (V in CSL at "Addr+XR1") and EA+1
DE00xxxx	Store contents of A and Q in CSL at EA (Addr+XR2) and EA+1
DE80xxxx	Store contents of A and Q in CSL at EA (V in CSL at "Addr+XR2") and EA+1
DF00xxxx	Store contents of A and Q in CSL at EA (Addr+XR3) and EA+1
DF80xxxx	Store contents of A and Q in CSL at EA (V in CSL at "Addr+XR3") and EA+1
	Logical AND (AND)
E0xx	AND contents of CSL at EA (I+DISP) with A
E1xx	AND contents of CSL at EA (XR1+DISP) with A
E2xx	AND contents of CSL at EA (XR2+DISP) with A
E3xx	AND contents of CSL at EA (XR3+DISP) with A
E400xxxx	AND contents of CSL at EA (Addr) with A
E480xxxx	AND contents of CSL at EA (V in CSL at Addr) with A
E500xxxx	AND contents of CSL at EA (Addr+XR1) with A
E580xxxx	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
E600xxxx	AND contents of CSL at EA (Addr+XR2) with A
E680xxxx	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A
E700xxxx	AND contents of CSL at EA (Addr+XR3) with A
E780xxxx	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical OR (OR)
E8xx	OR contents of CSL at EA (I+DISP) with A
E9xx	OR contents of CSL at EA (XR1+DISP) with A
EAxx	OR contents of CSL at EA (XR2+DISP) with A
EBxx	OR contents of CSL at EA (XR3+DISP) with A
EC00xxxx	OR contents of CSL at EA (Addr) with A
EC80xxxx	OR contents of CSL at EA (V in CSL with Addr) with A

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Hexadecimal Value	Logical OR (OR) (con't)
ED00xxxx	OR contents of CSL at EA (Addr+XR1) with A
ED80xxxx	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE00xxxx	OR contents of CSL at EA (Addr+XR2) with A
EE80xxxx	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF00xxxx	OR contents of CSL at EA (Addr+XR3) with A
EF80xxxx	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Exclusive OR (EOR)
F0xx	EOR contents of CSL at EA (I+DISP) with A
F1xx	EOR contents of CSL at EA (XR1+DISP) with A

Hexadecimal Value	Logical Exclusive OR (EOR) (con't)
F2xx	EOR contents of CSL at EA (XR2+DISP) with A
F3xx	EOR contents of CSL at EA (XR3+DISP) with A
F400xxxx	EOR contents of CSL at EA (Addr) with A
F480xxxx	EOR contents of CSL at EA (V in CSL at Addr) with A
F500xxxx	EOR contents of CSL at EA (Addr+XR1) with A
F580xxxx	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F600xxxx	EOR contents of CSL at EA (Addr+XR2) with A
F680xxxx	EOR contents of CSL at EA (V in CSL at "Addr+XR2) with A
F700xxxx	EOR contents of CSL at EA (Addr+XR3) with A
F780xxxx	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A

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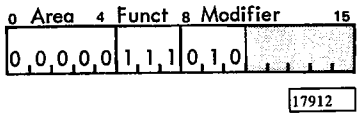
Appendix B. I/O Device Addressing

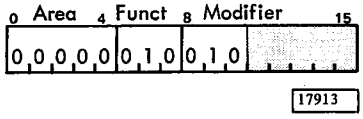
The area, function, and modifier codes listed below are required for 1800 I/O operations. Unused positions are indicated by the shaded areas. Refer to end of Appendix B for all notes.

CONSOLE DATA ENTRY SWITCHES

SENSE DEVICE: Move switch data to accumulator.

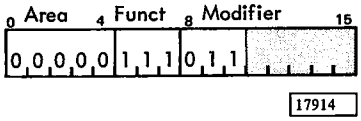


READ: Move switch data to core storage location specified by IOCC address word.

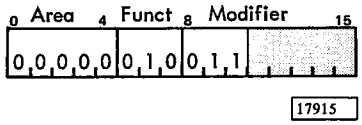


CONSOLE SENSE, PROGRAM, AND CE SWITCHES

SENSE DEVICE: Move switch data to accumulator.

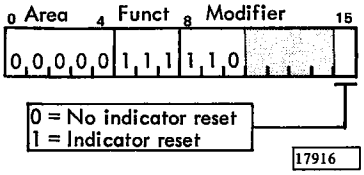


READ: Move switch data to core storage location specified by IOCC address word.



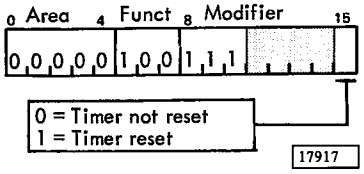
CONSOLE INTERRUPT

SENSE DEVICE: Move console DSW to accumulator



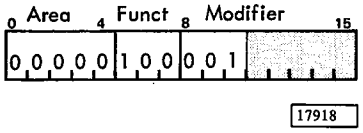
OPERATIONS MONITOR

CONTROL: Set or reset timer.



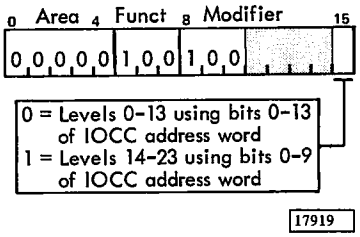
INTERVAL TIMERS

CONTROL: Start or stop timers according to bits 0, 1, and 2 of IOCC address word.



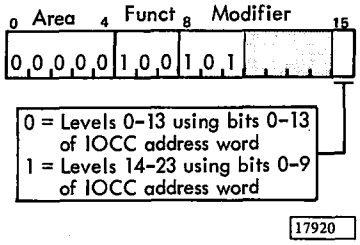
INTERRUPT MASK REGISTER

CONTROL: Mask or unmask interrupt levels.



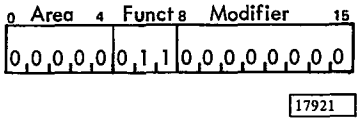
PROGRAM INTERRUPT

CONTROL: Set interrupt levels.



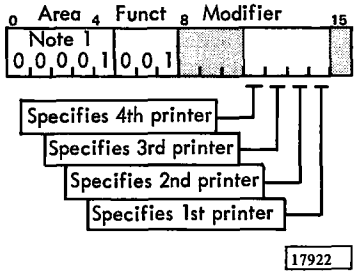
INTERRUPT LEVEL STATUS WORD

SENSE INTERRUPT: Move ILSW of highest priority interrupt level active to accumulator.

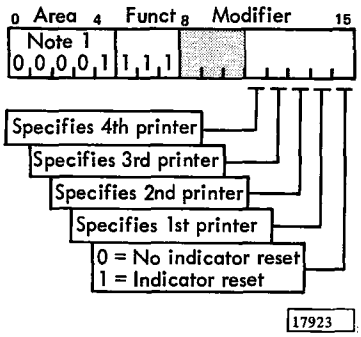


1053 PRINTER AND 1816 PRINTER-KEYBOARD

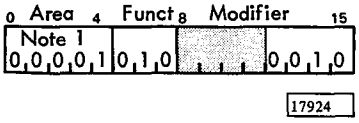
WRITE: Print single character from core storage location specified by IOCC address word.



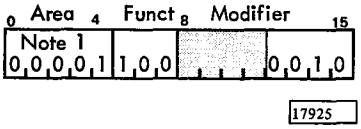
SENSE DEVICE: Move 1053/1816 DSW to accumulator.



READ: Move single 1816 keyboard character to core storage location specified by IOCC address word.

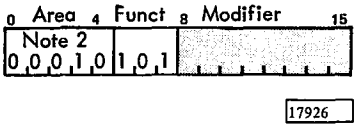


CONTROL: Place keyboard in ready status.

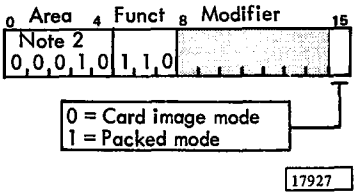


1442 CARD READ PUNCH

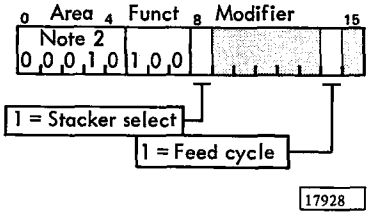
INITIALIZE WRITE: Punch contents of data table specified by IOCC address word into card columns.



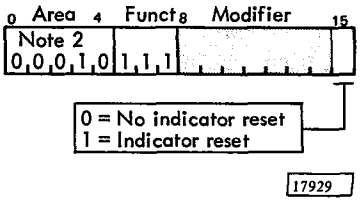
INITIALIZE READ: Move data in card columns to to data table specified by IOCC address word.



CONTROL: Feed card or stacker select.

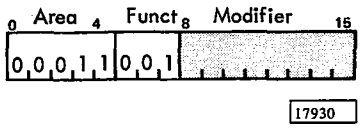


SENSE DEVICE: Move DSW to accumulator.

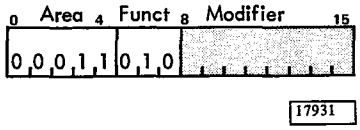


1054 AND 1055 PAPER TAPE

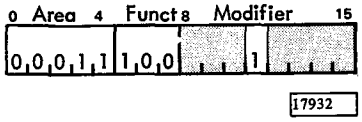
WRITE: Punch contents of core storage location specified by IOCC address word into tape.



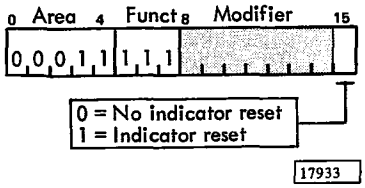
READ: Move character from tape buffer to core storage location specified by IOCC address word.



CONTROL: Move one character from tape to tape buffer.

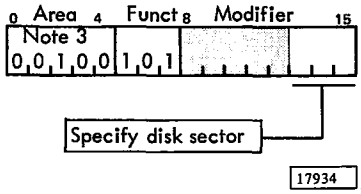


SENSE DEVICE: Move DSW to accumulator

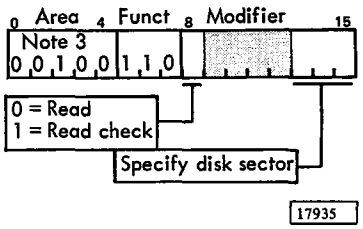


1810 DISK STORAGE DRIVE

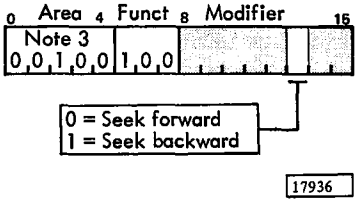
INITIALIZE WRITE: Move contents of data table specified by IOCC address word to disk sector.



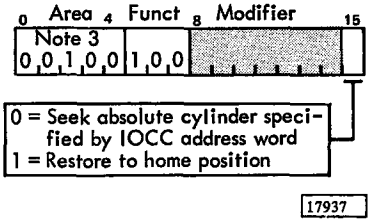
INITIALIZE READ: Move contents of disk sector to data table specified by IOCC address word.



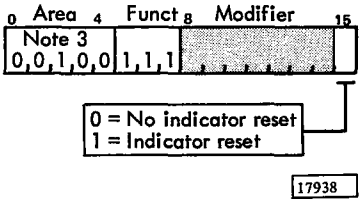
CONTROL A MODEL: Seek number of cylinders specified by IOCC address word.



CONTROL B MODEL: Seek cylinder or restore.

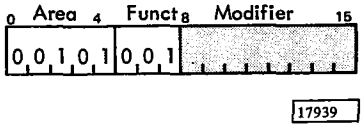


SENSE DEVICE: Move DSW to accumulator

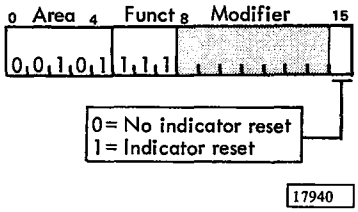


1627 PLOTTER

WRITE: Move contents of core storage location specified by IOCC address word to plotter.

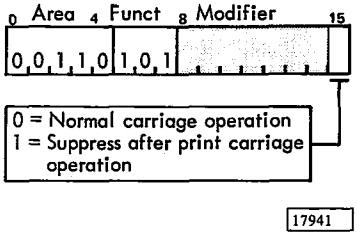


SENSE DEVICE: Move DSW to accumulator.

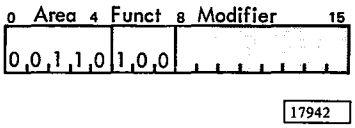


1443 PRINTER

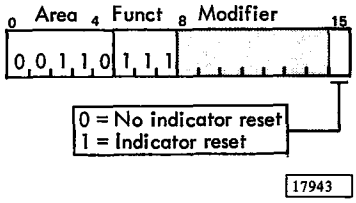
INITIALIZE WRITE: Move contents of data table specified by IOCC address word to printer.



CONTROL: Initiate carriage operation defined by bits 0-7 of IOCC address word.

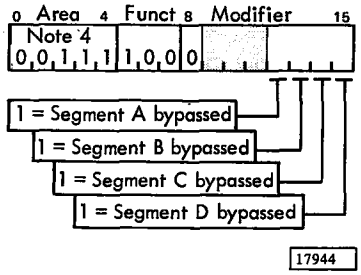


SENSE DEVICE: Move DSW to accumulator.

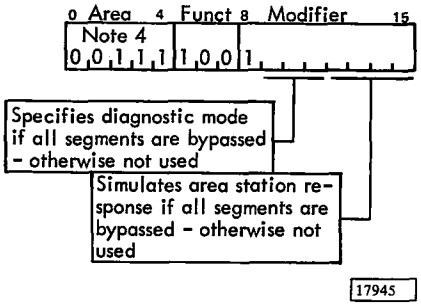


2790 ADAPTER

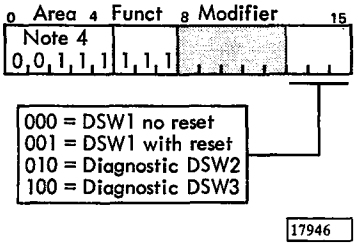
CONTROL: Stop loop.



CONTROL: Start loop.

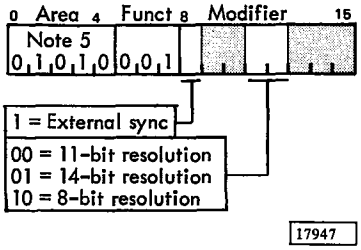


SENSE DEVICE: Move DSW to accumulator.

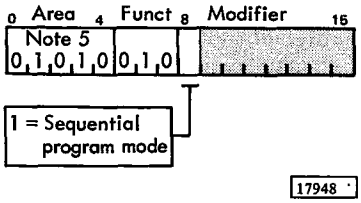


ANALOG INPUT

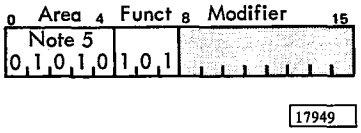
WRITE: Move multiplexer address from core storage to AMAR. Selected analog in point reading moves to ADC.



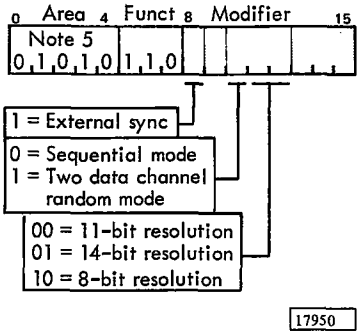
READ: Move ADC reading to core storage location specified by address word of IOCC.



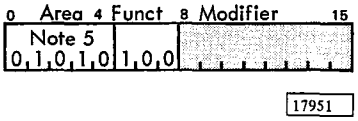
INITIALIZE WRITE: Move contents of multiplexer address table specified by IOCC address word to AMAR.



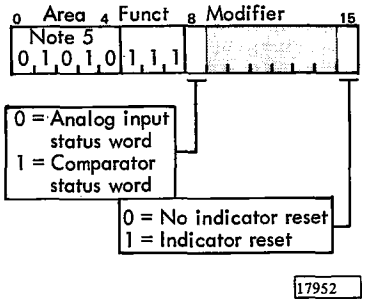
INITIALIZE READ: Move ADC readings to data table specified by IOCC address word.



CONTROL: Cause blast reset of ADC, multiplexer, and comparator.

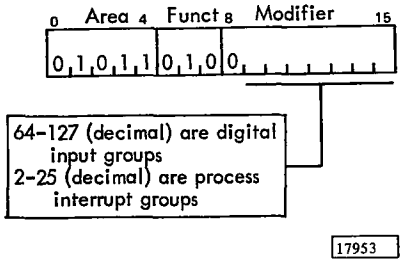


SENSE DEVICE: Move DSW to accumulator.

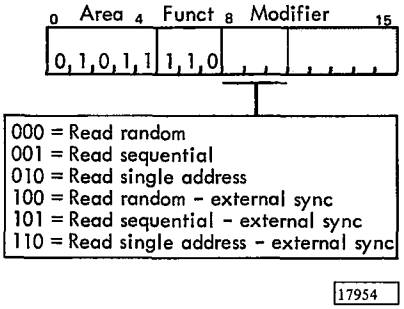


DIGITAL INPUT

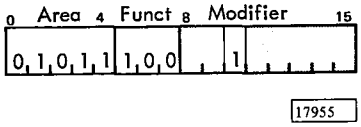
READ: Move digital input or process interrupt group readings to core storage location specified by address word of IOCC.



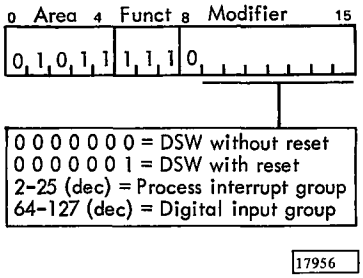
INITIALIZE READ: Move digital input readings to data table specified by IOCC address word.



CONTROL: Cause blast reset of all basic digital input controls.

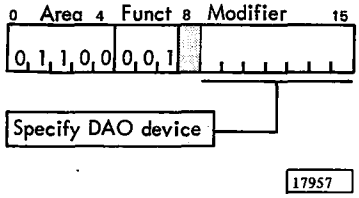


SENSE DEVICE: Move DSW, digital input group, or process interrupt group to accumulator.

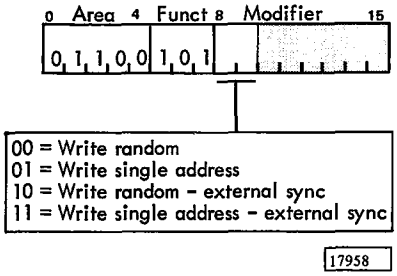


DIGITAL AND ANALOG OUTPUT

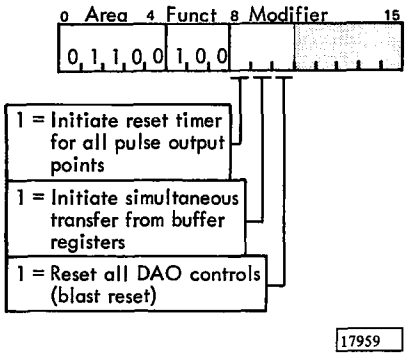
WRITE: Move contents of core storage location specified by IOCC address word to DAO device.



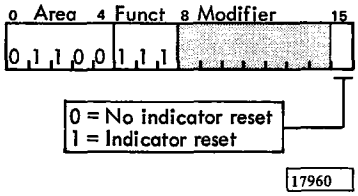
INITIALIZE WRITE: Move contents of data table specified by IOCC address word to DAO.



CONTROL:

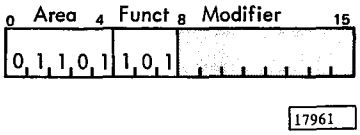


SENSE DEVICE: Move DSW to accumulator.

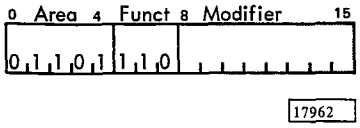


SYSTEM/360 ADAPTER

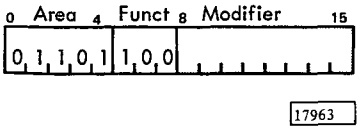
INITIALIZE WRITE: Move contents of data table specified by IOCC address word to System/360 adapter.



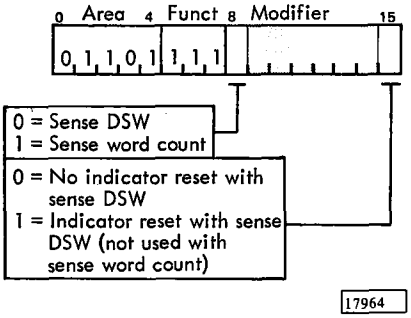
INITIALIZE READ: Move System/360 adapter data to data table specified by IOCC address word.



CONTROL: Reset.

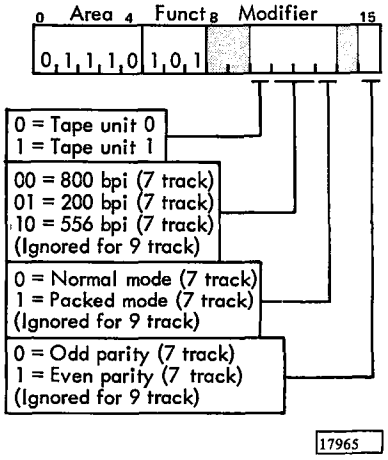


SENSE DEVICE: Move DSW or word count to accumulator.

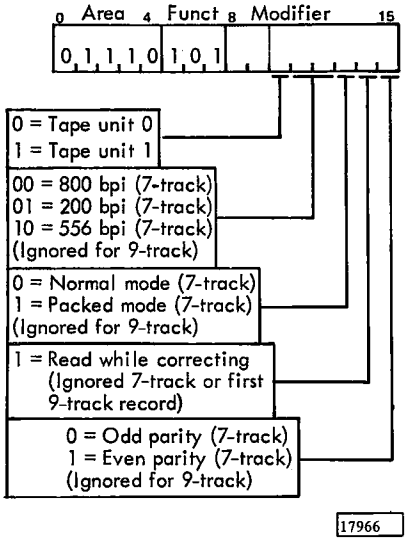


2401 OR 2402 MAGNETIC TAPE

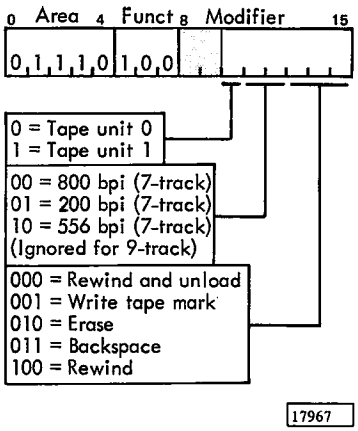
INITIALIZE WRITE: Move contents of data table specified by IOCC address word to tape unit.



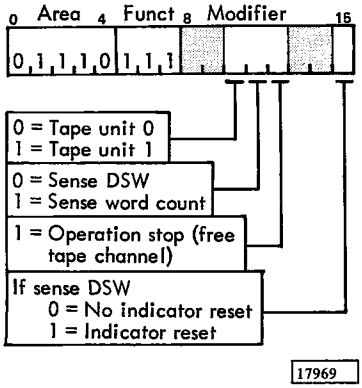
INITIALIZE READ: Move tape data to data table specified by IOCC address word.



CONTROL: Select tape unit and/or control function.

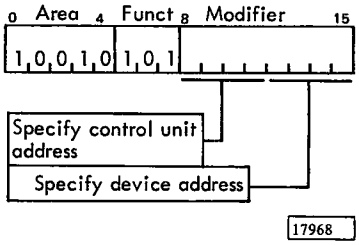


SENSE DEVICE: Move DSW or word count to accumulator.

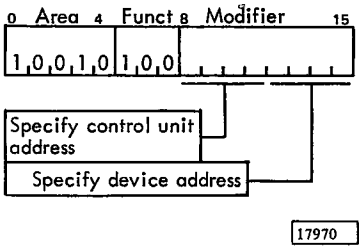


SELECTOR CHANNEL

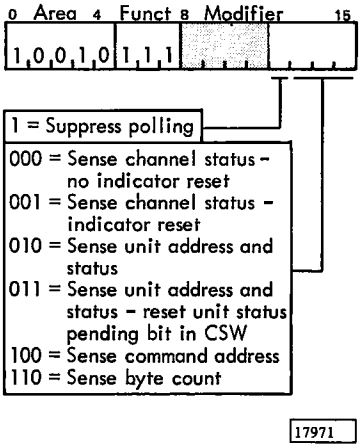
INITIALIZE WRITE: Start I/O.



CONTROL: Halt I/O.

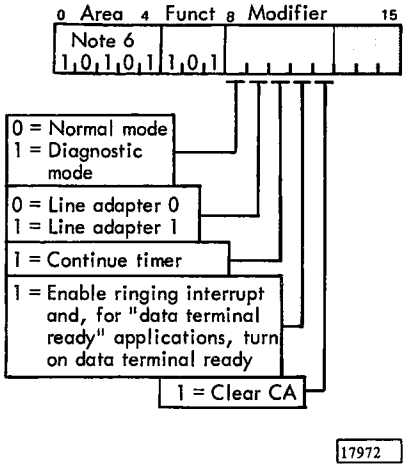


SENSE DEVICE: Move channel status word, unit address and status, command address, or byte count to accumulator.

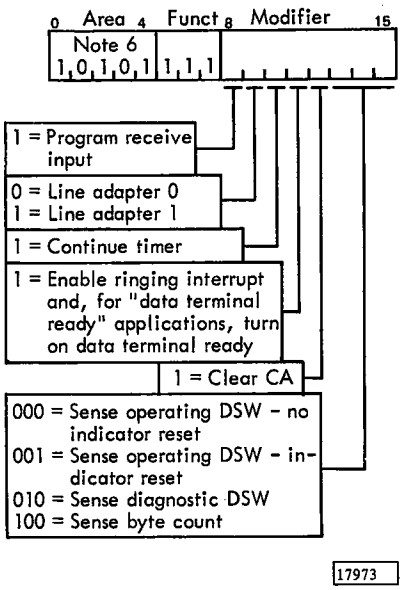


COMMUNICATIONS ADAPTERS

INITIALIZE WRITE: IOCC address word specifies core storage data table.



SENSE DEVICE: Move operating DSW, diagnostic DSW, or byte count to accumulator.



NOTES:

1. Area code for second four printers is 01111.
2. Area code for second 1442 is 10001.
3. The second and third 1810 drives require area codes of 01000 and 01001, respectively.
4. Area code for second 2790 adapter is 10011.
5. Area code for analog input expander is 10000.
6. Area codes for second, third and fourth communications adapters are:

   Second = 10110.
   Third = 10111.
   Fourth = 10100.

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Console Interrupt	• Interrupt Request															
	Interval Timers	• Timer A	• Timer B	• Timer C													
	Data Entry Switches	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Sense Switches	← Sense → 0	1	2	3	← Program → 4	5	6	7	← CE Sense → 8	9	10	11	12	13	14	15
1–15	1816 Printer-Keyboard 1053 Printer -In First Group -In Second Group	• Printer Service Response	• Keyboard Service Response (1816)	• Keyboard Request (1816)		Printer Busy	Printer Not Ready	Keyboard Not Ready	Storage Protect Violation (1816)	Keyboard Parity Error (1816)	Printer Parity Error			† CE Busy	† CE Not Ready		
2–17–	1442 Card Read Punch -First -Second			Any Error	Last Card	• Operation Complete	Parity Error	Storage Protect Violation	Feed Check Read Station					† CE Busy	† CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	PT Reader Any Error	• PT Reader Service Request	PT Punch Parity Error	• PT Punch Service Request	PT Reader Busy	PT Reader Not Ready	PT Punch Busy	PT Punch Not Ready	PT Reader Parity Error	PT Reader Storage Protect	† CE PT Reader Busy	† CE PT Reader Not Ready	† CE PT Punch Busy	† CE PT Punch Not Ready		
4–8–9–	1810 Disk Storage "A" First Drive Second Drive Third Drive	Any Error	• Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Violation	Data Error	Write Select Error	Overrun		† CE Not Ready	† CE Busy		Sector Count High	Sector Count Low
4–8–9–	1810 Disk Storage "B" First Drive Second Drive Third Drive	Any Error	• Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Violation	Data Error	Write Select Error	Overrun	Seek Error	† CE Not Ready	† CE Busy	B Model Access	Sector Count High	Sector Count Low
5	1627 Plotter	• Service Response	Parity Error											† CE Busy	† CE Not Ready	Busy	Not Ready
6	1443 Printer	• Transfer Complete	Error	• Print Complete	Channel 9	Channel 12	Channel 1	Parity Error				† CE Carriage Busy	† CE Printer Busy	† CE Printer Not Rdy	Carriage Busy	Printer Busy	Printer Not Ready
7–19–	2790 Adapters -First -Second Status (DSW1)	• Adapter Error Interrupt	Command Reject	No Frame	Storage Protect Violation	P-C Parity Error	Adapter Parity Error	Loop Parity Error	• Loop Channel Interrupt	Sync Fill Error		Adapter Active		Segment A Bypass	Segment B Bypass	Segment C Bypass	Segment D Bypass
	Diagnostic (DDSW2)		← DC Cycle Steal Counter → Position 4	Position 2	Position 1		Store CSW	Deactivate Channel	Channel Interrupt Store	Data Buffer Read	Data Buffer Write	Buffer Cycle Command Update	Channel Timer	Area Station Capture or Command Update	Update ISW	Input Frame Fetch	Output Frame Fetch
	Diagnostic (DDSW3)	← Table Address Register Bits → 0	1	2	3	4	5	6	7	← Input Channel Counter Bits → 0	1	2	3	Note: If all segments bypassed, DDSW3 reflects status of In-Bus instead of TAR and ICC.			
10–16–	Analog Input -Basic -Expander	• End of Table	• DPC SS Conv Complete	• DPC Rly Conv Complete	• Storage Protect Violation	• Parity Control Error	• Parity Data Error	• ADC Overload	• Overlap Conflict	Cyc Steal, SS, AMAR Busy	DPC Relay Busy						Any Error
10–16–	Comparator -AI Basic -AI Expander	• High Out of Limit	• Low Out of Limit		AMAR SS MPX			← Analog Multiplexer Address Register Bits → 512	256	128	64	32	16	8	4	2	1

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AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
11	Digital Input	• Parity Error	• Storage Protect Violation	• DI Scan Complete	• Command Reject												DI Busy
	PISW	← Process Interrupt Points (Customer Assigned Groups) →															
12	Digital and Analog Output	• Parity Error	Pulse Output Timer	• D & A Out Scan Complete	• Command Reject	Data Channel Active											D/AO Busy
13	S/360 Adapter	• Command Reject	1800 Command Stored	• 360 Command Stored	• Halt	• Data Check	• Storage Protect Violation	• Transfer End	• End of Table	← 360 Command Byte →							
	Adapter Word Counter			← Word Count (1's Complement) →													
14	Tape Control Unit		Tape Unit 1 Select	• Command Reject	• End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Data Bus Out or P-C Parity Error	Overrun	• Operation Complete	CE Diagnostic Indicator	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Busy or Rewind	Tape Busy or Not Ready
	TCU Word Counter	00 = True Count 11 = 1's Complement		← Word Count →													
18-	Selector Channel Status	• Not Operational	• Unit Status Pending	• Program Control Interrupt	• Program Check	Channel Data Check	Interface Control Check	Incorrect Length	Adapter Busy	Unit Operational							
	Unit Address and Status	← Control Unit Address →				← Device Address →				Attention	Status Modifier	Control Unit End	Busy	Channel End	Device End	Unit Check	Unit Exception
	SC Command Address	← Last CCW Address + 3 →															
	SC Byte Count	← Residual Byte Count (2's Complement +1) →															
21- 22- 23- 20-	CA Line Adapter(s) -First CA -Second CA -Third CA -Fourth CA	• Channel Stop	• Storage Protect Violation	• Time Out	• END Character Decoded or Ringing	• End of Table	Parity Error	BCC Error	Overrun	Data Set Ready	• Command Reject	Carrier On					
	Adapter Byte Counter	← CE Diagnostic Bits †† →			Transmit Latch	← Byte Count (1's Complement) →											
	Adapter Diagnostic	†† CE Diagnostic Bit	Character Phase	Character Trigger †	Clear to Send Off	Transparent Trigger	Text Trigger	End Trigger	Transmit Line Bit Trigger	← Serializer-Deserializer → Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7

• Interrupt conditions.
† Active only in CE mode.
†† Active only when wired by CE. Otherwise always 1's.

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IBM 3800 Printing Subsystem Functional Characteristics Printed in U.S.A. GA26-5918-8

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IBM Technical Newsletter

File Number 1800-01

Re: Form No. GA26-5918-8

This Newsletter No. GN26-0263

Date October 1, 1970

Previous Newsletter Nos. None

IBM 1800 FUNCTIONAL CHARACTERISTICS

This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are listed below.

77,78
223 through 232
239 through 242
242.1, 242.2 (added only)
243 through 250
269, 270
277 through 280
291, 292

A change to the text or a small change to an illustration is indicated by a vertical line to the left of the change; a changed or added illustration is denoted by the symbol • to the left of the caption.

Summary of Amendments

1. Provide information for the Pulse Count Adapter feature for the 2793 Area Station.
2. Provide information for the External Alarm Feature.

Note: Please file this cover letter at the back of the manual to provide a record of changes.

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IBM Technical Newsletter

Unit 1800-01

Base Publ. No. GA26-5918-8

This Newsletter No. GN26-0269

Date July 14, 1971

Previous Newsletter Nos. GN26-0263

IBM 1800 FUNCTIONAL CHARACTERISTICS

This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are listed below.

5 through 10	103 through 106	219, 220
25, 26	131 through 136	223 through 232
47 through 56	139, 140	237, 238
59 through 64	145, 146	241, 242
67 through 72	151, 152	245, 246
77, 78	155, 156	255, 256
83 through 86	175, 176	271, 272
89, 90	191, 192	277, 278
93 through 96	199 through 202	283, 284

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Summary of Amendments

1. Provide information about the 2797 Data Entry Unit for the 2790 adapter.
2. Provide information about the purpose of CE core storage.
3. Include miscellaneous editorial changes.

Note: Please file this cover letter at the back of the manual to provide a record of changes.

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IBM Technical Newsletter

Unit 1800-01

Base Publ. No. GA26-5918-8

This Newsletter No. GN26-0282

Date January 31, 1972

Previous Newsletter Nos. GN26-0263
GN26-0269

IBM 1800 FUNCTIONAL CHARACTERISTICS

This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are listed below.

77, 78
229, 230
231 through 238 (text rearrangement only)

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Summary of Amendments

Provide additional information regarding increment timer accuracy.

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00110	~~SHIFT L~~ WAIT	CMP
00111	~~SHIFT R (ROT)~~	DCM
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01001	BSC	LDD
01010	—	STO
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